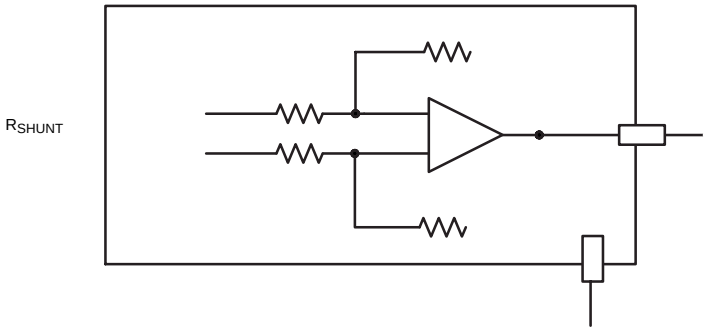


$V_{OUT} = (I_{LOAD} \times R_{SHUNT}) * GAIN + V_{REF}$

Figure 1. Example Application Schematic of High−Side Current Sensing

MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Supply Voltage (Note 1)		V_S	−0.3 to 6	V
IN+, IN−, CIN+, CIN−	Differential (V_{IN+}) − ($V_{IN−}$) (Note 2)	V_{IN+},$V_{IN−}$	44	V
	Common−Mode (Note 2)		−0.3 to +44	
REF Input		V_{REF}	GND−0.3 to (V_S) +0.3	V
EN Input		V_{EN}	GND−0.3 to (V_S) +0.3	V
Output (Note 2)		V_{OUT}	GND−0.3 to (V_S) +0.3	V
Input Current into Any Pin (Note 2)		I_{IN}	±10	mA
Operating Temperature		T_A	−40 to +150	°C
Storage Temperature		T_{STG}	−65 to +150	°C
Junction Temperature		$T_{J(max)}$	+150	°C
ESD Capability, Human Body Model (Note 3)		HBM	±2000	V
Charged Device Model (Note 3)		CDM	±1000	V
Latch−up Current (Note 4)			±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for safe operating parameters.
2. Input voltage at any pin may exceed the voltage shown if current at that pin is limited to ±10 mA.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per JEDEC standard JS−001−2017
   ESD Charged Device Model tested per JEDEC standard JS−002−2014
4. Latch−up Current tested per JEDEC standard JESD78E

THERMAL CHARACTERISTICS

Parameter	Symbol	Micro10 / MSOP10	SC88 / SC70−6 / SOT−363	Unit
Junction−to−ambient thermal resistance (Notes 5, 6)	θ_{JA}	180	188	°C/W
Junction−to−case thermal resistance (Notes 5, 6)	$\theta_{JC(top)}$	71	128	°C/W
Junction−to−top thermal characterization (Notes 5, 6)	Ψ_{JT}	1.6	21	°C/W
Junction−to−board thermal characterization (Notes 5, 6)	Ψ_{JB}	98	91	°C/W

5. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for safe operating parameters.
6. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate. (reference JESD51).

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Conditions	Min	Max	Unit
Operating Temperature	T_A	NCS prefix	−40	125	°C
		NCV prefix	−40	125	
Common Mode Input Voltage	V_{CM}	Full temperature range	−0.1	40	V
Supply Voltage	V_S	Full temperature range	1.8	5.5	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

[redacted]

2, unless otherwise noted. **Boldface** limits

				Min	Typ	Max	Unit
				109	127	–	dB
				109	127	–	
				109	134	–	
				109	134	–	
				–	±9	±19	μV
				–	±4	±12	
				–	±3	±10	
				–	±2	±10	
				–	±1	±60	μV
				–	±1	±40	
				–	±1	±25	
			G = 200	–	±1	±25	
Input Offset Voltage Drift vs. Temperature, RTI (Note 7)	DV_{OS} / dT	V_{SENSE} = 0 mV		–	±0.1	±0.5	μV/°C
Power Supply Rejection Ratio	PSRR	V_S = 1.8 V to 5.5 V, V_{SENSE} = 0mV		–	±1.0	**±10**	μV/V
Input Bias Current	I_{IB}	V_{SENSE} = 0 mV		–	29	35	μA
Input Bias Current in Shutdown (Note 10)	I_{IBSD}	V_{SENSE} = 0mV		–	–	140	nA
Input Bias Current in Shutdown (Note 10)	I_{IBSD}	T_A = −40 °C to 125 °C		–	–	**500**	nA
Input Offset Current	I_{IO}	V_{SENSE} = 0 mV		–	±0.3	–	μA
Enable Input Threshold Voltage	$V_{th(EN)}$	Enabled		1.4	–	–	V

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_{SENSE} = (V_{IN+}) − (V_{IN-}ACC, VwAó[illegible]

TYPICAL CHARACTERISTICS (At T_A = +25°C, V_{SENSE} = $(V_{IN+}) – (V_{IN–})$; V_S = V_{EN} = 1.8 V, V_{REF} = V_S/2, V_{CM} =12 V, and all gains unless otherwise noted.) (continued)

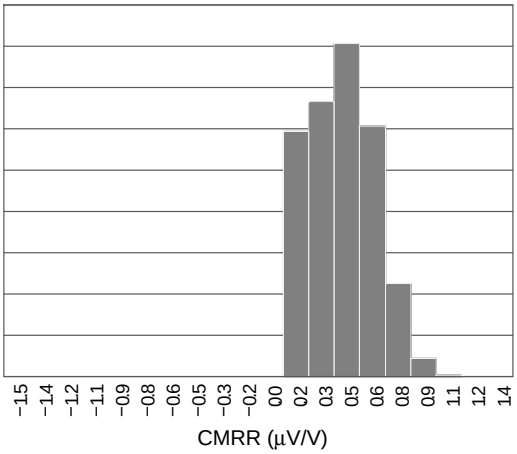


Figure 5b. Common Mode Rejection Ratio Distribution, G50

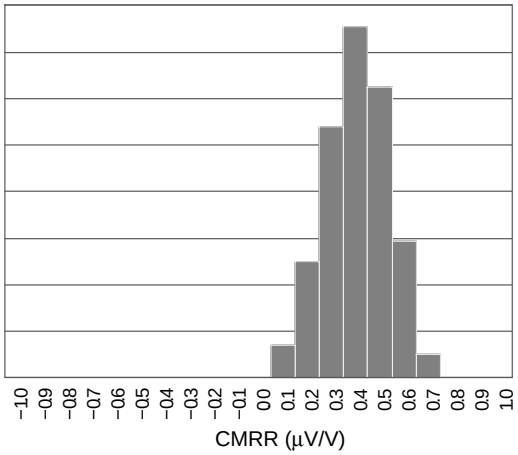


Figure 5c. Common Mode Rejection Ratio Distribution, G100

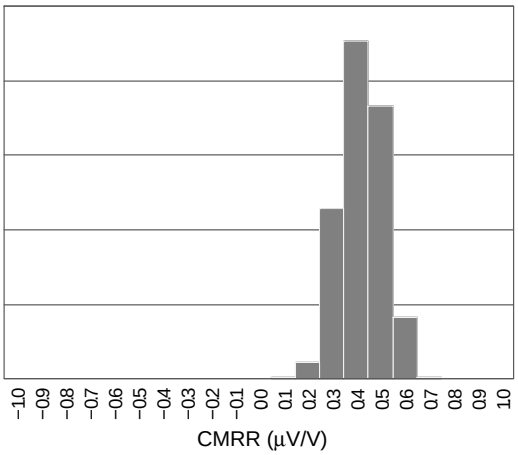


Figure 5d. Common Mode Rejection Ratio Distribution, G200

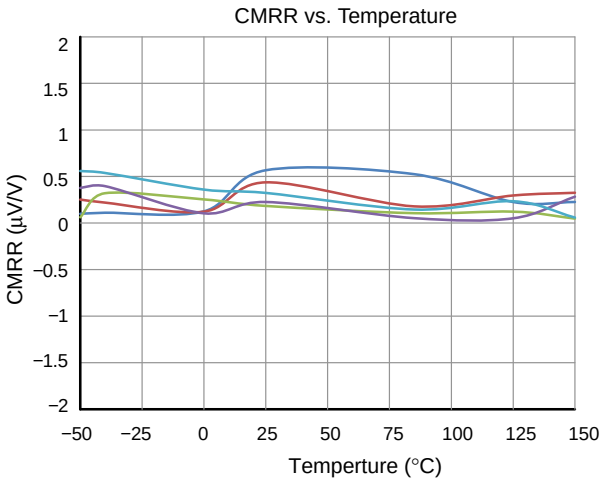


Figure 6. Common Mode Rejection Ratio vs Temperature, G100

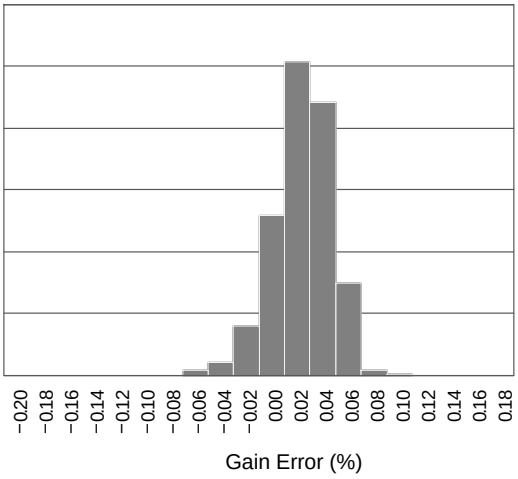


Figure 7a. Gain Error Distribution, G25

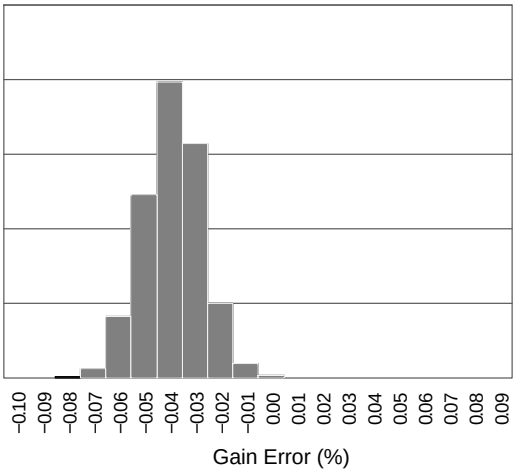


Figure 7b. Gain Error Distribution, G50

TYPICAL CHARACTERISTICS (At T_A = +25°C, V_{SENSE} = (V_{IN+}) – (V_{IN-}).; V_S = V_{EN} = 1.8 V, V_{REF} = V_S/2, V_{CM} =12 V, and all gains unless otherwise noted.) (continued)

IQ (μA)

Common Mode Voltage (V)

TYPICAL CHARACTERISTICS (At T_A = +25°C, V_{SENSE}


VIN (V)
Output (V)
Time (μs)

line that can overload the front end of any shunt current sensing IC.

This problem must be solved by filtering at the input of the amplifier. Note that all current sensing ICs are vulnerable to this problem, regardless of manufacturer claims. Filtering is required at the input of the device to resolve this problem, even if the spike frequencies are above the rated bandwidth of the device.

Ideally, select the capacitor to exactly match the time constant of the shunt resistor and its inductance; alternatively, select the capacitor to provide a pole below that point. Make the input filter time constant equal to or larger than the shunt and its inductance time constant:

$$\frac{L_{SHUNT}}{R_{SHUNT}} \leq R_{FILT}C_{FILT} \quad \text{(eq. 2)}$$

Selecting the Shunt Resistor

The desired accuracy of the current measurement determines the precision, shunt size, and the resistor value. The larger the resistor value, the more accurate the measurement possible, but a large resistor value also results in greater current loss.

For the most accurate measurements, use four terminal current sense resistors. It provides two terminals for the current path in the application circuit, and a second pair for the voltage detection path of the sense amplifier. This technique is also known as . This ensures that the voltage measured by the sense amplifier is the actual voltage across the resistor and does not include the small resistance of a combined connection. When using non−Kelvin shunts, follow manufacturer recommendations on how to lay out the sensing traces closely.

Gain Options

The gain is set by integrated, precision, ratio−matched resistors. The NCS21671 is available in gain options of 25 V/V, 50 V/V, 100 V/V, and 200 V/V. Adding external resistors to adjust the gain can contribute to the overall system error and is not recommended.

$$P_D \approx V_{in}(I_{GND}@I_{out}) + I_{out}(V_{in} - V_{out}) \quad \text{(eq. 3)}$$

$$V_{in(MAX)} \approx \frac{P_{D(MAX)} + (V_{out} \cdot I_{out})}{I_{out} + I_{GND}} \quad \text{(eq. 4)}$$

ORDERING INFORMATION

Device	Channels	Package	Gain	OPN	Marking	Shipping†

INDUSTRIAL AND CONSUMER

Package	GAIN	Enable	Filter Pins	Part Number	Marking	Shipping
SC70−6	25	No	No	NCS21671SQ025T2G	AAC(M)	Tape and Reel 3000 / Reel
	50			NCS21671SQ050T2G	\A/(YW)	
	100			NCS21671SQ100T2G	\A/(YW)	
	200			NCS21671SQ200T2G	R(YW)	
Micro10	25	Yes	Yes	NCS21671DM025R2G	G025	Tape and Reel 4000 / Reel
	50			NCS21671DM050R2G	G050	
	100			NCS21671DM100R2G	G100	
	200			NCS21671DM200R2G	G200	

AUTOMOTIVE GRADE1 QUALIFIED

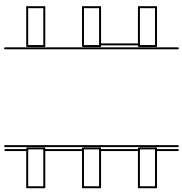
Package	GAIN	Enable	Filter Pins	Part Number	Marking	Shipping
SC70−6	25	No	No	NCV21671SQ025T2G	AAC(M)	Tape and Reel 3000 / Reel
	50			NCV21671SQ050T2G	\A/(YW)	
	100			NCV21671SQ100T2G	\A/(YW)	
	200			NCV21671SQ200T2G	R(YW)	
Micro10	25	Yes	Yes	NCV21671DM025R2G	G025	Tape and Reel 4000 / Reel
	50			NCV21671DM050R2G	G050	
	100			NCV21671DM100R2G	G100	
	200			NCV21671DM200R2G	G200	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

PACKAGE DIMENSIONS

SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

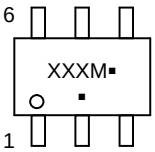
STYLE 4:
PIN 1. CATHODE

SC−88 2.00x1.25x0.90, 0.65P
CASE 419B−02
ISSUE Z

DATE 18 APR 2024

_ BURRS. MOLD FLASH,
PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

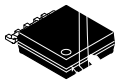
RECOMMENDED MOUNTING

STYLES ON PAGE 2

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED



SCALE 2:1

Micro10
CASE 846B
ISSUE D

DATE 07 DEC 2004

0.08 (0.003) M B S A S