PIN FUNCTION DESCRIPTION

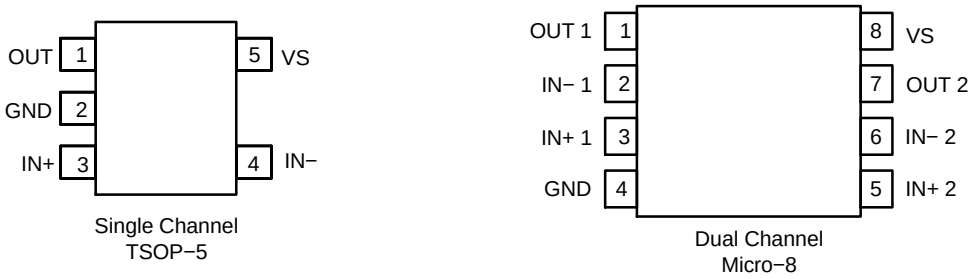


Figure 2. Pin Function Description

PIN DESCRIPTION

Pin Name	Type	Description
IN+	Input	This pin is connected to the positive side of the sense resistor or current shunt.
IN−	Input	This pin is connected to the negative side of the sense resistor or current shunt.
OUT	Output	The output pin provides a low impedance voltage output.
V_S	Supply	This is the positive supply pin that provides power to the internal circuitry. An external bypass capacitor of 0.1 F is recommended to be placed as close as possible to this pin.
GND	Supply	This is the negative supply rail of the circuit.

MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Supply Voltage (Note 1)		V_S	−0.3 to 5.5	V
Analog Inputs	Differential (V_{IN+})−($V_{IN−}$) (Note 2)	V_{IN+}, $V_{IN−}$	42	Analog Inputs
	Common−Mode (Note 2)		−0.3 to +42	
Output		V_{OUT}	GND−0.3 to (V_S) +0.3	V
Maximum Output Current		I_{OUT}	8	mA
Input Current into Any Pin		I_{IN}	10	mA
Maximum Junction Temperature		$T_{J(max)}$	+150	C
Storage Temperature Range		T_{STG}	−65 to +150	C
ESD Capability, Human Body Model (Note 3)		HBM	2000	V
Charged Device Model (Note 3)		CDM	1000	V
Latch−up Current (Note 4)			100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for safe operating parameters.
2. Input voltage at any pin may exceed the voltage shown if current at that pin is limited to 10 mA
3. This device series incorporates ESD protection and is tested by the following methods: ESD Human Body Model tested per JEDEC standard JS−001−2017
   ESD Charged Device Model tested per JEDEC standard JS−002−2014
4. Latch−up Current tested per JEDEC standard: JESD78E

THERMAL CHARACTERISTICS

Parameter	Symbol	Package	Value	Unit
Thermal Resistance, Junction−to−Air (Notes 5, 6)	θ_{JA}	TSOP−5 / SOT23−5	208	C/W
		Micro8 / MSOP−8	162	

5. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for safe operating parameters
6. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate

ELECTRICAL CHARACTERISTICS (continued)
At T_A = +25 C, V_{SENSE} = (V_{IN+}) – (V_{IN-}); V_S = 5 V, V_{IN+} = 12 V, unless otherwise noted. **Boldface** limits apply over the specified temperature range, T_A = –40 C to 125 C unless otherwise noted, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT						
Gain	G	G 20	–	20	–	V/V
		G 50	–	50	–	
		G 100	–	100	–	
		G 200	–	200	–	
Gain Error		T_A = 25 C	–	0.1	–	%
		T_A = −40 C to +125 C	–	–	**±0.4**	
Gain Error vs Temperature		T_A = −40 C to +125 C	–	1.5	**±20**	ppm/ C
Nonlinearity Error			–	0.01	–	%
Maximum Capacitive Load	C_L	No sustained oscillation	–	1	–	nF
Settling Time to 1%			–	5	–	μs
VOLTAGE OUTPUT						
Output Voltage High, Swing from V_S Supply Rail	$V_S - V_{OH}$	V_S = 5.5 V R_L = 10 kΩ to GND, T_A = 25 C	–	0.02	–	V
		V_S = 5.5 V R_L = 10 k to GND, T_A				

TYPICAL CHARACTERISTICS (At T_A = +25 C, V_{SENSE} = (V_{IN+}) – (V_{IN-}), V_S = 5.0 V, V_{IN}+ = 12 V, and all gains unless otherwise noted.)

Figure 3a. Input Offset Voltage Distribution, G20

Figure 3b. Input Offset Voltage Distribution, G50

Figure 3c. Input Offset Voltage Distribution, G100

Figure 3d. Input Offset Voltage Distribution, G200

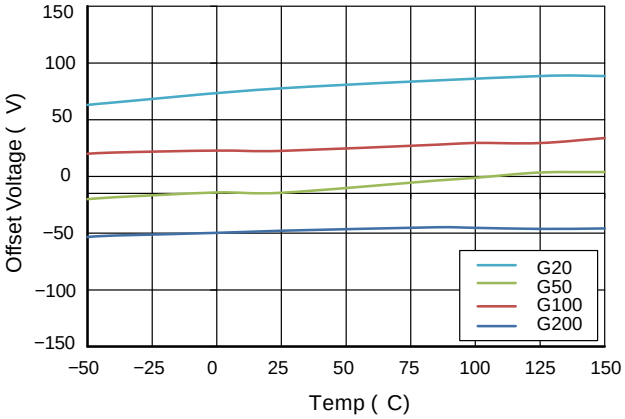


Figure 4. Input Offset vs. Temperature

Figure 5a. Common Mode Rejection Ratio Distribution, G20

TYPICAL CHARACTERISTICS (At T_A = +25 C, V_{SENSE} = (V_{IN+}) – (V_{IN-}), V_S = 5.0 V, V_{IN}+ = 12 V, and all gains unless otherwise noted.) (continued)

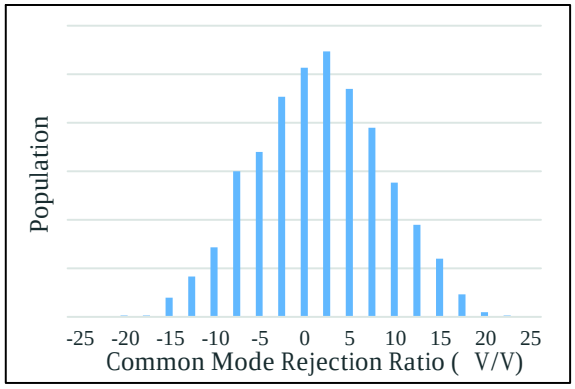


Figure 5b. Common Mode Rejection Ratio Distribution, G50

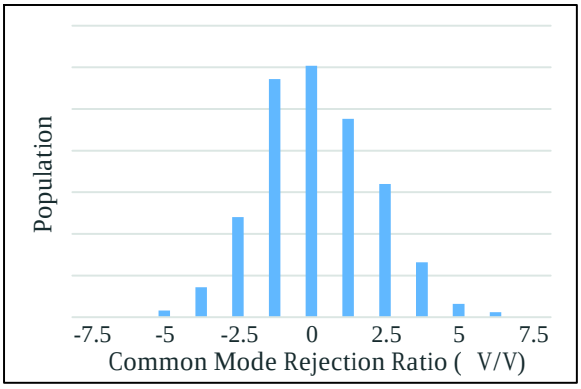


Figure 5c. Common Mode Rejection Ratio Distribution, G100

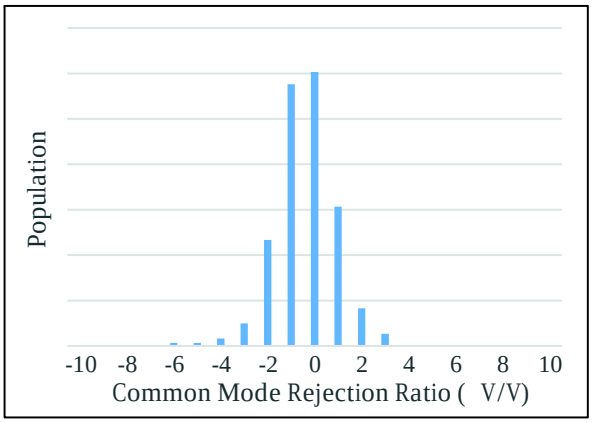


Figure 5d. Common Mode Rejection Ratio Distribution, G200

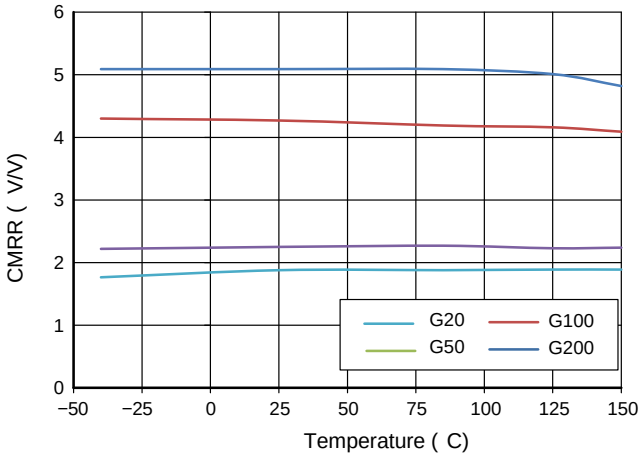


Figure 6. Common Mode Rejection Ratio vs Temperature

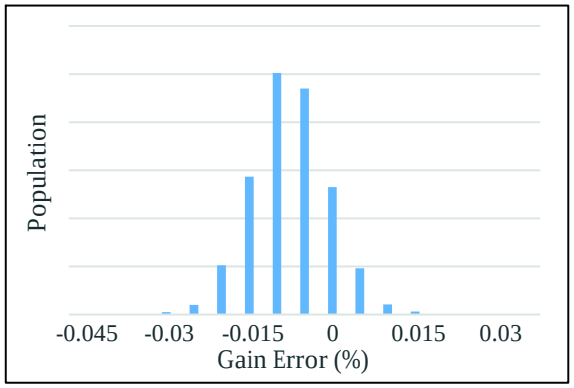


Figure 7a. Gain Error Distribution, G20

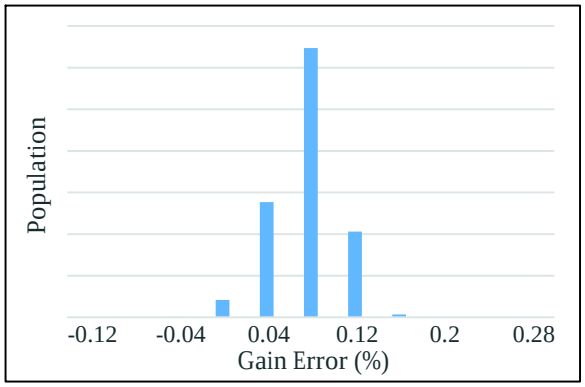
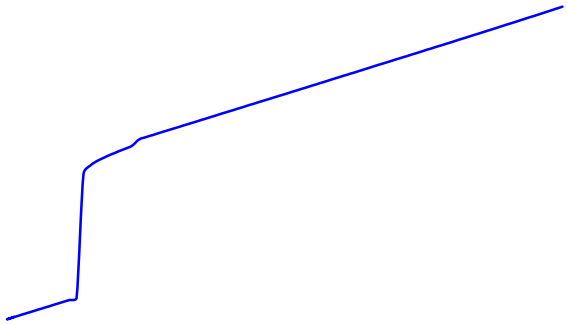


Figure 7b. Gain Error Distribution, G50

TYPICAL CHARACTERISTICS (At T_A = +25 C, V_{SENSE} = (V_{IN+}) – (V_{IN-}), V_S = 5.0 V, V_{IN}+ = 12 V, and all gains unless otherwise noted.) (continued)

TYPICAL CHARACTERISTICS (At T_A = +25 C, V_{SENSE} = (V_{IN+}) – (V_{IN-}), V_S = 5.0 V, V_{IN}+ = 12 V, and all gains unless otherwise noted.) (continued)



TYPICAL CHARACTERISTICS (At T_A = +25

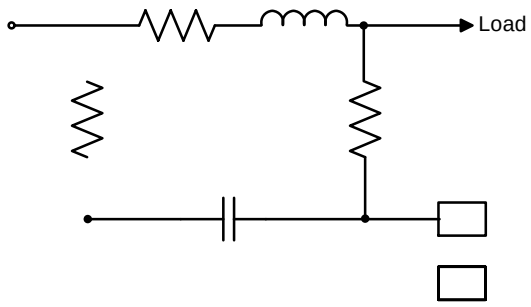
TYPICAL CHARACTERISTICS (At T_A = +25 C, V_{SENSE} = (V_{IN+}) – (V_{IN-}), V_S = 5.0 V, V_{IN}+ = 12 V, and all gains unless

APPLICATION INFORMATION

Current Sensing Techniques

Unidirectional Operation

Input Filtering



Ω

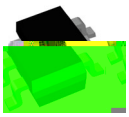
$$Vout = \frac{VIN\_(Rload)}{400K + (Rload)} \quad \text{(eq. 3)}$$

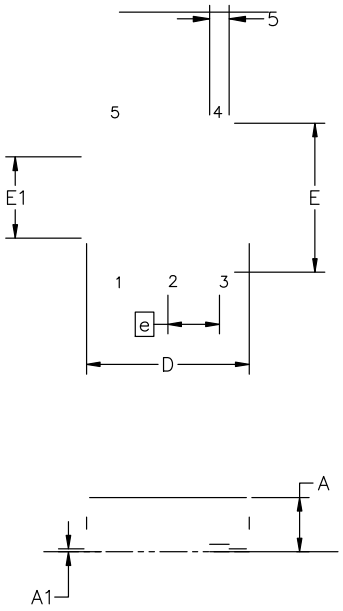
ORDERING INFORMATION

Device	Channels	Package	Gain	OPN	Marking	Shipping†
INDUSTRIAL AND CONSUMER						
NCS21673	Single	TSOP−5	20	NCS21673SN2G020T1G	AE2	Tape and Reel 3000 / Reel
			50	NCS21673SN2G050T1G**	AE3	
			100	NCS21673SN2G100T1G**	AE4	
			200	NCS21673SN2G200T1G**	AE5	
NCS21674	Dual	Micro8	20	NCS21674DMG020R2G**	G020	Tape and Reel 4000 / Reel
			50	NCS21674DMG050R2G	G050	
			100	NCS21674DMG100R2G	G100	
			200	NCS21674DMG200R2G	G200	
AUTOMOTIVE QUALIFIED						
NCV21673*	Single	TSOP−5	20	NCV21673SN2G020T1G	AE2	Tape and Reel 3000 / Reel
			50	NCV21673SN2G050T1G**	AE3	
			100	NCV21673SN2G100T1G**	AE4	
			200	NCV21673SN2G200T1G**	AE5	
NCV21674*	Dual	Micro8	20	NCV21674DMG020R2G**	G020	Tape and Reel 4000 / Reel
			50	NCV21674DMG050R2G	G050	
			100	NCV21674DMG100R2G	G100	
			200	NCV21674DMG200R2G	G200	

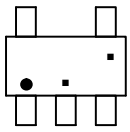
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
**In Development / Consult Sales

TSOP−5 3.00x1.50x0.95, 0.95P

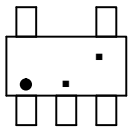




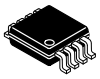
GENERIC
MARKING DIAGRAM*



Analog



Discrete/Logic



SCALE 2:1

Micro8
CASE 846A–02
ISSUE K

DATE 16 JUL 2020