## 750 MHz Voltage Feedback Op Amp with Fast Enable Feature

NCS2552 is a 750 MHz voltage feedback monolithic operational amplifier featuring high slew rate and low differential gain and phase error. The voltage feedback architecture allows for a superior bandwidth and low power consumption. This device features an enable pin.

### Features

3.0 dB Small Signal BW ( $A_V = +2.0$ ,  $V_O = 0.5 V_{p\ p}$ ) 750 MHz Typ Slew Rate 1700 V/µs Fast Enable Time 5.0 ns Supply Current 13 mA Input Referred Voltage Noise 5.0 nV/ $\sqrt{Hz}$ THD 64 dBc (f = 5.0 MHz,  $V_O = 2.0 V_{p\ p}$ ) Output Current 100 mA Pin Compatible with EL5157, AD8057 This is a Pb Free Device

### Applications

Line Drivers Radar/Communication Receivers





### PIN FUNCTION DESCRIPTION

Pin (SOT23/SC70)	Symbol	Function	Equivalent Circuit
1	OUT	Output	

### ATTRIBUTES

	Characteristics	Value	
ESD			

## AC ELECTRICAL CHARACTERISTICS ( $V_{CC}$ = +5.0 V, $V_{EE}$ = -5.0 V, $T_A$ = -40 C to +85 C, $R_L$ = 150 $\Omega$ to GND, $R_F$ = 150 $\Omega$ , $A_V$ = +2.0, Enable is left open, unless otherwise specified).

Symbol	Characteristic	Conditions	Min	Тур	Max	Unit
FREQUENC	CY DOMAIN PERFORMANCE					
BW	Bandwidth 3.0 dB Small Signal 3.0 dB Large Signal	$\begin{array}{l} A_V = +2.0, \ V_O = 0.5 \ V_{p-p} \\ A_V = +2.0, \ V_O = 2.0 \ V_{p-p} \end{array}$		750 350		MHz
GF <sub>0.1dB</sub>	0.1 dB Gain Flatness Bandwidth	A <sub>V</sub> = +2.0		40		MHz
dG	Differential Gain	$A_V$ = +2.0, $R_L$ = 150 $\Omega$ , f = 3.58 MHz		0.07		%
dP	Differential Phase	$A_V = +2.0$ , $R_L = 150 \Omega$ , $f = 3.58 MHz$		0.01		
TIME DOM	AIN RESPONSE					
SR	Slew Rate	$A_V = +2.0, V_{step} = 2.0 V$		1700		V/µs
t <sub>s</sub>	Settling Time 0.1%	A <sub>V</sub> = +2.0, V <sub>step</sub> = 2.0 V		10		ns
t <sub>r</sub> t <sub>f</sub>	Rise and Fall Time	(10%–90%) $A_V$ = +2.0, $V_{step}$ = 2.0 V		2.0		ns
t <sub>ON</sub>	Turn-on Time			5.0		ns
t <sub>OFF</sub>	Turn-off Time			15		ns
HARMONIC	/NOISE PERFORMANCE					
THD	Total Harmonic Distortion	f = 5.0 MHz, $V_{O}$ = 2.0 $V_{p-p}$		-64		dB
HD2	2nd Harmonic Distortion	f = 5.0 MHz, $V_{O}$ = 2.0 $V_{p-p}$		-65		dBc
HD3	3rd Harmonic Distortion	f = 5.0 MHz, $V_{O}$ = 2.0 $V_{p-p}$		-75		dBc
IP3	Third–Order Intercept	$f = 10 \text{ MHz}, V_O = 1.0 \text{ V}_{p-p}$		40		dBm
SFDR	Spurious–Free Dynamic Range	f = 5.0 MHz, $V_{O}$ = 2.0 $V_{p-p}$		55		dBc
e <sub>N</sub>	Input Referred Voltage Noise	f = 1.0 MHz		5.0		$nV/\sqrt{Hz}$
i <sub>N</sub>	Input Referred Current Noise	f = 1.0 MHz		4.0		pA/ <del>√Hz</del>

-

# AC ELECTRICAL CHARACTERISTICS ( $V_{CC}$ = +2.5 V, $V_{EE}$ = -2.5 V, $T_A$ = -40 C to +85 C, $R_L$ = 150 $\Omega$ to GND, $R_F$ = 150 $\Omega$ , $A_V$ = +2.0, Enable is left open, unless otherwise specified).

Symbol	Characteristic	Characteristic Conditions N		Тур	Max	Unit					
FREQUENCY DOMAIN PERFORMANCE											
BW	Bandwidth 3.0 dB Small Signal 3.0 dB Large Signal	$A_V$ = +2.0, $V_O$ = 0.5 $V_{p-p}$ $A_V$ = +2.0, $V_O$ = 1.0 $V_{p-p}$		550 200		MHz					
GF <sub>0.1dB</sub>	0.1 dB Gain Flatness Bandwidth	$A_{\rm V} = +2.0$		35		MHz					
dG	Differential Gain	$A_V$ = +2.0, $R_L$ = 150 $\Omega$ , f = 3.58 MHz		0.07		%					
dP	Differential Phase	$A_V$ = +2.0, $R_L$ = 150 $\Omega$ , f = 3.58 MHz		0.02							

TIME DOMAIN RESPONSE

SR	Slew Rate	$A_V = +2.0, V_{step} = 1.0 V$	900	V/µs
t <sub>s</sub>	Settling Time 0.1%	A <sub>V</sub> = +2.0, V <sub>step</sub> = 1.0 V	10	ns
t <sub>r</sub> t <sub>f</sub>	Rise and Fall Time	(10%–90%) $A_V$ = +2.0, $V_{step}$ = 1.0 V	1.7	ns
t <sub>ON</sub>	Turn-on Time		5.0	ns
t <sub>OFF</sub>	Turn-off Time		15	ns

HARMONIC/NOISE PERFORMANCE

THD	Total Harmonic Distortion	f = 5.0 MHz, $V_0$ = 1.0 $V_{p-p}$	-60	dB
HD2	2nd Harmonic Distortion	f = 5.0 MHz, $V_0$ = 1.0 $V_{p-p}$	-65	dBc
HD3	3rd Harmonic Distortion	f = 5.0 MHz, $V_0$ = 1.0 $V_{p-p}$	-63	dBc
IP3	Third–Order Intercept	$f = 10 \text{ MHz}, \text{ V}_{O} = 0.5 \text{ V}_{p-p}$	35	dBm
SFDR	Spurious–Free Dynamic Range	f = 5.0 MHz, $V_0$ = 1.0 $V_{p-p}$	63	dBc

е

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = +2.5 V, V<sub>EE</sub> = -2.5 V, T<sub>A</sub> = -40 C to +85 C, R<sub>L</sub> = 150 $\Omega$ to GND, R<sub>F</sub> = 150 $\Omega$ , A<sub>V</sub> = +2.0, Enable is left open, unless otherwise specified).

Symbol	Characteristic	Conditions	Min	Тур	Max	Unit
DC PERFO	RMANCE					
V <sub>IO</sub>	Input Offset Voltage		-10	0	+10	mV
$\Delta V_{IO} / \Delta T$	Input Offset Voltage Temperature Coefficient			6.0		μV/ C
I <sub>IB</sub>	Input Bias Current	$V_{O} = 0 V$		± 3.2	±20	μΑ
$\Delta I_{IB} / \Delta T$	Input Bias Current Temperature Coefficient	V <sub>O</sub> = 0 V		± 40		nA/ C
V <sub>IH</sub>	Input High Voltage (Enable) (Note 3)		1.5			V
V <sub>IL</sub>	Input Low Voltage (Enable) (Note 3)				0.5	V
INPUT CHA	ARACTERISTICS					
V <sub>CM</sub>	Input Common Mode Voltage Range (Note 3)		± 1.1	±1.6		V
CMRR	Common Mode Rejection Ratio	(See Graph)	40	50		dB
R <sub>IN</sub>	Input Resistance			4.5		MΩ
C <sub>IN</sub>	Differential Input Capacitance			1.0		pF
OUTPUT C	HARACTERISTICS		•	•	•	•
R <sub>OUT</sub>	Output Resistance	Closed Loop Open Loop		0.1 13		Ω
Vo	Output Voltage Range		± 1.1	±1.6		V
Ι <sub>Ο</sub>	Output Current		±50	±100		mA
POWER SU	JPPLY					
Vs	Operating Voltage Supply			5.0		V
1	Device Currely Current		5.0	44.5	47	A

I <sub>S,ON</sub>	Power Supply Current – Enabled		5.0	11.5	17	mA
I <sub>S,OFF</sub>	Power Supply Current – Disabled			0.5	0.8	mA
PSRR	Power Supply Rejection Ratio	(See Graph)	40	56		dB

4. Guaranteed by design and/or characterization.

Figure 5. Frequency Response:







http://onsemi.com 18II.674129m3818Im.6741m8I3812. 97741m8I3812. m.67414829812. 977*4*II **43/298.120/**m.67416348292288I741634829228m.674172I38292288I74196348292288I7528I382

NCS2552



Figure 23. Turn ON Time Delay Vertical: 500 mV/div (Enable), 200 mV/div (Output) Horizontal: 5 ns/div



Figure 24. Turn OFF Time Delay Vertical: 500 mV/div (Enable), 200 mV/div (Output) Horizontal: 5 ns/div

### Printed Circuit Board Layout Techniques

Proper high speed PCB design rules should be used for all wideband amplifiers as the PCB parasitics can affect the overall performance. Most important are stray capacitances at the output and inverting input nodes as it can effect peaking and bandwidth. A space (3/16 is plenty) should be left around the signal lines to minimize coupling. Also, signal lines connecting the feedback and gain resistors should be short enough so that their associated inductance does not cause high frequency gain errors. Line lengths less than 1/4 are recommended.

### Video Performance

This device designed to provide good performance with NTSC, PAL, and HDTV video signals. Best performance is obtained with back terminated loads as performance is degraded as the load is increased. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage.

### ESD Protection

All device pins have limited ESD protection using internal diodes to power supplies as specified in the attributes table (see Figure 25). These diodes provide moderate protection

to input overdrive voltages above the supplies. The ESD diodes can support high input currents with current limiting series resistors. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response. Under closed loop operation, the ESD diodes have no effect on circuit performance. However, under certain conditions the ESD diodes will be evident. If the device is driven into a slewing condition, the ESD diodes will clamp large differential voltages until the feedback loop restores closed loop operation. Also, if the device is powered down and a large input signal is applied, the ESD diodes will conduct.

NOTE: Human Body Model for +IN and –IN pins are rated at 0.8kV while all other pins are rated at 2.0kV.



Figure 25. Internal ESD Protection

#### ORDERING INFORMATION



#### TSOP-6 3.00x1.50x0.90, 0.95P CASE 318G ISSUE W

DATE 26 FEB 2024

NDTES: 1. DIMENSIONING AND TOLERAN

#### TSOP-6 3.00x1.50x0.90, 0.95P CASE 318G ISSUE W

### DATE 26 FEB 2024

### GENERIC **MARKING DIAGRAM\***





XXX = Specific Device Code A =Assembly Location

Y = Year

W = Work Week

= Pb-Free Package •

STYLE 1:	STYLE 2:	STYLE 3:	STYLE 4:	STYLE 5:	STYLE 6:
PIN 1. DRAIN	PIN 1. EMITTER 2	PIN 1. ENABLE	PIN 1. N/C	PIN 1. EMITTER 2	PIN 1. COLLECTOR
2. DRAIN	2. BASE 1	2. N/C	2. V in	2. BASE 2	2. COLLECTOR
3. GATE	3. COLLECTOR 1	3. R BOOST	3. NOT USED	3. COLLECTOR 1	3. BASE
4. SOURCE	4. EMITTER 1	4. Vz	4. GROUND	4. EMITTER 1	4. EMITTER
5. DRAIN	5. BASE 2	5. V in	5. ENABLE	5. BASE 1	5. COLLECTOR
6. DRAIN	6. COLLECTOR 2	6. V out	6. LOAD	6. COLLECTOR 2	6. COLLECTOR
STYLE 7:	STYLE 8:	STYLE 9:	STYLE 10:	STYLE 11:	STYLE 12:
PIN 1. COLLECTOR	PIN 1. Vbus	PIN 1. LOW VOLTAGE GATE	PIN 1. D(OUT)+	PIN 1. SOURCE 1	PIN 1. I/O
2. COLLECTOR	2. D(in)	2. DRAIN	2. GND	2. DRAIN 2	2. GROUND
3. BASE	3. D(in)+	3. SOURCE	3. D(OUT)-	3. DRAIN 2	3. I/O
4. N/C	4. D(out)+	4. DRAIN	4. D(IN)-	4. SOURCE 2	4. I/O
5. COLLECTOR	5. D(out)	5. DRAIN	5. VBUS	5. GATE 1	5. VCC
6. EMITTER	6. GND	6. HIGH VOLTAGE GATE	6. D(IN)+	6. DRAIN 1/GATE 2	6. I/O

onsemi, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries. onsemi owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of onsemi's product/patent coverage may be accessed at <a href="http://www.onsemi.com/site/pdf/Patent-Marking.pdf">www.onsemi.com/site/pdf/Patent-Marking.pdf</a>. Onsemi reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and onsemi makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or incruit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using onsemi