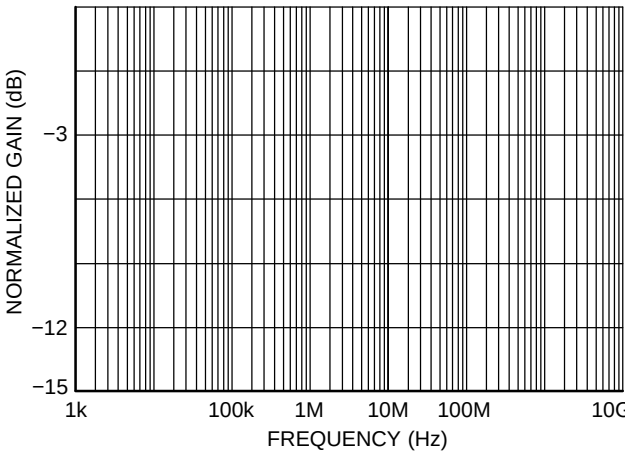
NCS2552

750 MHz Voltage Feedback Op Amp with Fast Enable Feature

NCS2552 is a 750 MHz voltage feedback monolithic operational amplifier featuring high slew rate and low differential gain and phase error. The voltage feedback architecture allows for a superior bandwidth and low power consumption. This device features an enable pin.

- ǐ3.0 dB Small Signal BW (A_V = +2.0, V_O = 0.5 $V_{pǐp}$) 750 MHz Typ
- Slew Rate 1700 V/μs
- Fast Enable Time 5.0 ns
- Supply Current 13 mA
- Input Referred Voltage Noise 5.0 nV/$\sqrt{Hz}$
- THD ǐ64 dBc (f = 5.0 MHz, V_O = 2.0 $V_{pǐp}$)
- Output Current 100 mA
- Pin Compatible with EL5157, AD8057
- This is a PbǐFree Device

- Line Drivers
- Radar/Communication Receivers



1	OUT	Output	


ESD

(V_{CC} = +5.0 V, V_{EE} = −5.0 V, T_A = −40 C to +85 C, R_L = 150 Ω to GND, R_F = 150 Ω, A_V = +2.0, Enable is left open, unless otherwise specified).

BW	Bandwidth 3.0 dB Small Signal 3.0 dB Large Signal	 A_V = +2.0, V_O = 0.5 V_{p-p} A_V = +2.0, V_O = 2.0 V_{p-p}		 750 350		MHz
$GF_{0.1dB}$	0.1 dB Gain Flatness Bandwidth	A_V = +2.0		40		MHz
dG	Differential Gain	A_V = +2.0, R_L = 150 Ω, f = 3.58 MHz		0.07		%
dP	Differential Phase	A_V = +2.0, R_L = 150 Ω, f = 3.58 MHz		0.01		
SR	Slew Rate	A_V = +2.0, V_{step} = 2.0 V		1700		V/μs
t_s	Settling Time 0.1%	 A_V = +2.0, V_{step} = 2.0 V		 10		ns
t_r t_f	Rise and Fall Time	(10%−90%) A_V = +2.0, V_{step} = 2.0 V		2.0		ns
t_{ON}	Turn−on Time			5.0		ns
t_{OFF}	Turn−off Time			15		ns
THD	Total Harmonic Distortion	f = 5.0 MHz, V_O = 2.0 V_{p-p}		−64		dB
HD2	2nd Harmonic Distortion	f = 5.0 MHz, V_O = 2.0 V_{p-p}		−65		dBc
HD3	3rd Harmonic Distortion	f = 5.0 MHz, V_O = 2.0 V_{p-p}		−75		dBc
IP3	Third−Order Intercept	f = 10 MHz, V_O = 1.0 V_{p-p}		40		dBm
SFDR	Spurious−Free Dynamic Range	f = 5.0 MHz, V_O = 2.0 V_{p-p}		55		dBc
e_N	Input Referred Voltage Noise	f = 1.0 MHz		5.0		$nV/\sqrt{Hz}$
i_N	Input Referred Current Noise	f = 1.0 MHz		4.0		$pA/\sqrt{Hz}$

(V_{CC} = +2.5 V, V_{EE} = −2.5 V, T_A = −40 C to +85 C, R_L = 150 Ω to GND, R_F = 150 Ω, A_V = +2.0, Enable is left open, unless otherwise specified).

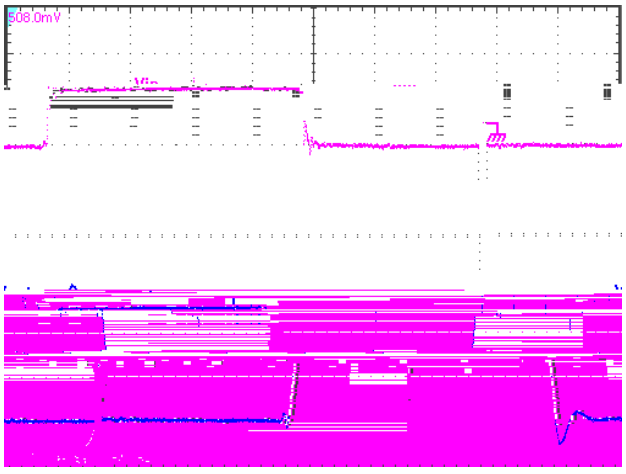
BW	Bandwidth 3.0 dB Small Signal 3.0 dB Large Signal	 A_V = +2.0, V_O = 0.5 V_{p-p} A_V = +2.0, V_O = 1.0 V_{p-p}		 550 200		MHz
$GF_{0.1dB}$	0.1 dB Gain Flatness Bandwidth	A_V = +2.0		35		MHz
dG	Differential Gain	A_V = +2.0, R_L = 150 Ω, f = 3.58 MHz		0.07		%
dP	Differential Phase	A_V = +2.0, R_L = 150 Ω, f = 3.58 MHz		0.02		
SR	Slew Rate	A_V = +2.0, V_{step} = 1.0 V		900		V/μs
t_s	Settling Time 0.1%	 A_V = +2.0, V_{step} = 1.0 V		 10		ns
t_r t_f	Rise and Fall Time	(10%−90%) A_V = +2.0, V_{step} = 1.0 V		1.7		ns
t_{ON}	Turn−on Time			5.0		ns
t_{OFF}	Turn−off Time			15		ns
THD	Total Harmonic Distortion	f = 5.0 MHz, V_O = 1.0 V_{p-p}		−60		dB
HD2	2nd Harmonic Distortion	f = 5.0 MHz, V_O = 1.0 V_{p-p}		−65		dBc
HD3	3rd Harmonic Distortion	f = 5.0 MHz, V_O = 1.0 V_{p-p}		−63		dBc
IP3	Third−Order Intercept	f = 10 MHz, V_O = 0.5 V_{p-p}		35		dBm
SFDR	Spurious−Free Dynamic Range	f = 5.0 MHz, V_O = 1.0 V_{p-p}		63		dBc

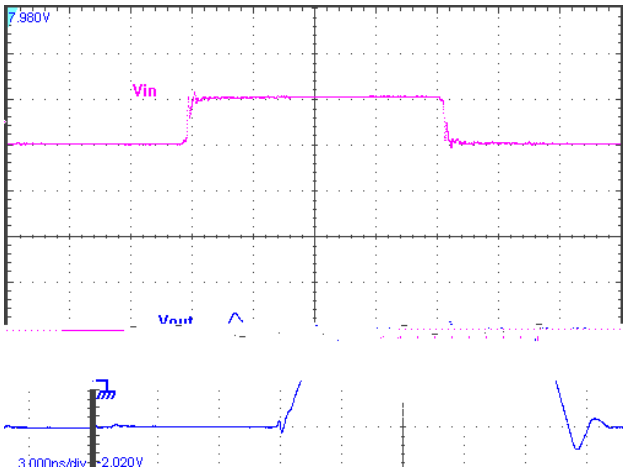
e

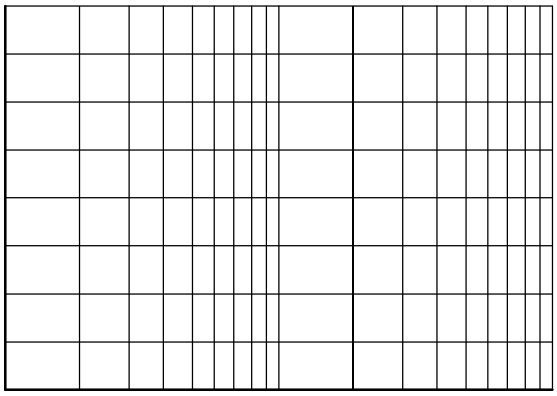
(V_{CC} = +2.5 V, V_{EE} = −2.5 V, T_A = −40 C to +85 C, R_L = 150 Ω to GND, R_F = 150 Ω, A_V = +2.0, Enable is left open, unless otherwise specified).

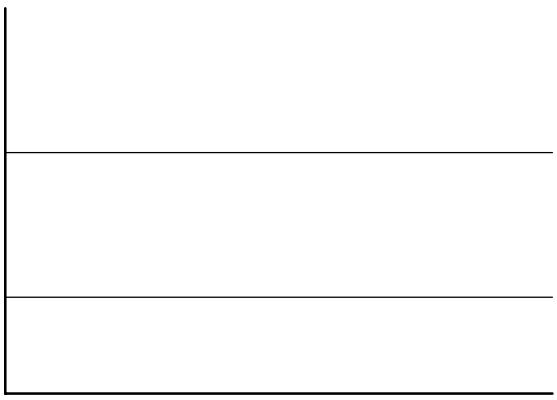
V_{IO}	Input Offset Voltage		−10	0	+10	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Coefficient			6.0		μV/ C
I_{IB}	Input Bias Current	V_O = 0 V		±3.2	±20	μA
$\Delta I_{IB}/\Delta T$	Input Bias Current Temperature Coefficient	V_O = 0 V		±40		nA/ C
V_{IH}	Input High Voltage (Enable) (Note 3)		1.5			V
V_{IL}	Input Low Voltage (Enable) (Note 3)				0.5	V
V_{CM}	Input Common Mode Voltage Range (Note 3)		±1.1	±1.6		V
CMRR	Common Mode Rejection Ratio	(See Graph)	40	50		dB
R_{IN}	Input Resistance			4.5		MΩ
C_{IN}	Differential Input Capacitance			1.0		pF
R_{OUT}	Output Resistance	Closed Loop Open Loop		0.1 13		Ω
V_O	Output Voltage Range		±1.1	±1.6		V
I_O	Output Current		±50	±100		mA
V_S	Operating Voltage Supply			5.0		V
$I_{S,ON}$	Power Supply Current − Enabled		5.0	11.5	17	mA
$I_{S,OFF}$	Power Supply Current − Disabled			0.5	0.8	mA
PSRR	Power Supply Rejection Ratio	(See Graph)	40	56		dB

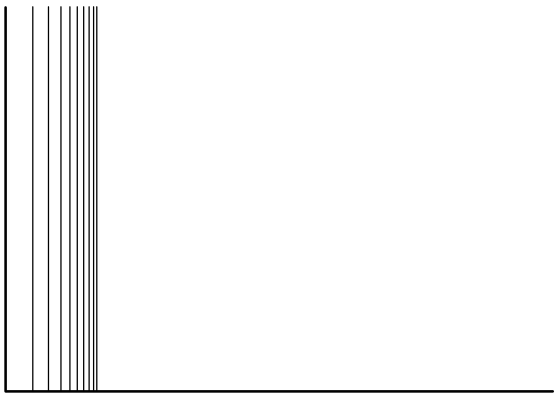
4. Guaranteed by design and/or characterization.

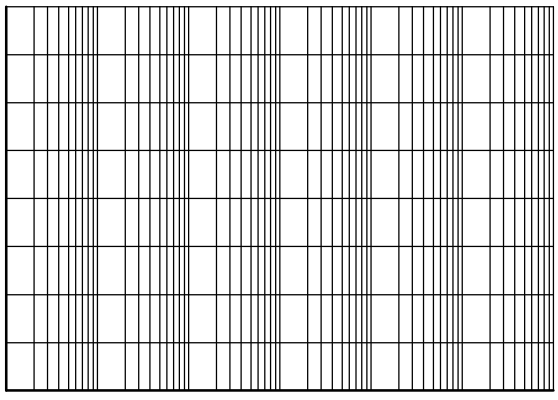

508.0mV

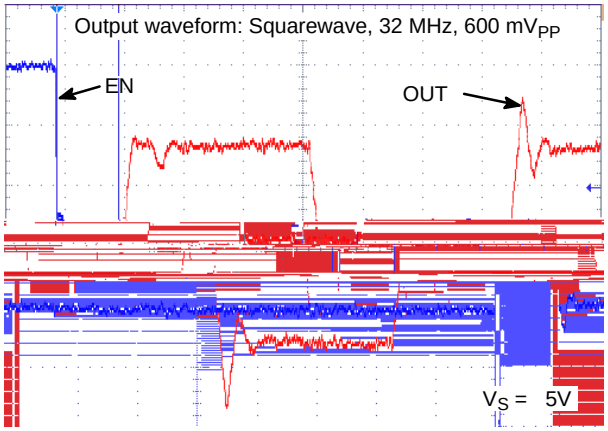

7.980V
Vin
Vout
3.000ns/div
2.020V

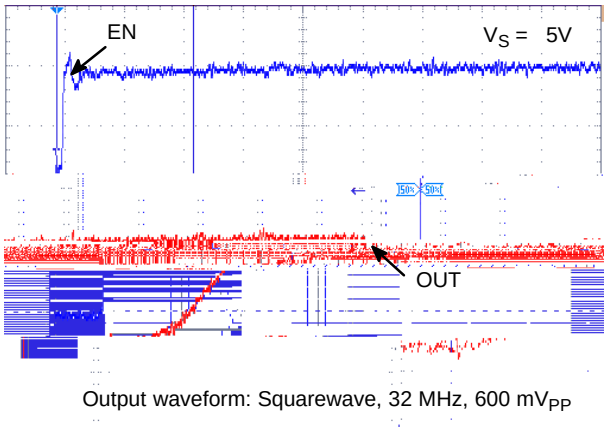












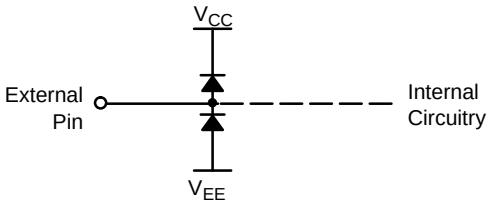
Output waveform: Squarewave, 32 MHz, 600 mV_{PP}

Proper high speed PCB design rules should be used for all wideband amplifiers as the PCB parasitics can affect the overall performance. Most important are stray capacitances at the output and inverting input nodes as it can effect peaking and bandwidth. A space (3/16 is plenty) should be left around the signal lines to minimize coupling. Also, signal lines connecting the feedback and gain resistors should be short enough so that their associated inductance does not cause high frequency gain errors. Line lengths less than 1/4 are recommended.

This device designed to provide good performance with NTSC, PAL, and HDTV video signals. Best performance is obtained with back terminated loads as performance is degraded as the load is increased. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage.

All device pins have limited ESD protection using internal diodes to power supplies as specified in the attributes table (see Figure 25). These diodes provide moderate protection to input overdrive voltages above the supplies. The ESD diodes can support high input currents with current limiting series resistors. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response. Under closed ĭ loop operation, the ESD diodes have no effect on circuit performance. However, under certain conditions the ESD diodes will be evident. If the device is driven into a slewing condition, the ESD diodes will clamp large differential voltages until the feedback loop restores closed ĭ loop operation. Also, if the device is powered down and a large input signal is applied, the ESD diodes will conduct.

NOTE: Human Body Model for +IN and –IN pins are rated at 0.8kV while all other pins are rated at 2.0kV.



TSOP−6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

DATE 26 FEB 2024

NOTES:
1. DIMENSIONING AND TOLERAN

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ISSUE W

DATE 26 FEB 2024

GENERIC
MARKING DIAGRAM*

XXX = Specific Device Code
A =Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O