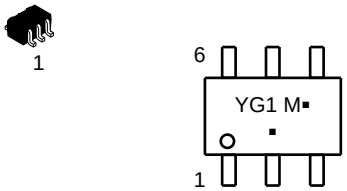
Video Amplifier, 1-Channel, With Reconstruction Filter and SAG Correction

The NCS2561 is a single high speed video driver including a 2−pole reconstruction filter and SAG correction capability. The NCS2561 is available in a space saving SC−88 package optimized for low voltage, portable applications. It is designed to be compatible with Digital−to−Analog Converters (DAC) embedded in most video processors.

The NCS2561 internally integrates an 8 MHz 2−pole video DAC reconstruction filter with a fixed gain of 2. The NCS2561 also has a built−in SAG correction circuit when used at the output in an AC −coupled mode. To further reduce power consumption, an enable pin is provided.



(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

Features

- Internal 8 MHz 2−Pole Reconstruction Filter
- Internal Fixed Gain: 6 dB
- Integrated Level Shifter
- SAG Correction Circuit for Reducing Coupling Capacitor Size
- Low Quiescent Current: 6 mA Typ
- Shutdown Current < 5 □A
- Wide Input Voltage Range
- Capability to Drive 2 CVBS Video Signals Together (2x150 1 j 1 J 0 0 m-27.326 0 lSQq1 0 0 1 123.021 182.893 cm0.964 w 1 j 1 J 0 0

Related Resource:
Refer to Application Note AND8457/D for details

August, 2018 − Rev. 4
Publication Order Number:
NCS2561/D

PIN FUNCTION AND DESCRIPTION

Pin	Name	Type	Description
1	IN	Input	Video Input
2	GND	Ground	Ground
3	SAG	Output	Sag Compensation
4	OUT	Output	Video Output

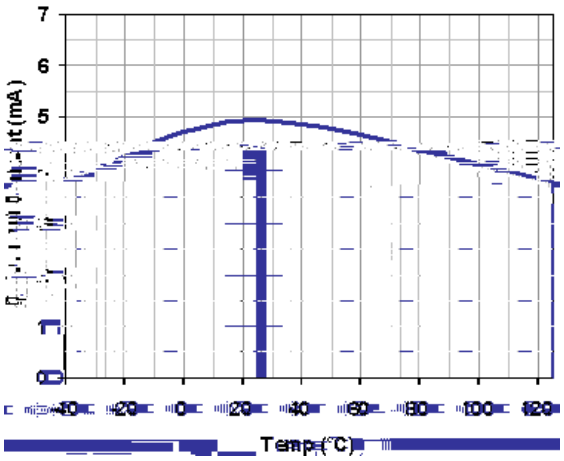


Figure 8. Quiescent Current vs. Temperature (V_{CC} = 3.0 V)

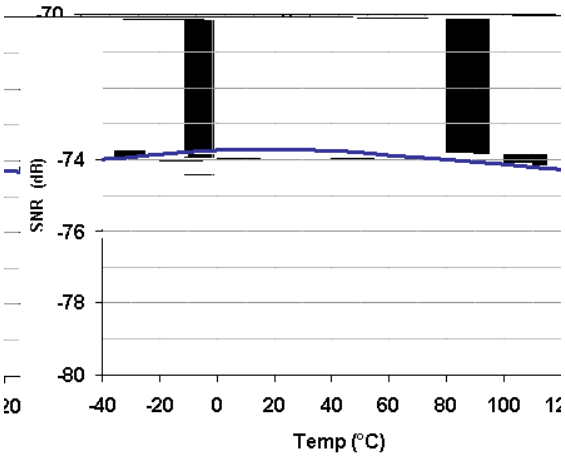
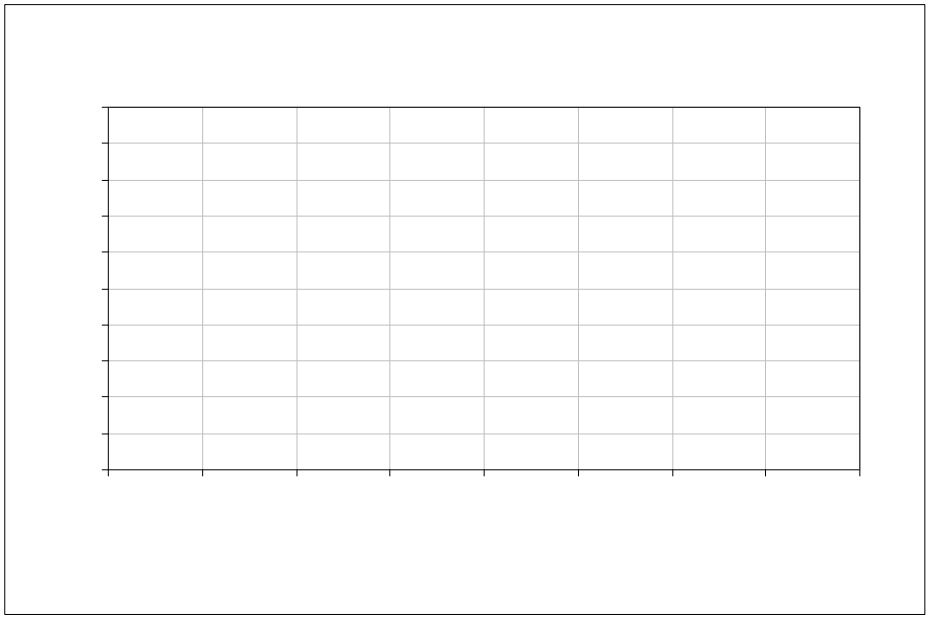


Figure 9. Signal−to−Noise Ratio vs. Temperature

Sag Correction

Video drivers that do not incorporate sag compensation traditionally recommend a large coupling capacitor (220 □F) on the output of the video driver. Larger output coupling capacitors (≥ 470 □F) are often chosen by design engineers when the application allows this (Set−Top Box). A larger output coupling capacitor allows a lower cut−off frequency to avoid field tilt effects; however in portable applications there is a trade−off between large and expensive coupling capacitors, and a coupling configuration to saving space. The sag compensation circuitry allows the reduction of this output coupling capacitor value by inducing peaking at the lower cutoff frequency of the high pass filter. The high−pass filter is created by the coupling capacitor and the load resistor (1/(2□R_LCout), and this peaking lowers the cutoff frequency. Simulation results provided in Figure 11 show the effect of the sag compensation at the low cut−off frequency.



The Csag value has no significant impact on the coupling even as the value increases. A value of 22 □F is recommended for optimal performance.

To achieve similar behavior to an output coupling capacitor value Cout = 220 □F (no sag) the nominal equivalent sag combination is Csag = 22 □F and Cout = 67□□F. A value of 47□□F for Cout will yield equivalent results. If we consider a coupling cap of 470 □F, the best compromise for sag combination is Csag = 22 □F and Cout = 100 □F. A value of 67□□F for Cout will yield equivalent results.

Figures 13 and 14 show the impact of the output coupling capacitor on a video signal corresponding to a worst case situation regarding the low frequency bandwidth. The video signal used is a 50 Hz 1/2 black − 1/2 white video pattern. This signal is obtained using the PAL Flat Field Square wave signal option available with the video generator TG700 from Tektronix. These measurements show how the sag function can help to reduce the field tilt problem using lower value coupling capacitor than traditional approach.

Figure 13. No sag, Cout = 220 μF
(Top : Input, Bottom : Output)

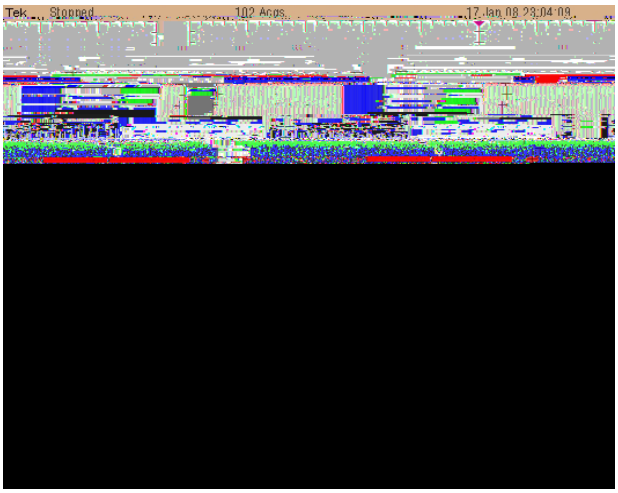


Figure 14. Csag = 22 μF, Cout = 47 μF
(Top : Input, Bottom : Output)

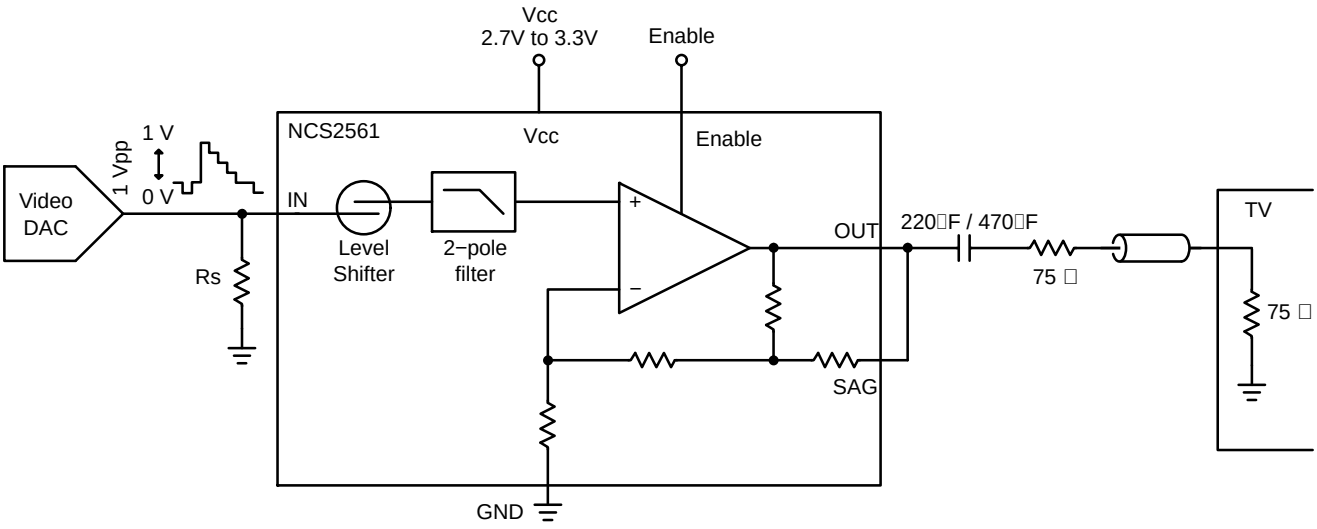


Figure 15. NCS2561 in an AC−Coupled Configuration with no sag

DC−Coupled Output

Having efficient output AC−coupled capability thanks to the sag correction option, with the built−in level shifter, the NCS2561 can also be DC−coupled to a 150 □ load. This has the advantage of eliminating the AC−coupling capacitors at

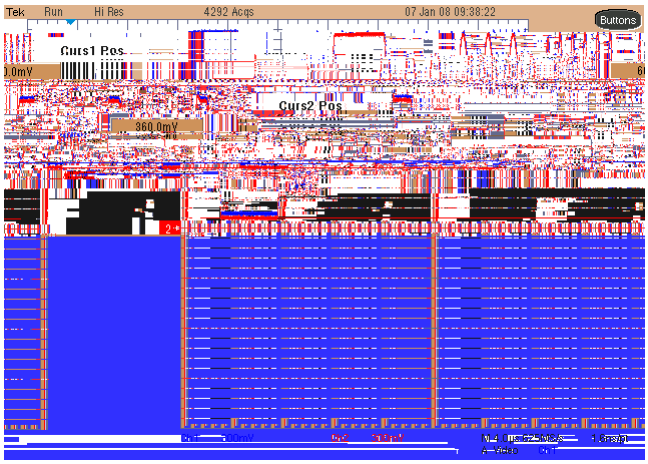


Figure 18. Multiburst Test with two 150 Ω loads

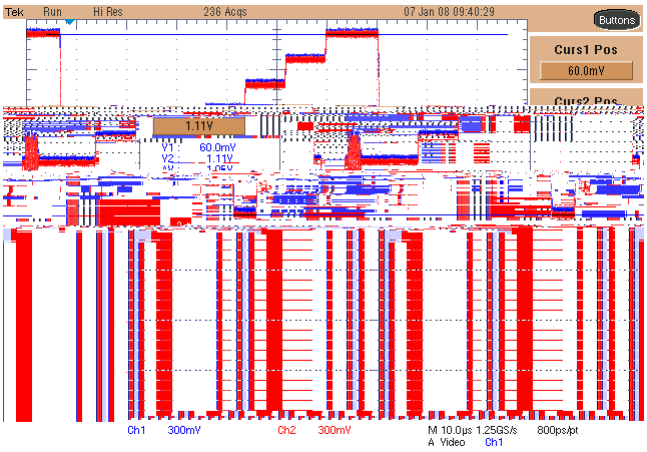


Figure 19. Linearity Test with two 150 Ω loads

ESD Protection

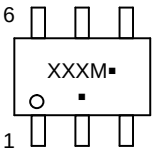
All the device pins are protected against electrostatic discharge at a level of 2 kV HBM. The output has been considered with a particular attention with ESD structure able to sustain typically more than 2 kV HBM. Actually more than 4 kV has been measured on this specific output pin. This feature is particularly important for video driver which usually constitutes the last stage in the video chain before the video output connector.

SC−88 2.00x1.25x0.90, 0.65P
CASE 419B−02
ISSUE Z

DATE 18 APR 2024

_ BURRS. MOLD FLASH,
PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED MOUNTING

STYLES ON PAGE 2

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED