

NCS36000

OPERATING RANGES (N e 6)

Rating	Symbol	Min	Typ	Max	Unit
Al g P e S ly	V_{DD}	3.0	5.0	5.75	V
Al g G d Refe e ce	V_{SS}		0.0	0.1	V
S ly C e (S a dby, N L ad)	I_{DD}			170 μ	A
Digi al I (MODE)	V_{ih}	0.7 * V_{DD}	V_{DD}	$V_{DD} + 0.3$	V
	V_{il}	VSS		$V_{DD} * 0.28$	
Digi al O (OUT, LED)	P h P I I O (10 mA L ad)	V_h	0.67 * V_{DD}	V_{DD}	V
		V_l	VSS	$V_{DD} * 0.3$	
OP1_P (Se l) (N e 7)	AMP 1 IN	0.1		$V_{DD} 1.1$	V
Ambie Tem e a e	T_A	40		85	$^{\circ}C$

6. Refe ELECTRICAL CHARACTERISTICS a d APPLICATION INFORMATION f Safe O e a i g a ea.

7. G a a eed By De ig (N e e d a a m e e).

ELECTRICAL CHARACTERISTICS $V_i = 1V, C_i = 100F, C_o = 100F$, f y ical al e $T_A = 25^{\circ}C$; le he i e ed.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
LDO Voltage Reference						
O V l age	$V_{DD} = 3.0V \text{ } 5.75V$	VREF	2.6	2.7	2.8	V
S ly C e	$V_{DD} = 3.0V \text{ } 5.75V$	IREF		20	50	μA
C m a a High T i Le el		V_h	2.413	2.5	2.588	V
C m a a L T i Le el		V_l	1.641	1.7	1.760	V
Refe e ce l age f i e i g i f e c d a m l i f e		V_m	2.007	2.1	2.174	V

System Oscillator

O cilla F e e cy	$V_{DD} = 5.0V$ $R_3 = 220k\Omega$ $C_2 = 100F$	OSC		62.5		Hz
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Window Comparator

L e T i Th e h l d	See V l a b e					
Highe T i Th e h l d	See V h a b e					

Differential Amplifiers (Amplifier Circuit)

DC Gai	$V_{DD} = 5.0V$ (N e 8)	A	80			dB
C m m m del Ra ge	$V_{DD} = 5.0V$ (N e 8)	CMIR	0.1		$V_{DD} 1.1$	V
P e S ly Rejec i Ra i	$V_{DD} = 5.0V$ (N e 8)	PSRR		60		dB
O D i e C e	$V_{DD} = 5.0V$ (N e 8)	I_{1}			25	μA

POR

POR Relea e V l age		V_{POR}	1.35		2.85	V
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8. G a a eed By De ig (N e e d a a m e e).

NCS36000

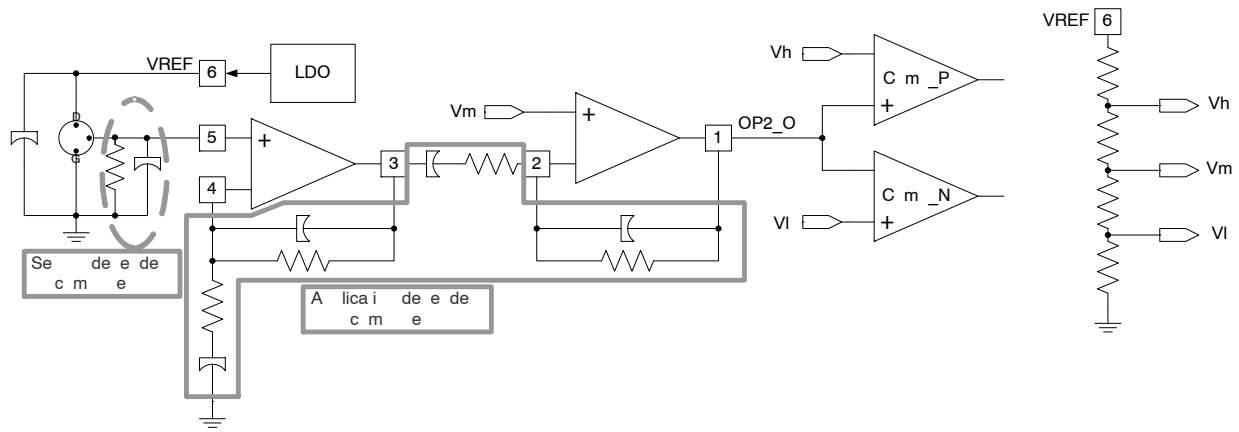


Figure 5. Figure Showing Simplified Block Diagram of Analog Conditioning Stages

Digital Signal Processing Block (all times assume a 62.5 Hz system oscillator frequency)

The digital signaling processing block performs three major functions.

The first function is that the device toggles LED during the start up sequencing at approximately two hertz regardless of the state of the XLED_EN pin. The startup sequence lasts for thirty seconds. During that time the OUT pin is held low regardless of the state of OP2_O.

The second function of the digital signal processing block is to insure a certain glitch width is seen before OUT is toggled. The digital signal processing block is synchronous with the system oscillator frequency and therefore the deglitch time is related to when the comparators toggle within the oscillator period. A signal width less than two clock period is guaranteed to be deglitched as a zero. A signal width of greater than three clock cycles is guaranteed to be de or 312002 Tc .0415 Tz Sednditioni7)(hI906 TD2djac 1 0to when0103757 -1.puls04) 1.9(occur outside J T* - -.0out n no

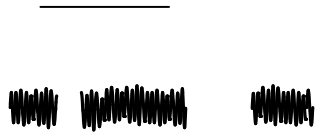


Figure 7. Timing Diagram for Dual-Pulse Mode Detection

NCS36000

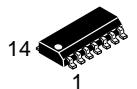
ORDERING INFORMATION

Device	Package	Shipping†
NCS36000DRG	SOIC 14 (Pb Free)	3000 / Tape & Reel

DISCONTINUED (New 13)

NCS36000DG	SOIC 14 (Pb Free)	55 Units / Rail
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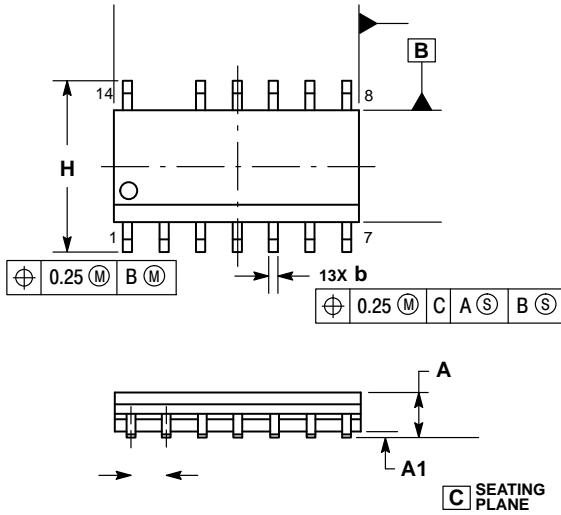
† If main area details specific, include a lead time and a reference, lead time reference Tape and Reel Packaging



SCALE 1:1

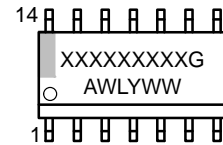
SOIC 14 NB
CASE 751A-03
ISSUE L

DATE 03 FEB 2016



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
 5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

STYLES ON PAGE 2

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STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE

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