Bluetooth® 5.2 Radio System-on-Chip (SoC) for Automotive

NCV-RSL10

Introduction

A member of the RSL10 product family, NCV−RSL10 brings the industry's lowest power Bluetooth Low Energy technology to the automotive industry. NCV−RSL10 helps enable advanced new functionality including keyless entry using a fob or smartphone, active safety and diagnostic alerts, and enhanced infotainment controls while maximizing energy efficiency.

The Bluetooth 5.2 certified radio SoC supports 2 Mbps data rates, twice the speed possible with previous Bluetooth generations. Specially designed and ques,Sy

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FEATURES

- **Arm Cortex−M3 Processor:** A 32−bit core for real−time applications, specifically developed to enable high−performance low−cost platforms for a broad range of low−power applications.
- **LPDSP32:** A 32−bit Dual Harvard DSP core that efficiently supports custom crypto graphic algorithms or other signal processing that require significant number crunching.
- **Radio Frequency Front−End:** Based on a 2.4 GHz RF transceiver, the RFFE implements the physical layer of the Bluetooth Low Energy technology standard and other proprietary or custom protocols.
- **Protocol Baseband Hardware:** Bluetooth 5.2 certified and includes support for a 2 Mbps RF link and custom protocol options. The RSL10 baseband stack is supplemented by support structures that enable implementation of **onsemi** and customer designed custom protocols.
- **Highly−Integrated SoC:** The dual−core architecture is complemented by high−efficiency power management units, oscillators, flash and RAM memories, a DMA

Table 3. ELECTRICAL PERFORMANCE SPECIFICATIONS
Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C for VBAT = VDDO = 3 V in DC−DC (buck) mode.

Description	Symbol	Conditions	Min	Typ	Max	Units
OVERALL						
Current consumption RX, V_{BAT} = 3 V	I_{VBAT}			0.9		mA
Current consumption TX, V_{BAT} = 3 V	I_{VBAT}			0.9		mA
Deep sleep current, example 1, V_{BAT} = 3 V	Ids1	Wake up from wake up pin or DIO wake up.		25		nA
Deep sleep current, example 2, V_{BAT} = 3 V	Ids2	Embedded 32 kHz oscillator running with interrupts from timer or external pin.		40		nA
Deep sleep current, example 3, V_{BAT} = 3 V	Ids3	As Ids2 but with 8 kB RAM data retention.		100		nA
Standby Mode current, V_{BAT} = 3 V	Istb	Digital blocks and memories are not clocked and are powered at a reduced voltage.		17		μA
EEMBC ULPMark BENCHMARK, CORE PROFILE						
ULPMark CP 3.0 V		Arm Cortex−M3 processor running from RAM, VBAT= 3.0 V, IAR C/C++ Compiler for ARM 8.20.1.14183		1090		ULP Mark
ULPMark CP 2.1 V		Arm Cortex−M3 processor running from RAM, VBAT= 2.1 V, IAR C/C++ Compiler for ARM 8.20.1.14183		1260		ULP Mark
EEMBC CoreMark BENCHMARK for the Arm Cortex−M3 Processor and the LPDSP32 DSP						
Arm Cortex−M3 processor running from RAM		At 48 MHz SYSCLK. Using the IAR 8.10.1 C compiler, certified		159		Core Mark
LPDSP32 running from RAM		At 48 MHz SYSCLK Using the 2020.03 release of the Synopsys LPDSP32 C compiler		174		Core Mark
Arm Cortex−M3 processor and LPDSP32 running from RAM, VBAT = 3 V		At 48 MHz SYSCLK		284		Core Mark/ mA
Arm Cortex−M3 processor running CoreMark from RAM, VBAT = 3 V		At 48 MHz SYSCLK (processor consumption only)		12.3		μA/MHz
Arm Cortex−M3 processor running CoreMark from Flash, VBAT = 3 V		At 48 MHz SYSCLK (processor consumption only)		14.6		μA/MHz
LPDSP32 running CoreMark from RAM, VBAT = 3 V		At 48 MHz SYSCLK (processor consumption only)		8.2		μA/MHz
INTERNALLY GENERATED VDDC: Digital Block Supply Voltage						
Supply voltage: operating range						

Table 5. VDDC Target Trimming Voltage as a Function of SYSCLK Frequency

VDDC Voltage (V)	Maximum SYSCLK Frequency (MHz)	Restriction
0.92	≤ 24	The ADC will be functional in low frequency mode and between 0 and 85°C only.
1.00	≤ 24	Fully functional
1.05	48	Fully functional

NOTE: These are trimming targets at room/ATE temperature 25～30°C.

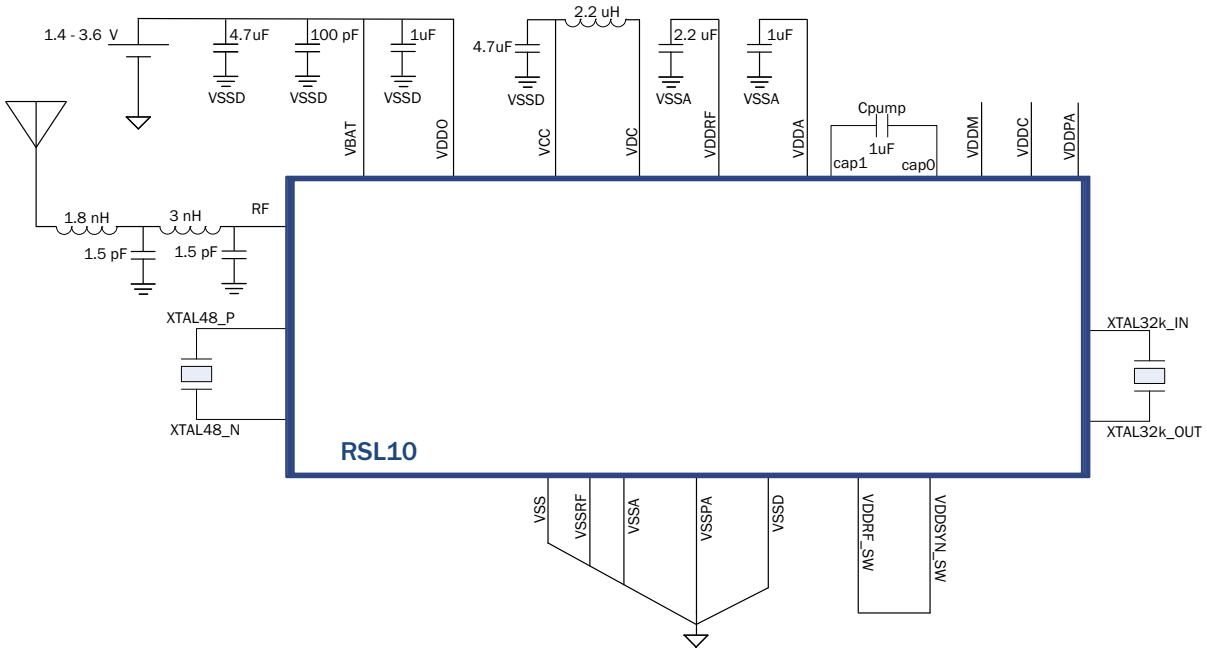
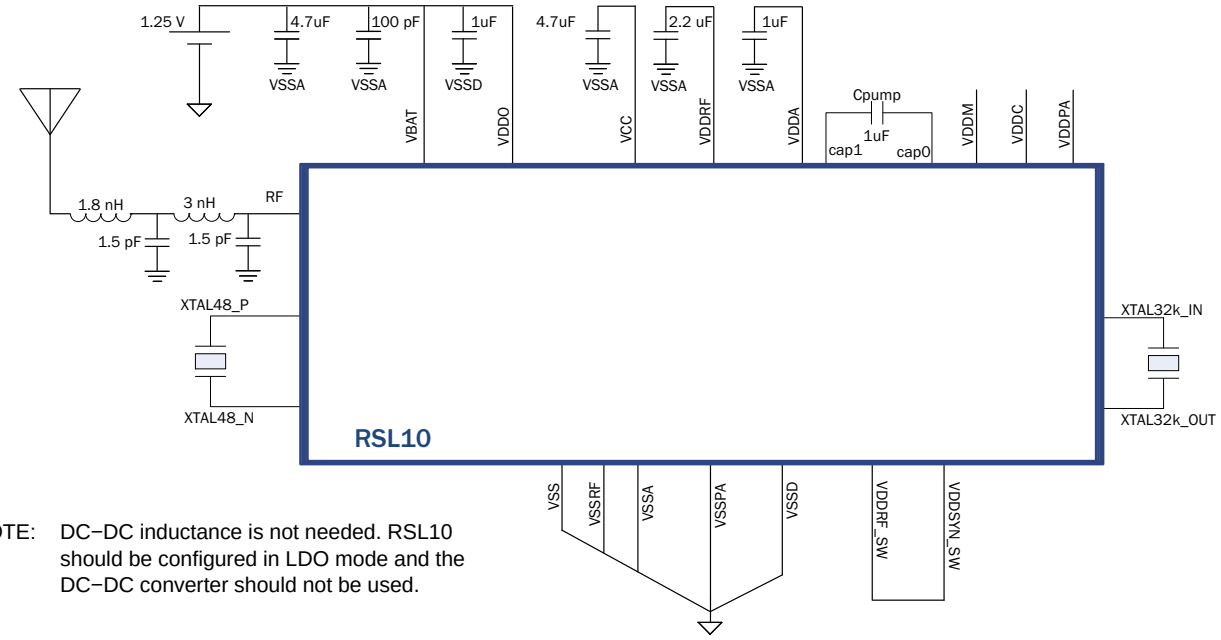


Figure 2. RSL10 Application Diagram in Buck Mode



NOTE: DC−DC inductance is not needed. RSL10 should be configured in LDO mode and the DC−DC converter should not be used.

Figure 3. RSL10 Application Diagram in LDO Mode

Table 8. CHIP INTERFACE SPECIFICATIONS

Pad Name	Description	Power Domain	I/O	A/D	Pull	Pad #, QFN48
VBAT						

Table 8. CHIP INTERFACE SPECIFICATIONS

Pad Name	Description	Power Domain	I/O	A/D	Pull	Pad #, QFN48

ARCHITECTURE OVERVIEW

The architecture of the RSL10 chip is shown in Figure 4.

Figure 4. RSL10 Architecture

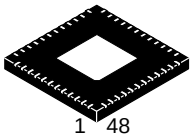
NCV−RSL10

Arm Cortex−M3 Processor Subsystem

The Arm Cortex−M3 processor subsystem includes the Arm Cortex−M3 processor, which is the master processor of the RSL10 chip. It also contains the Bluetooth baseband controller, and all interfaces and other peripherals.

Arm Cortex−M3 Processor

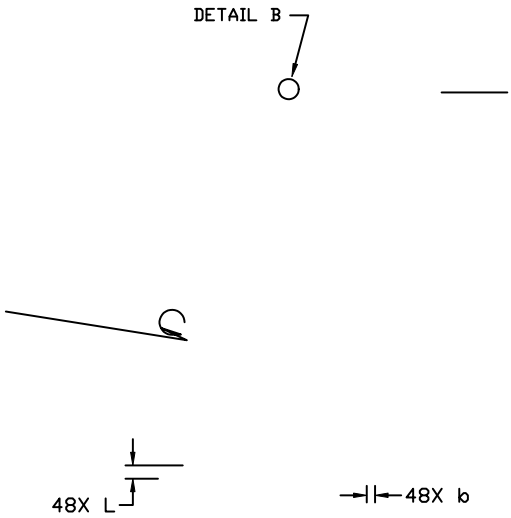
The Arm Cortex−M3 processor is a state−of−the−art 32−bit core with embedded multiplier and ALU for handling



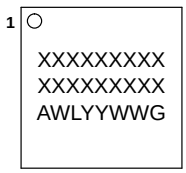
SCALE 2:1

QFNW48 7x7, 0.5P
CASE 512AD
ISSUE B

DATE 18 JAN 2019



GENERIC
MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.