ORDERING INFORMATION

Device	Package

FEATURES

Arm Cortex−M33 Processor

The Cortex−M33 32−bit Armv8−M processor is designed for IoT and deeply embedded applications that require high performance, power efficiency and security. The processor has many features to execute high performance applications such a Floating−Point Unit (FPU), DSP extensions and Memory Protection Unit (MPU). Secure debug is done through the SWJ−DP which combines JTAG−DP and SW−DP for either JTAG probe or Serial Wire Debug (SWD) connection.

Cybersecurity Platform

The Cortex−M33 processor with TrustZone Armv8−M security extensions forms the basis of the security platform. The Arm CryptoCell−312 allows for end−to−end product

Software Development Kit

Contains Eclipse−based **onsemi** IDE plus support for other industry standard development environments, Bluetooth protocol stack, sample applications, libraries and many other software components and tools to enable rapid application development.

RoHe Development Kit

Arm Cortex−M33 Processor

The Cortex−M33 32−bit Armv8−M processor is designed for IoT and deeply embedded applications that require high performance, power efficiency and security. The processor has many features to execute high performance applications such a Floating−Point Unit (FPU), DSP extensions and Memory Protection Unit (MPU). Secure debug is done through the dedicated Serial Wire Debug Port (SW−DP) interface.

DMA Controller

The Direct Memory Access (DMA) Controller allows background transfers between peripherals and memories without processor intervention. The processor can be in a low power state or used for other computational tasks while the transfer occurs. The DMA is connected to the processor, peripherals and RAM memories and has four independent channels.

Cybersecurity Platform

The Cortex−M33 processor with TrustZone Armv8−M security extensions forms the basis of the security platform that is extended with Arm CryptoCell−312.

Secure Boot with Root of Trust

The secure boot ROM authenticates firmware in flash with a certificate−based mechanism using a private−public key scheme. This is the basis of the hardware Root of Trust. This same mechanism ensures continuity of the hardware Root of Trust after secure Firmware−Over−The−Air (FOTA) update.

Data and Application Encryption

User available cryptographic services including AES−128, AES−256, SHA−256, Hash Message Authentication Code (HMAC), PKA (Public Key Accelerator), ChaCha and AIS−31 compliant True Random Number Generator (TRNG) allow for development of custom proprietary security solutions.

TrustZone

Enables secure software access control to protect critical software and hardware resources.

Secure Lifecycle State Management

Lifecycle states refers to the multiple states RSL15 could go through during its lifetime. The first lifecycle state is the Chip Manufacture (CM) Lifecycle State. The device manufacture transitions to the Device Manufacture (DM) Lifecycle State. At field deployment, it is transitioned to the Secure (SE) Lifecycle State. A Return to Manufacturer (RMA) State is also available. Lifecycle state management ensures the authenticity, integrity and confidentiality of code and data belonging to different stakeholders at each lifecycle.

In addition to the Secure Lifecycle States, an Energy Harvesting (EH) Mode is available for applications that require fast cold startup (initial application of VBAT) but do not require secure boot with Root of Trust. This mode is especially useful when RSL15 is used in energy harvesting systems.

RF Subsystem

The RSL15 2.4 GHz radio front−end implements the physical layer for the Bluetooth Low Energy standard and other standard, proprietary, or custom protocols.

It operates in the worldwide deployable 2.4 GHz ISM band (2.4000 to 2.4835 GHz).

RF Architecture

The 2.4 GHz radio front−end is based on a low−IF architecture and comprises the following building blocks:

- High performance single−ended RF port which alleviates the need for an external balun
- On−chip matching network with 50 Ω RF input
- Low power LNA (low noise amplifier), and mixer

Peripherals and Subsystems Availability in Power Modes

The different power modes allow for low power operation in many types of applications. When applications utilize one or more external sensors that require continued biasing regardless of the power mode of RSL15, it may be possible to use the VDDA voltage for this purpose.

VDDA can be kept active even in Sleep, Smart Sense and Standby Modes.

Table 2 describes the peripherals available in all power modes.

Table 2. POWER MODE PERIPHERAL AVAILABILITY

Component	Power Mode				
	Run	**Idle**	**Standby**	**Smart Sense**	**Sleep**
Processor	On	On	Off	Off	Off
Baseband/RF	On	On	Off	Off	Off
RAM Retention	N/A	N/A	N/A	Available	Available
CryptoCell	On	On	On or Off	On or Off	On or Off
RTC	On	On	On or Off	On or Off	On or Off
ULP Data Acquisition Subsystem	On	On	On or Off	On or Off	Off
Successive Approximation ADC	On	On	On or Off	On or Off	Off
Pulse Counter	On	On	On or Off	On or Off	Off
Comparator	On	On	On or Off	On or Off	On or Off
DAC	On	On	Off	Off	Off
ACS−PWM	On	On	On or Off	On or Off	On or Off
PWM	On	On	Off	Off	Off
Low Speed ADC	On	On	Off	Off	Off
32k Clock Output	On	On	On or Off	On or Off	On or Off
I2C	On	On	Off	Off	Off
SPI	On	On	Off	Off	Off
UART	On	On	Off	Off	Off
LIN	On	On	Off	Off	Off
PCM	On	On	Off	Off	Off
Temp Sensor	On	On	Off	Off	Off

ULP Data Acquisition Subsystem

The ULP Data Acquisition Subsystem comprises a small FIFO, Accumulator and Threshold Comparator that can be used in combination with the Successive Approximation ADC and pulse counter to perform data acquisition and rudimentary data processing and decision making.

The ULP Data Acquisition Subsystem has various features to further reduce power consumption such as Burst Sampling Mode, which allows for bursts of high speed sampling followed by an adjustable delay between sampling bursts.

The pulse counter can be configured to accept inputs from any of GPIO[3:0]. It counts pulses from these GPIOs during

Peripherals

Timers

There are four independent 24−bit timers that can operate as single−shot, multi−shot or free−run. An interrupt can be generated on timer expiration. Also, a GPIO interrupt can capture and store the current timer value.

Watchdog

The independent watchdog timer cannot be disabled. It must be reloaded at regular intervals. At the first timer expiration, an interrupt is generated and the timer is reloaded. At the second timer expiration, a reset is issued to the system.

PWM

Memory Map

The RSL15 memory map is shown in Figure 5 (512 kB flash version only).

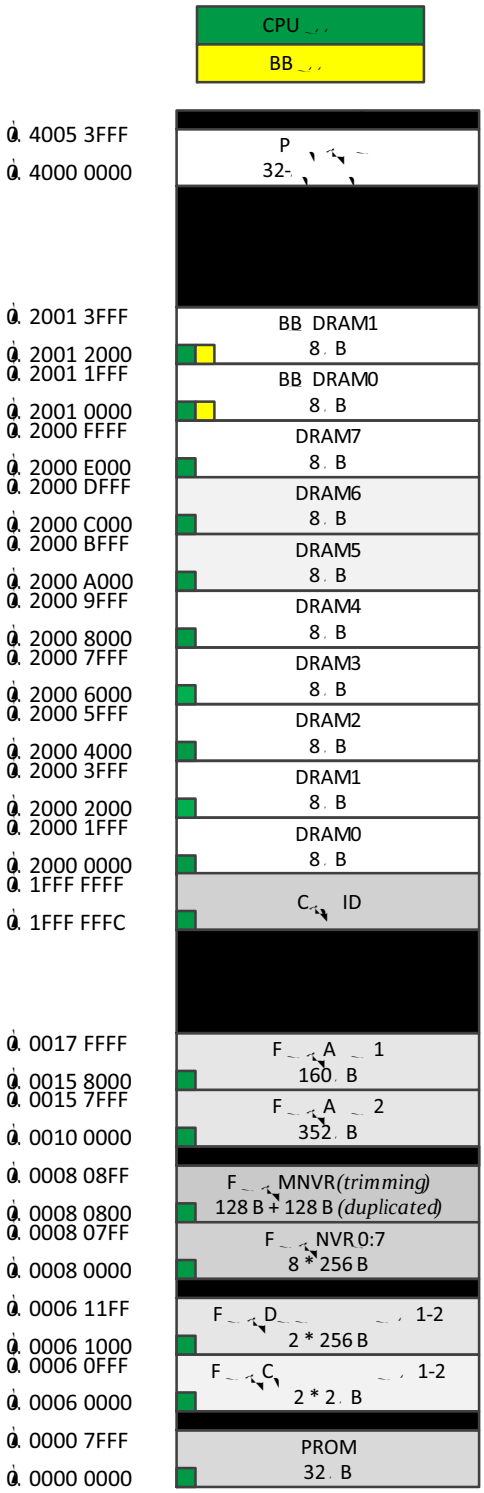

Figure 5. RSL15 Memory Map

System Clock

The following table lists the sources and valid frequencies of System Clock.

Table 5. SYSTEM CLOCK

System Clock Frequency (MHz)

Power Consumption

RF Current Consumption

Table 6 shows key peak current consumption values for RF activity. Unless otherwise noted, the specifications mentioned in the table below are valid at 25 C, VBAT = VDDO (Buck mode for VBAT > 1.4 V, LDO mode for VBAT 1.4 V), 48 MHz (RFCLK) active, Radio ON and internal supplies trimmed to factory defaults.

Table 6. RF CURRENT CONSUMPTION

Operating Conditions	VBAT	DC Conversion	Min	Typ	Max	Unit
Radio Receive Mode Rx @ 125 kbps, 2.4 GHz 8 MHz system clock Cortex−M33 running BLE baseband only All Peripherals Disabled 64 kB RAM enabled	3.0 V	BUCK Mode		2.9		mA
	1.8 V	BUCK Mode		4.4		
	1.25 V	LDO Mode		6		
Radio Receive Mode Rx @ 500 kbps, 2.4 GHz 8 MHz system clock Cortex−M33 running BLE baseband only All Peripherals Disabled 64 kB RAM enabled	3.0 V	BUCK Mode		2.9		mA
	1.8 V	BUCK Mode		4.4		
	1.25 V	LDO Mode		6		
Radio Receive Mode Rx @ 1 Mbps, 2.4 GHz 8 MHz system clock Cortex−M33 running BLE baseband only All Peripherals Disabled 64 kB RAM enabled	3.0 V	BUCK Mode		2.7		mA
	1.8 V	BUCK Mode		4.3		
	1.25 V	LDO Mode		5.8		
Radio Receive Mode Rx @ 2 Mbps, 2.4 GHz 8 MHz system clock Cortex−M33 running BLE baseband only All Peripherals Disabled 64 kB RAM enabled	3.0 V	BUCK Mode		3.2		mA
	1.8 V	BUCK Mode		4.9		
	1.25 V	LDO Mode		6.7		
Radio Transmit Mode Tx @ 1 Mbps, 2.4 GHz, 0 dBm 8 MHz system clock Cortex−M33 running BLE baseband only All Peripherals Disabled 64 kB RAM enabled	3.0 V	BUCK Mode		4.3		mA
	1.8 V	BUCK Mode		6.7		
	1.25 V	LDO Mode		9.1		
Radio Transmit Mode Tx @ 1 Mbps, 2.4 GHz, 3 dBm 8 MHz system clock Cortex−M33 running BLE baseband only All Peripherals Disabled 64 kB RAM enabled	3.0 V	BUCK Mode		8		mA
	1.8 V	BUCK Mode		12.3		
	1.25 V	LDO Mode		16.9		
Radio Transmit Mode Tx @ 1 Mbps, 2.4 GHz, 5 dBm 8 MHz system clock Cortex−M33 running BLE baseband only All Peripherals Disabled 64 kB RAM enabled	3.0 V	BUCK Mode		10.6		mA
	1.8 V	BUCK Mode		16.5		
	1.25 V	LDO Mode		22.5		
Radio Transmit Mode Tx @ 1 Mbps, 2.4 GHz, 6 dBm	3.0 V	BUCK Mode		11.4		mA

Run Mode Current Consumption

Table 7 shows key current consumption values for Run Mode. Unless otherwise noted, the specifications mentioned in the table below are valid at 25 C, VBAT = VDDO (Buck mode for VBAT > 1.4 V, LDO mode for VBAT 1.4 V), 48 MHz (RFCLK) active, Radio OFF and internal supplies trimmed to factory defaults.

Table 7. RUN MODE CURRENT CONSUMPTION

Operating Conditions	VBAT	DC

Standby Mode Current Consumption

Table 9 shows key current consumption values for Standby Mode. Unless otherwise noted, the specifications mentioned in the table below are valid at 25 C, VBAT = VDDO (Buck mode for VBAT > 1.4 V, LDO mode for VBAT 1.4 V), 48 MHz (RFCLK) inactive, Radio OFF and internal power supplies trimmed to factory defaults.

Table 9. STANDBY MODE CURRENT CONSUMPTION

Operating Conditions	Wakeup Source	VBAT	DC Conversion	Min	Typ	Max	Unit
Clocks stopped All peripherals disabled **8 kB RAM retained** 32 kHz RC32 inactive 32 kHz XTAL32K inactive	GPIO	3.0 V	BUCK Mode		17		μA
		1.8 V	BUCK Mode		20		
		1.25 V	LDO Mode		26		
Clocks stopped All peripherals disabled **16 kB RAM retained** 32 kHz RC32 inactive 32 kHz XTAL32K inactive	GPIO	3.0 V	BUCK Mode		17.5		μA
		1.8 V	BUCK Mode		21		
		1.25 V	LDO Mode		26		
Clocks stopped All peripherals disabled **32 kB RAM retained** 32 kHz RC32 inactive 32 kHz XTAL32K inactive	GPIO	3.0 V	BUCK Mode		17.6		μA
		1.8 V	BUCK Mode		21		
		1.25 V	LDO Mode		26		
Clocks stopped All peripherals disabled **64 kB RAM retained** 32 kHz RC32 inactive 32 kHz XTAL32K inactive	GPIO	3.0 V	BUCK Mode		18		μA
		1.8 V	BUCK Mode		21		
		1.25 V	LDO Mode		26		
Clocks stopped All peripherals disabled **8 kB RAM retained** **32 kHz RC32 active** 32 kHz XTAL32K inactive	RTC timer	3.0 V	BUCK Mode		21		μA
		1.8 V	BUCK Mode		22		
		1.25 V	LDO Mode		29		
Clocks stopped All peripherals disabled **8 kB RAM retained** 32 kHz RC32 inactive **32 kHz XTAL32K active**	RTC timer	3.0 V	BUCK Mode		19		μA
		1.8 V	BUCK Mode		21		
		1.25 V	LDO Mode		28		

Sleep Mode Current Consumption

Table 10 shows key current consumption values for Sleep Mode. Unless otherwise noted, the specifications mentioned in the table below are valid at 25

ULP Data Acquisition Subsystem Performance

Table 11 shows key current consumption values for ULP Data Acquisition Subsystem in Smart Sense Mode. Unless otherwise noted, the specifications mentioned in the table below are valid at 25 C, VBAT = VDDO (Buck mode for VBAT > 1.4 V, LDO mode for VBAT 1.4 V), 48 MHz (RFCLK) inactive, Radio OFF and internal supplies trimmed to factory defaults.

Table 11. ULP DATA ACQUISITION SUBSYSTEM PERFORMANCE

Operating Condition	Min	Typ	Max	Unit
Continuous ADC operation in Smart Sense mode with wakeup on ADC threshold Configuration/conditions: VBAT = 3 V, BUCK Mode, Successive Approximation ADC enabled and selected, XTAL32K, VREF = VBAT reference selected, ADC Fs = 256 sps, accumulation 4 samples. Processor would wake to Run mode by ADC threshold but this is not included in this measurement		206		nA
Continuous ADC operation in Smart Sense mode, wakeup on FIFO full, transfer content to RAM Configuration/conditions: VBAT = 3 V, BUCK Mode, 16 kB RAM retained, XTAL32K, Successive Approximation ADC enabled, VREF = VBAT, ADC Fs = 1 ksps, accumulation 16 samples, FIFO Size 16. Processor wakes to Run mode every 256 ms to transfer samples to RAM		2.1		μA
Continuous ADC operation in Smart Sense mode, wakeup on FIFO full, transfer content to RAM Configuration/conditions: VBAT = 3 V, BUCK Mode, 16 kB RAM retained. XTAL32K, Successive Approximation ADC enabled, VREF = VDDA, ADC Fs = 1 ksps, Accumulation 16 samples, FIFO Size 16. Processor wakes to Run mode every 256 ms to transfer samples to RAM		4.1		μA
Continuous Pulse Counter accumulation in Smart Sense mode, wakeup when FIFO full, transfer content to RAM Configuration/conditions: VBAT = 3 V, BUCK Mode, 16 kB RAM retained, XTAL32K, Pulse Counter enabled, Pulse Count Interval 1000 ms, accumulation of 5 samples, result stored in FIFO. Processor wakes to Run mode every 5 s to transfer sample to RAM		348		nA

Wakeup Timing Specifications

Table 12. WAKEUP TIMING SPECIFICATIONS

Description	Symbol	Conditions	Min	Typ	Max	Unit
Cold startup − VBAT applied to entering RUN mode		To start of startup code execution (Energy Harvesting state)		2.4		ms
		To start of startup code execution (Secure state) using secure bootloader				

Table 13. EEMBC BENCHMARK SCORES

Table 14. RF SPECIFICATIONS (continued)

Description	Symbol	Conditions	Min	Typ	Max	Unit
TRANSMIT MODE SPECIFICATIONS						
Transmit power range						

Table 17. SLOW RC OSCILLATOR (RC32)

Parameter	Symbol	Notes	Min	Typ	Max	Unit
Factory trimmed frequency	RC32			32.768		kHz
Startup time		After VBAT applied			2	ms
Current consumption		Temperature comp enabled		120		nA

Table 18. 48 MHz CRYSTAL OSCILLATOR (RFCLK)

Parameter	Symbol	Notes	Min	Typ	Max	Unit
Crystal Frequency	RFCLK			48		MHz
Startup time		After VBAT Applied			1.5	ms
Recommended XTAL parameter ESR		Equiv. Series res.	20		80	Ω
			6	8	10	pF

66 558.76 070552.189 5660.756 10723 Tc[(Ty)72.3(p)]TJ

Low Speed ADC Converter (LSAD) Specifications

Table 22. LOW SPEED ADC CONVERTER (LSAD) SPECIFICATIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Resolution	ADC_{RES}		8	12	14	bits
Precision	ADC_{PRES}	0−50 C	−20		20	mV
Input voltage range	ADCRANGE		0		2	V
INL	ADC_{INL}		−2		+2	mV
DNL	ADC_{DNL}		−1		+1	mV
Channel sampling frequency	ADCCH_SF	8 channels are converted sequentially, ADC running at 50 kHz	0.0195		6.25	kHz

NOTE: All LSAD parameters are for SLOWCLK at 1 MHz.

Table 23. DAC SPECIFICATIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output voltage range	Vout	Cannot exceed VDDO	0.1			

Pulse Counter Specifications

Table 25. PULSE COUNTER SPECIFICATIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Pulse width			>1 sensor clock cycle			cycle
Pulse count duration		Using accumulation to reach max	0.976		16000	ms

GPIO Interface Specifications

Table 26. GPIO INTERFACE SPECIFICATIONS

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Voltage level for HIGH Input	VIH			0.75 x VDDO		VDDO +0.3	V
Voltage level for LOW Input	VIL			−0.3		0.25 x VDDO (Note 9)	V
Voltage level for HIGH Output	VOH			VDDO − 0.4			V
Voltage level for LOW Output	VOL					0.4	V
Voltage at GPIO selected as LSAD input	Vlsad			VSSA − 0.3		2	V
Drive Strength (Note 10)	IOH / IOL	VDDO = 3.3 V	Drive = 0		3.4		mA
			Drive = 1		6.8		mA
			Drive = 2		13.5		mA
			Drive = 3		20.2		mA
		VDDO = 1.8 V	Drive = 0		2.0		mA
			Drive = 1		4.0		mA

LDO Mode Operation

Figure 7 shows RSL15 external components and connections for LDO Mode operation with GPIO Levels at GND and VBAT.

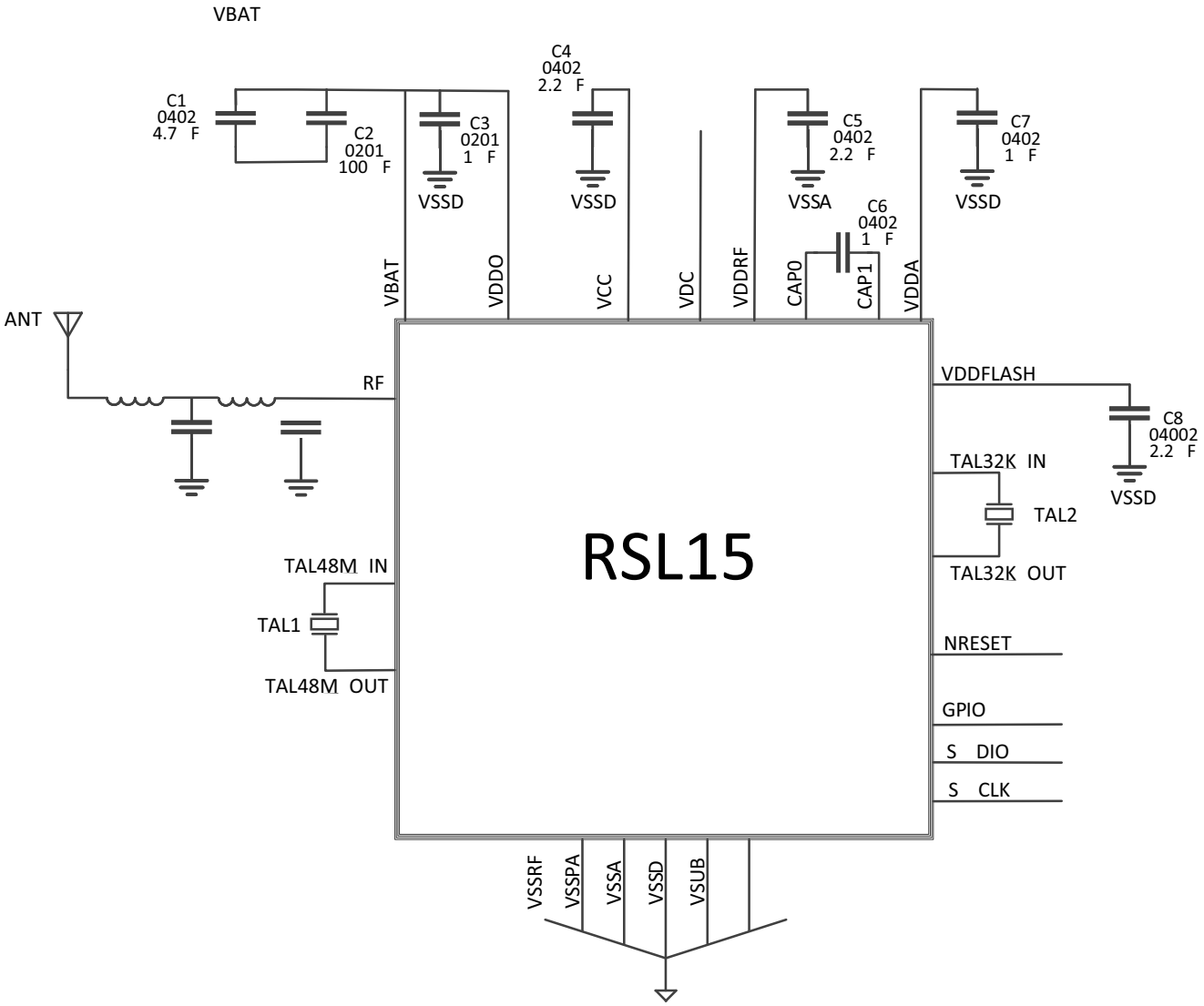

Figure 7. RSL15 LDO Mode Connection Diagram, VDDO = VBAT

External Component Overview

Table 27. RECOMMENDED EXTERNAL COMPONENTS

Components	Function	Recommended Typical Value	Nominal Tolerance
C1, C2	VBAT decoupling	4.7 μF // 100 pF (Note 11)	20%
C3	VDDO decoupling	1 μF	20%
C4	VCC decoupling	2.2 μF − GRM155C80J225KE95D, Murata − AMK105BJ225, Taiyo Yuden	20%
C5	VDDRF decoupling	2.2 μF	20%
C6	Pump capacitor for the charge pump	1 μF	20%
C7	VDDA decoupling	1 μF	20%
C8	VDDFLASH decoupling	2.2 μF	20%
L1	DC−DC converter inductance	2.2 μH (See Table 28 below)	20%
XTAL1	XTAL for 48 MHz oscillator	− 416F48022IKR, CTS Frequency Controls − 8Q−48.000MEEV−T, TXC Corporation, Taiwan	
XTAL2	XTAL for 32 kHz oscillator	− 9HT12−32.768KDZF−T, TXC Corporation − MC−306, Epson − CM8V−T1A, Micro Crystal Switzerland	
C9, C10, L2, L3	External harmonic filter	C9 1.5 pF / C10 1.5 pF 0.25 pF, C0G/NP0, Murata GRM0335C L2 3 nH / L3 1.8 nH 0.1 nH, Murata LQP03TN (Note 12)	

NOTE: Capacitors C1 to C8 recommendations:
Multilayer ceramic caps with nominal voltage 6.3 V (to reduce capacitance drop due to DC biasing effect), ESR < 0.2 Ω over frequency range 100k – 10MHz, Type X5R with max 15% variation over temperature range so 35% total capacitance tolerance.

11. The recommended decoupling capacitance uses 2 capacitors with the values specified.
12. For improved harmonic performance in environments where RSL15 is operating in close proximity to smartphones or base stations, FBAR filters such as the Broadcom ACPF−7924 can be applied instead of the suggested discrete harmonic filter.

Table 28. RECOMMENDED DC−DC CONVERTER INDUCTANCE TABLE

Manufacturer	Part Number	Case Size

PIN DEFINITIONS

QFN40 Pin Out

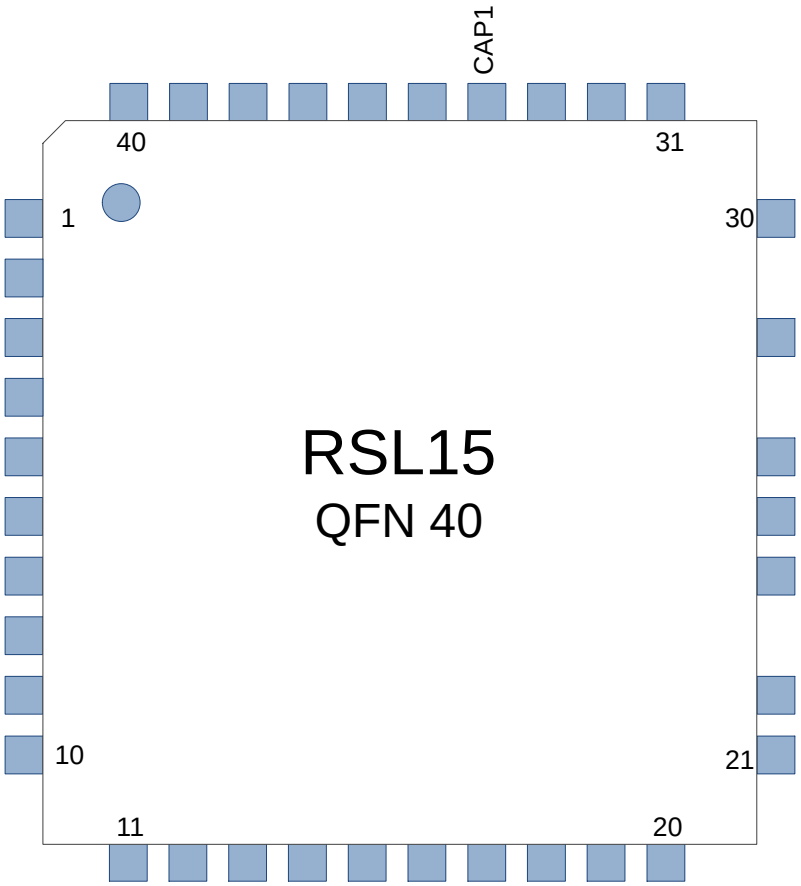

Figure 8. QFN40 Pin Out

Table 29. PIN DEFINITION AND MULTIPLEXING (continued)

Pad Name	Description	Power Domain	Type	Pull	Pad #, QFN
SHLD	Connect to ground				25
XTAL48M_IN	Input pin for 48 MHz XTAL				26
VSUB	Substrate ground (RF)		P		27
XTAL48M_OUT	Output pin for 48 MHz XTAL				28
VDDRF	LDO for RF		P		29
VSSRF	RF analog ground		P		30
RF	RF signal input/output (Antenna)		I/O		31
VSSPA	Ground for RF PA LDO	VDDA	P		32
VDDFLASH	LDO for Flash	VDDA	P		33
CAP1	Charge pump capacitor	VDDA			34
CAP0	Charge pump capacitor	VDDA			35
VDDA	Charge pump output for analog and flash supplies				36

Table 30. GPIO MULTIPLEXING (continued)

GPIO	Mode	Description
0:15	UART0_RX UART0_TX / LIN0_TX LIN_RX SPI0_MOSI/DATA0 SPI0_MISO/DATA1 SPI0_DATA2 SPI0_DATA3 SPI0_CS SPI0_CLK SPI1_MOSI/DATA0 SPI1_MISO/DATA1 SPI1_DATA2 SPI1_DATA3 SPI1_CS SPI1_CLK I2C0_SCL I2C0_SDA I2C1_SCL I2C2_SDA PWM0	

PCB LAYOUT GUIDELINES

1. Decoupling capacitors should be placed as close to the related balls as possible
2. Differential output signals should be routed as symmetrically as possible
3. Analog input signals should be shielded as well as possible
4. Pay close attention to the parasitic coupling capacitors
5. Special care should be made for PCB design in order to obtain good RF performance
6. Multi−layer PCB should be used with a keep−out area on the inner layers directly below the antenna matching circuitry in order to reduce the stray capacitances that influence RF performance
7. All the supply voltages should be decoupled as close as possible to their respective pin with high performance RF capacitors. These supplies should be routed separately from each other and if possible on different layers with short lines on the PCB from the chip's pin to the supply source
8. Digital signals should not be routed close to the crystal or the power supply lines
9. Proper DC−DC component placement and layout is critical to RX sensitivity performance in DC−DC mode. Minimize parasitic capacitance and inductance on the VDC node as much as possible.
10. [QFN only]: Ground EP by vias to a ground plane and/or through at least two VSS pins to PCB surface ground.
11. [QFN only]: Connect SHLD pin to EP, and connect SHLD to an external ground trace shielding XTAL48M_IN from SWCLK.

PACKAGE MARKING INFORMATION

Chip Identification

System identification is used to identify different system components. For the RSL15 chip, the key identifier components and values are as follows:

Chip Family: 0x0B
Chip Version: 0x02
Chip Major Revision: 0x02

ELECTROSTATIC DISCHARGE (ESD) SENSITIVE DEVICE

CAUTION: ESD sensitive device. Permanent damage may occur on devices subjected to high−energy electrostatic discharges. Proper ESD precautions in handling, packaging and testing are recommended to avoid performance degradation or loss of functionality.

SOLDER INFORMATION

The RSL15 QFN package is constructed with all RoHS compliant material and should be reflowed accordingly.

This device is Moisture Sensitive Class MSL1 and must be stored and handled accordingly. Re−flow according to IPC/JEDEC standard J−STD−020C, Joint Industry Standard: Re−flow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices. Hand soldering is not recommended for this part.

For more information, see SOLDERRM/D

QFNW40 6x6, 0.5P
CASE 484BC
ISSUE O

DATE 14 FEB 2022