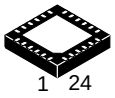

XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

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Figure 2. Internal Block Diagram

PIN CONNECTIONS

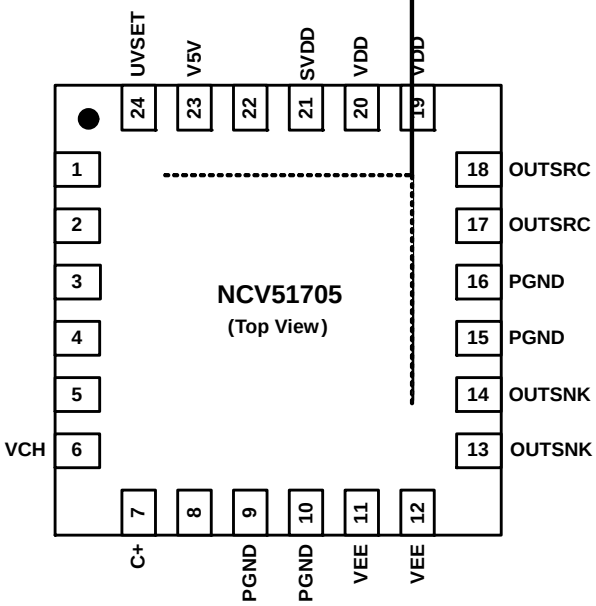

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{DD}	Power Supply Voltage	−0.3	28	V
V_{V5V}	Bias Rail	−0.3	5.5	V
V_{CH}	Charge Pump Supply Voltage	−0.3	10	V
V_{EE}	Charge Pump Output; Negative Gate Drive Voltage	−9	+0.3	V
V_{VEESET}	Charge Pump Output Voltage Select	−0.3	28	V
$V_{IN+;}$ V_{IN-}	Logic Input Voltage Levels	−0.3	V5V+0.3	V
V_{XEN}	Logic Output Voltage	−0.3	V5V+0.3	V
V_{UVSET}	UVLO SET Voltage	−0.3	V5V+0.3	V
V_{DESAT}	Desaturation / Current sense voltage	−0.3	12	V
V_{C+}	Positive node of the flying charge pump capacitor	−0.3	VCH+0.3	V
V_{C-}	Negative node of the flying charge pump capacitor	+0.3	V_{EE} -0.3	V
V_{OUTSRC}	Gate Drive Source Output Voltage	V_{EE} -0.3	V_{DD} +0.3	V
V_{OUTSNK}	Gate Drive Sink Output Voltage	V_{EE} -0.3	V_{DD} +0.3	V

f

Table 6. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{DD}	Positive Power Supply Voltage	10	22	V
V_{EE}	Negative Power Supply Voltage	−8	0	V
V_{CH}	Charge Pump Power Supply Voltage	0	8	V
V_{V5V}	5 V internal/external bias output	0	5.5	V
V_{ENA}	Logic Enable Voltage	0	5.5	V
V_{IN}	Logic Input Voltage	0	5.5	V
V_{XEN}	Logic Output Voltage	0	5.5	V
V_{VEESET}	Charge Pump Output Voltage Setting	0	22	V
V_{UVSET}	UVLO Threshold Setting	2	3.5	V
V_{DESAT}	Desaturation Voltage	0	10	V
f_{SW}	Operating Frequency (Note 6)		500	kHz
T_A	Operating Ambient Temperature	−40	125	C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Maximum operating frequency refers to ground referenced applications and might be limited by power dissipation below the recommended value.

Table 7. ELECTRICAL CHARACTERISTICS (V_{DD} = 20 V, V_{EESET} = 0 V and C_{LOAD} = 1000 pF for typical values T_J = 25 C, for min/max values T_J = −40 C to +125 C, unless otherwise specified.) (Note 7)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
VDD SECTION						
I_{DD}	Operating V_{DD} Supply Current	f_{IN} = 100 kHz, V_{EESET} = 5 V		12	18	mA
I_{QDD1}	Quiescent V_{DD} Supply Current 1	V_{IN+} = V_{IN-} = 0 V, V_{EESET} = 5 V		4.5	6.5	mA
I_{QDD2}	Quiescent V_{DD} Supply Current 2	V_{IN+} = 0 V, V_{IN-} = 5 V		0.85	1.1	mA
I_{UVSET}	Source Current for UV Voltage Set	V_{UVSET} = 3 V	20	25	30	μA
V_{DDUV+}	V_{DD} Supply Under−Voltage Positive−going Threshold	V_{UVSET} = 3 V	17	18	19	V
V_{DDUV-}	V_{DD} Supply Under−Voltage Negative−going Threshold	V_{UVSET} = 3 V	16	17	18	V
V_{DDHYS}	V_{DD} Supply UVLO Hysteresis Voltage	V_{DDUV+} − V_{DDUV-}		1		V
5V REGULATOR SECTION						
V_{V5V}	External Bypass for 5 V (Note 8)	T_J = 25 C	4.9	5	5.1	V
		Total Variation	4.75	5	5.25	V
V_{V5V_Reg}	5 V Line Regulation	10 V < V_{DD} < 22 V, I_{OUT} = 10 mA			50	mV
	[redacted]lation					
[redacted]	[redacted]rrent (N	[redacted]				[redacted]
CHARGE PUMP SECTION						
						V

Table 7. ELECTRICAL CHARACTERISTICS (V_{DD} = 20 V, V_{EESET} = 0 V and C_{LOAD} = 1000 pF for typical values T_J = 25 C, for min/max values T_J = −40

TYPICAL PERFORMANCE CHARACTERISTICS

TYPICAL CHARACTERISTICS ARE PROVIDED AT 25 C AND V_{DD} = 20 V UNLESS OTHERWISE NOTED.

Figure 4. Operating Current (I_{DD}) vs. Operating Voltage (V_{DD})

Figure 5. Operating Current (I_{DD}) vs. Operating Frequency

Figure 6. Propagation Delay Time vs. Operating Voltage (V_{DD})

Figure 7. Sourcing Current vs. Operating Voltage (V_{DD})

Figure 8. Sinking Current vs. Operating Voltage (V_{DD})

Figure 9. Operating Current (I_{DD}) vs.

TYPICAL PERFORMANCE CHARACTERISTICS

TYPICAL CHARACTERISTICS ARE PROVIDED AT 25 C AND V_{DD} = 20 V UNLESS OTHERWISE NOTED.

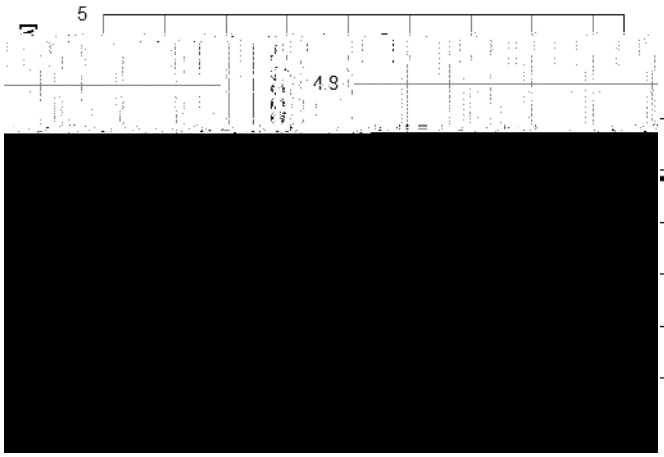

Figure 10. Quiescent Current 1 (I_{QDD1}) vs. Temperature

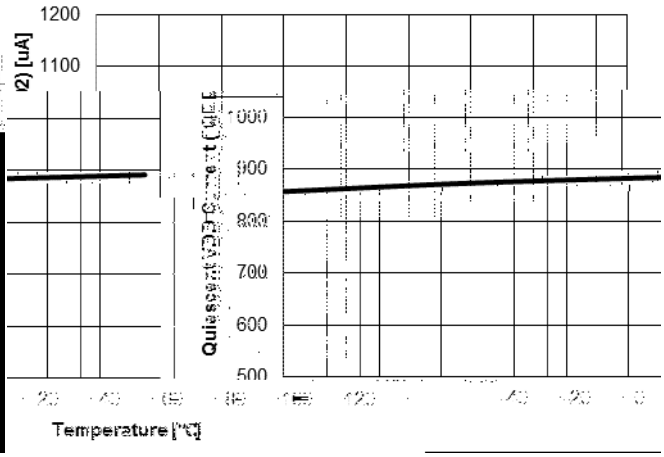

Figure 11. Quiescent Current 2 (I_{QDD2}) vs. Temperature

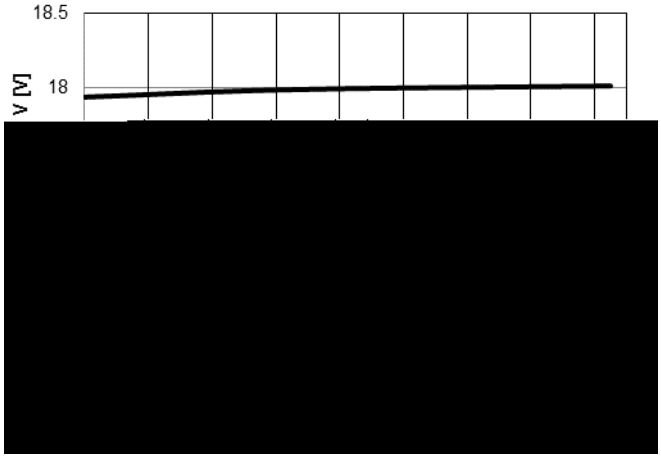

Figure 12. VDD UVLO vs. Temperature

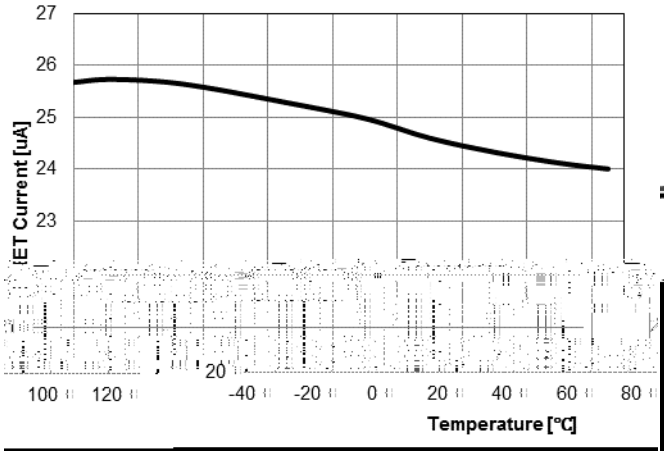

Figure 13. UVSET Current (I_{UVSET}) vs. Temperature

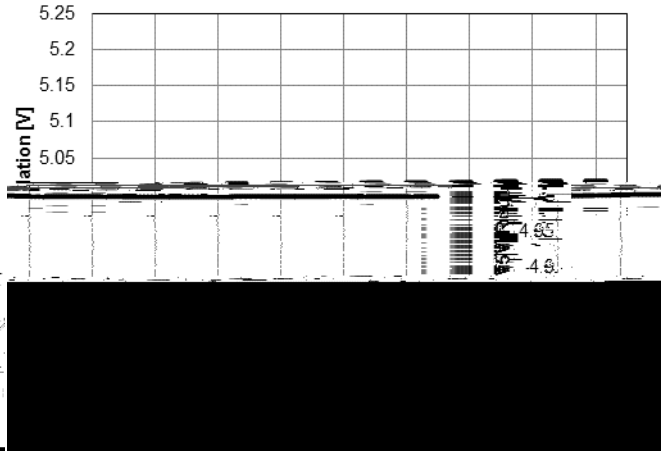

Figure 14. 5 V Regulated Output Voltage (V5V) vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

TYPICAL CHARACTERISTICS ARE PROVIDED AT 25 C AND V_{DD} = 20 V UNLESS OTHERWISE NOTED.

Figure 15. Negative Bias Voltage of Charge Pump vs. Temperature

Figure 16. VEE5 Regulated Voltage with $I_{VEE,MAX}$ vs. Temperature

Figure 17. Charge Pump Operating Frequency (f_{OSC}) vs. Temperature

Figure 18. Desaturation Current (I_{DESAT}) vs. Temperature

Figure 19. DESAT Threshold Voltage ($V_{TH,DESAT}$) vs. Temperature

NCV51705

APPLICATIONS INFORMATION

The NCV51705 can be quickly configured by following the steps outlined in this section. The component references made throughout this section refer to the schematic diagram and reference designations shown in Figure 27.

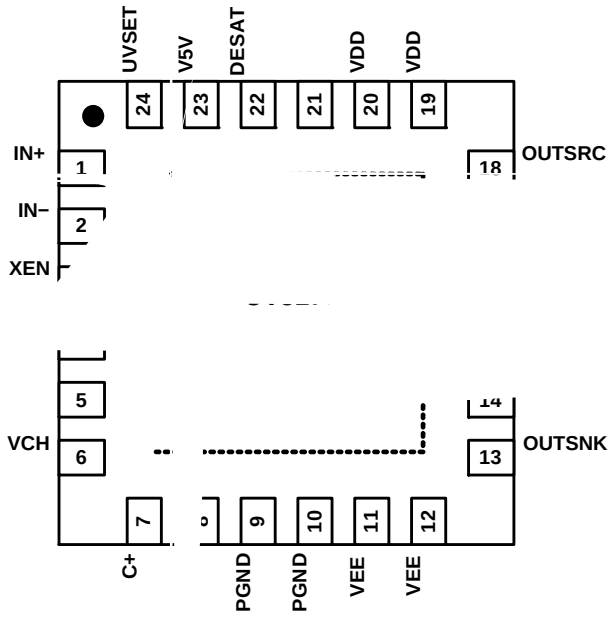

Figure 27. Application Schematic

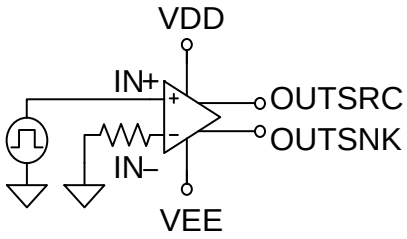

Figure 28. Non−inverting Input Configuration

Table 8. NON−INVERTING LOGIC, IN+, TRUTH TABLE

IN+ (PWM)	IN− (SGND)	OUTSRC	OUTSNK
0	0	0	1
1	0	1	0

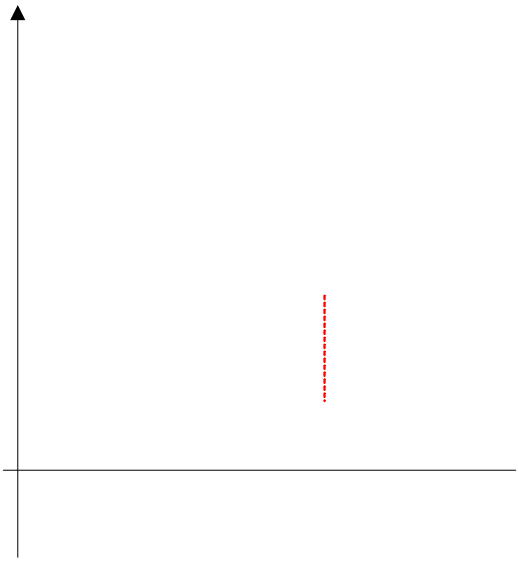

Table 10. XEN DELAY

Item	Timing Definition	Typical XEN Delay
ON Delay (IN to XEN)	IN+ rising (V_{IH}) to XEN falling (90%)	= T_{ON}
	IN− falling (V_{IL}) to XEN falling (90%)	= T_{ON}
OFF Delay (IN to XEN)	IN+ falling (V_{IL}) to XEN rising (10%)	= T_{OFF} + 40 ns
	IN− rising (V_{IH}) to XEN rising (10%)	= T_{OFF} + 40 ns

The intent of this signal is that it can be used as a fault flag and in half−bridge power topologies, can provide a synchronization signal for implementing cross−conduction (overlap) protection for the power transistors.

Whenever XEN is HIGH, V_{GS} is LOW and the SiC MOSFET is OFF. Therefore, if XEN and the PWM input signals are both HIGH, a fault condition is detected and can be digitally assigned to take whatever precautions might be desired. XEN can also be used as a control signal for cross−conduction prevention between a high−side and low−side switch used in a half or full−bridge configuration. The schematic diagram shown in Figure 32 illustrates a circuit example how to utilize the XEN signals for fault detection and cross−conduction prevention. As can be seen in this implementation, the functions are independent and it is up to the designer to decide whether any one or both functions are needed to be implemented in the system.

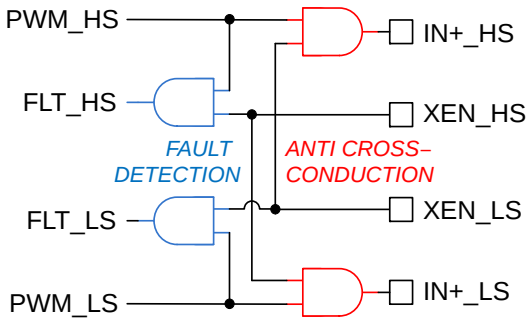

Figure 32. Examples of XEN Signal Usage

If XEN_HS transitions from LOW to HIGH while PWM_HS is HIGH, the PWM pulse width had been terminated early by one of the protection functions of the NCV51705. The protection function are; any of the Under Voltage Lock−Out (UVLO) protections, and Desaturation Detection (DESAT). As Figure 32 indicates a FAULT signal can be generated by a simple AND connection of the PWM input signal and the corresponding XEN output.

In case of cross−conduction prevention, the XEN signal of one driver is used to enable the operation of the other driver as depicted in a simplified manner in Figure 32. The isolation for the high side driver is not shown in the simplified schematic of Figure 32 but the operation of the system can be easily followed. While the high−side driver is ON, XEN_HS is LOW preventing any gate drive to be applied to the low−side driver. Once the high−side driver turns OFF its XEN_HS signal transitions to HIGH and the PWM_LS signal can pass through to the low−side driver. An identical sequence exists to ensure that the high−side driver cannot be turned ON until the low−side driver is OFF.

Signal Ground (SGND) and Power Ground (PGND)

Signal ground connection (SGND) is the GND for all control

starts when V_{DD} > 7.5 V. Additionally, the V_{EE} voltage rail includes an internally fixed under−voltage lockout (UVLO)

The configurability of the VEESET pin is summarized in Table 11.

Table 11. SUMMARY OF VEESET PIN CONFIGURATION

VEESET	COMMENT	V_{EE}	$V_{EE(UVLO)}$
V_{DD}	10.5 V<VEESET<V_{DD}	−8 V	

characteristic curves. Because the on−resistance of a SiC MOSFET dramatically increases even for a slight decrease in V_{GS}, the allowable UVLO hysteresis must be small. For this reason, the NCV51705 has a fixed 1 V hysteresis so that the turn−

D_1. Because the drain voltage on the SiC MOSFET sees extremely high dV/dt, the current through the p−n junction capacitance of D_1 can become very high if R_1 is not sized appropriately. Therefore, selecting a fast, high−voltage diode with lowest junction capacitance should be a priority. Typical values for R_1 will be near the range of 5 kΩ<R_1<10 kΩ but this can vary according to the I_D and R_{DS} parameters of the selected SiC MOSFET. If R_1 is much smaller than 5 kΩ, the instantaneous current into the DESAT pin can be hundreds of milliamps, which is problematic to the 400 μA internal DESAT current source. Conversely, if R_1 is much larger than 10 kΩ, a *RC* delay ensues as a product of R_1 and the junction capacitance of D_1. The delay can be on the order of few μs, resulting in an additional delay time responding to an over current condition.

5 V Bias (V5V)

This is the bypass capacitor pin for the internal 5 V bias rail powering the control circuitry. The recommended capacitor value is 2.2 μF. At least a 1 μF, good−quality, high−frequency, ceramic capacitor should be placed in close proximity to the pin. A smaller ceramic capacitor value such as 100 nF will assure stability but may result in a 500 mV overshoot on the 5 V rail during start−up. The 5 V rail starts to rise approximately 30 μs after V_{DD} is applied. Once the 7 V threshold is exceeded at the VDD pin, the 5 V rail is enabled. The V5V pin can source up to 10 mA making it suitable for use as a low power bias supply for housekeeping circuits such as open collector pull−up, optocoupler or digital isolator bias.

PCB Guideline