Isolated High Current IGBT Gate Driver

NCV57001

NCV57001 is a high−current single channel IGBT driver with internal galvanic isolation, designed for high system efficiency and reliability in high power applications. Its features include complementary inputs, open drain FAULT and Ready outputs, active Miller clamp, accurate UVLOs, DESAT protection, and soft turn−off at DESAT. NCV57001 accommodates both 5 V and 3.3 V signals on the input side and wide bias voltage range on the driver side including negative voltage capability. NCV57001 provides > 5 kVrms (UL1577 rating) galvanic isolation and > 1200 V_{IORM} (working voltage) capabilities. NCV57001 is available in the wide−body SOIC

PIN DESCRIPTION

Pin Name	No.	I/O	Description
V_{EE2A}	1	Power	Output side negative power supply. A good quality bypassing capacitor is required from these pins to GND2 and should be placed close to the pins for best results. Connect it to GND2 for unipolar supply application.
V_{EE2}			

SAFETY AND INSULATION RATINGS

Symbol	Parameter		Min	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1 Rated Mains Voltage	< 150 V_{RMS}	I − IV	
		< 300 V_{RMS}	I − IV	
		< 450 V_{RMS}	I − IV	
		< 600 V_{RMS}	I − IV	
		< 1000 V_{RMS}	I − III	
CTI	Comparative Tracking Index (DIN IEC 112/VDE 0303 Part 1)		600	
	Climatic Classification		40/100/21	
	Polution Degree (DIN VDE 0110/1.89)		2	
V_{PR}	Input−to−Output Test Voltage, Method b, V_{IORM} x 1.875 = V_{PR}, 100% Production Test with tm = 1 s, Partial Discharge < 5 pC		2250	V_{pk}
	Input−to−Output Test Voltage, Method a, V_{IORM} x 1.6 = V_{PR}, Type and Sample Test with tm = 10 s, Partial Discharge < 5 pC		−	V_{pk}
V_{IORM}	Maximum Repetitive Peak Voltage		1200	V_{pk}
V_{IOWM}	Maximum Working Insulation Voltage		870	V_{RMS}
V_{IOTM}	Highest Allowable Over Voltage		8400	V_{pk}
E_{CR}	External Creepage		8.0	mm
E_{CL}	External Clearance		8.0	mm
DTI	Insulation Thickness		17.3	um
T_{Case}				

ABSOLUTE MAXIMUM RATINGS (Over operating free−

OPERATING RANGES (Note 6)

Symbol	Parameter	Min	Max	Unit
V_{DD1}−GND1	Supply voltage, input side	UVLO1	5.5	V
V_{DD2}−GND2	Positive Power Supply, output side	UVLO2	24	V
V_{EE2}−GND2	Negative Power Supply, output side	−10	0	V
V_{DD2}−V_{EE2} (V_{MAX2})	Differential Power Supply, output side	0	24	V
V_{IL}	Low level input voltage at IN+, IN−, /RST	0		

ELECTRICAL CHARACTERISTICS (V_{DD1} = 5 V, V_{DD2} = 15 V, V_{EE2} = −8 V. For typical values T_A = 25°

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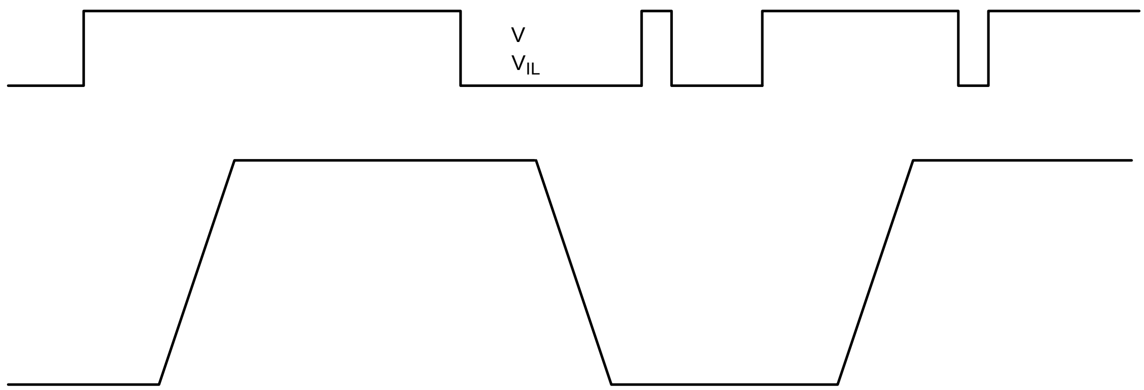
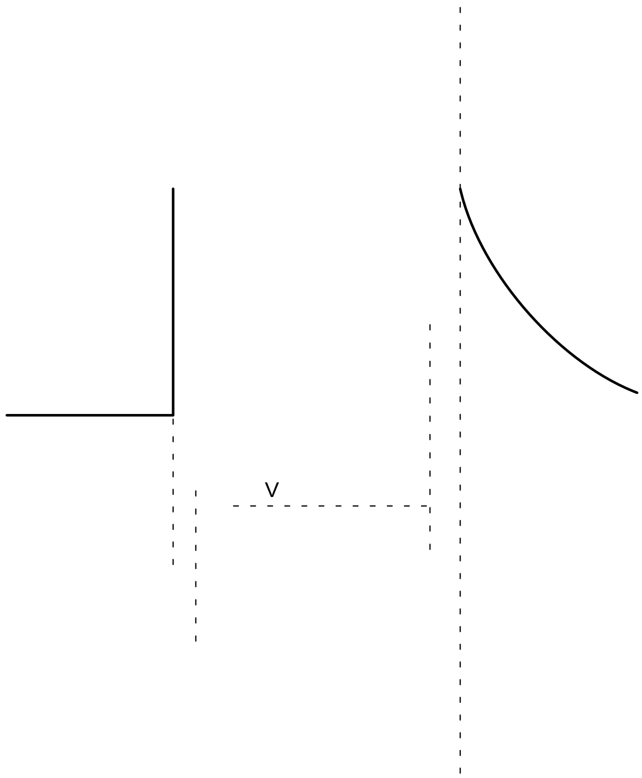
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS						
t_{PD-ON}	IN+, IN− to Output High Propagation Delay	C_{LOAD} = 10 nF V_{IH} to 10% of output change for PW > 150 ns. OUT and CLAMP pins are connected together	40	60	90	ns
t_{PD-OFF}	IN+, IN− to Output Low Propagation Delay	C_{LOAD} = 10 nF V_{IL} to 90% of output change for PW > 150 ns. OUT and CLAMP pins are connected together				


V
V_IL


V

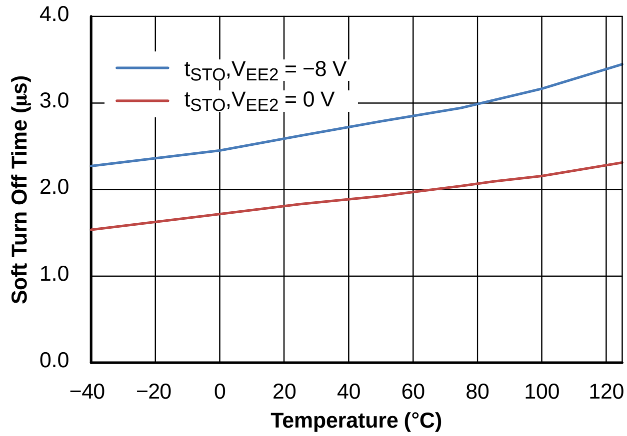


Figure 18. Soft Turn Off Time

FEATURE DESCRIPTIONS

Under Voltage Lockout (UVLO)

UVLO ensures correct switching of IGBT connected to the driver output.

- The IGBT is turned−off, if the supply V_{CC1} drops below $V_{UVLO1-OUT-OFF}$ and the RDY pin output goes to low.
- The driver output does not start to react to the input signal on V_{IN} until the V_{CC1} rises above the $V_{UVLO1-OUT-ON}$ again. If the supply V_{CC1} increase over $V_{UVLO1-OUT-ON}$, the RDY pin output goes to be open−drain and outputs continue to switch IGBT
- The IGBT is turned−off, if the supply V_{CC2} drops below $V_{UVLO2-OUT-OFF}$ and the RDY pin output goes to low.
- The driver output does not start to react to the input signal on V_{IN} until the V_{CC1} rises above the $V_{UVLO1-OUT-ON}$ again. If the supply V_{DD1} increases over $V_{UVLO1-OUT-ON}$, the RDY pin output goes to be open−drain and outputs continue to switch IGBT
- VEE2 is not monitored.

Figure 19. UVLO Diagram

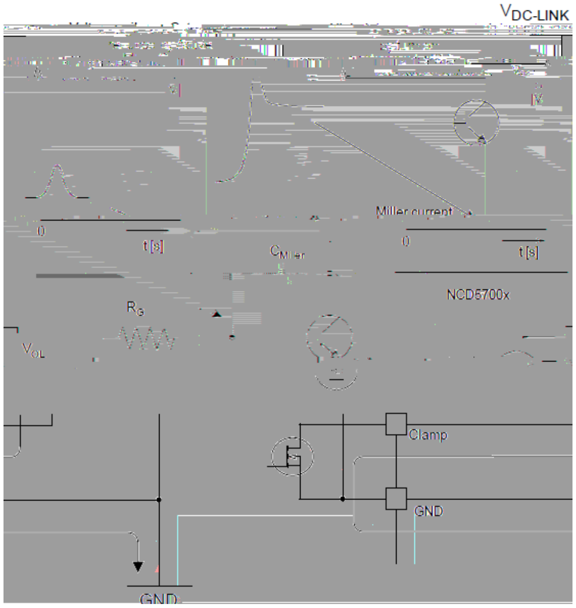


Figure 20. Current Path without Miler Clamp Protection

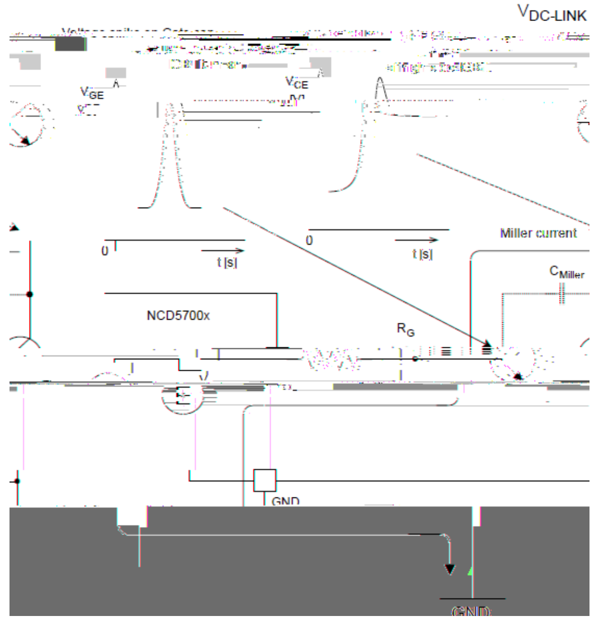


Figure 21. Current Path with Miler Clamp Protection

Non−inverting and Inverting Input Pin (IN+, IN−)

NCV57001 has two possible input modes to control IGBT. Both inputs have defined minimum input pulse width to filter occasional glitches.

- Non−inverting input IN+ controls the driver output while inverting input IN− is set to LOW
- Inverting input IN− controls the driver output while non−inverting input IN+ is set to HIGH

Desaturation Protection (DESAT)

Desaturation protection ensures the protection of IGBT at short circuit. When the V_{CESAT} voltage goes up and reaches the set limit, the output is driven low and /FLT output is activated. Blanking time can be set by internal current source and an external capacitor. To avoid false DESAT triggering and minimize blanking time, fast switching diodes with low internal capacitance are recommended. All DESAT protective diodes internal capacitances builds voltage divider with the blanking capacitor.

DESAT Circuit Parameters Specification

$$t_{BLANK} = C_{BLANK} \cdot \frac{V_{DESAT-THR}}{I_{DESAT-CHG}}$$

$$V_{DESAT-THR} > R_{S-DESAT} \cdot I_{DESAT-CHG} + V_{F\ HV\ diode} + V_{CESAT\_IGBT}$$

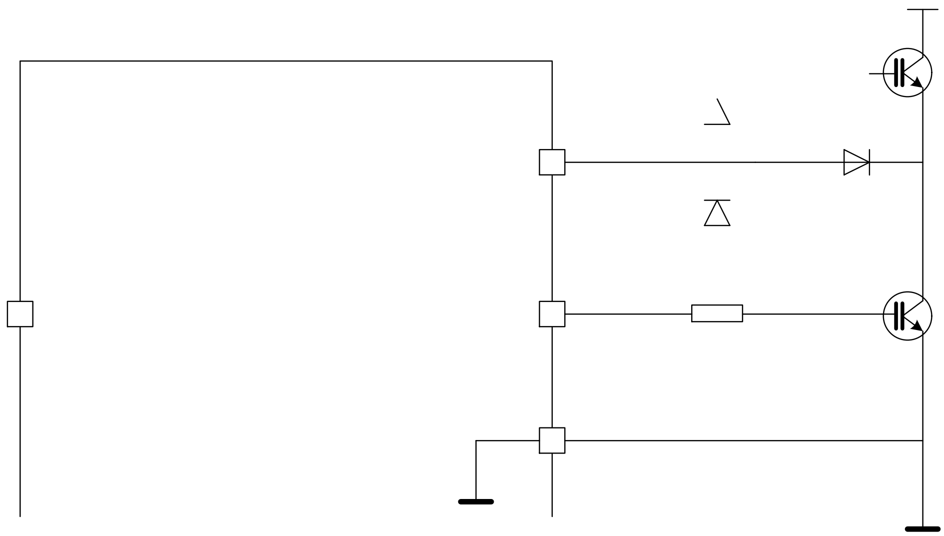


Figure 22. DESAT Protection Schematic

Fault Output Pin (FLT)

FLT open−drain output provides feedback to the controller about driver DESAT protection conditions. The open−drain FLT outputs of multiple NCV57001 devices can be wired together forming a single, common fault bus for interfacing directly to the microcontroller. FLT output has 50kΩ internal pull−up resistor to VDD1.

Ready Output Pin (RDY)

RDY open−drain output provides feedback to the controller about driver UVLO and TSD protections conditions.

- If either side of device have insufficient supply (VDD1 or VDD2), the RDY pin output goes low; otherwise, RDY pin output is open drain.
- If the temperature crosses the TSD threshold, the RDY pin output goes low; otherwise, RDY pin output is open drain.

The open−drain RDY outputs of multiple NCV57001 devices can be "OR"ed together.

Reset Input Pin (RST)

Reset input pin has internal pull−up resistor to VDD1. In normal condition the RST pin is connected to HIGH, to reset FAULT conditions connect RST pin to LOW. In applications that does not allow to control the reset, RST pin should be connected to IN+, the driver will be reset by each input pulse.

RESET Input

- FLT input is used to set back FLT output after DESAT conditions disappear

Power Supply (VDD1, VDD2, VEE2)

NCV57001 is designed to support two different power supply configurations, bipolar or unipolar power supply. For reliable high output current the suitable external power capacitors required. Parallel combination of 100 nF + 4.7 μF ceramic capacitors is optimal for a wide range of applications using IGBT. For reliable driving IGBT modules (containing several parallel IGBT's) is a higher capacity required (typically 100 nF + 10 μF). Capacitors should be as close as possible to the driver's power pins.

- In bipolar power supply the driver is typically supplied with a positive voltage of 15 V at VDD2 and negative voltage −5 V at VEE2 (Figure 24). Negative power supply prevents a dynamic turn on throughout the internal IGBT input capacitance.
- In Unipolar power supply the driver is typically supplied with a positive voltage of 15 V at VDD2. Dynamic turn on throughout the internal IGBT input capacitance could be prevented by Active Miler Clamp function. CLAMP output should be directly connected to IGBT gate (Figure 25).

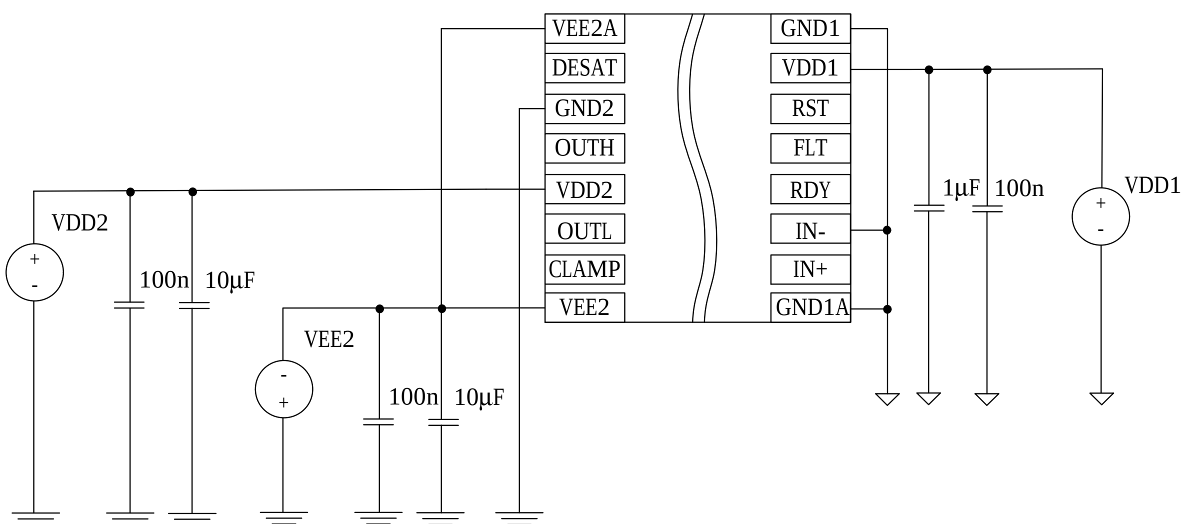


Figure 24. Bipolar Power Supply

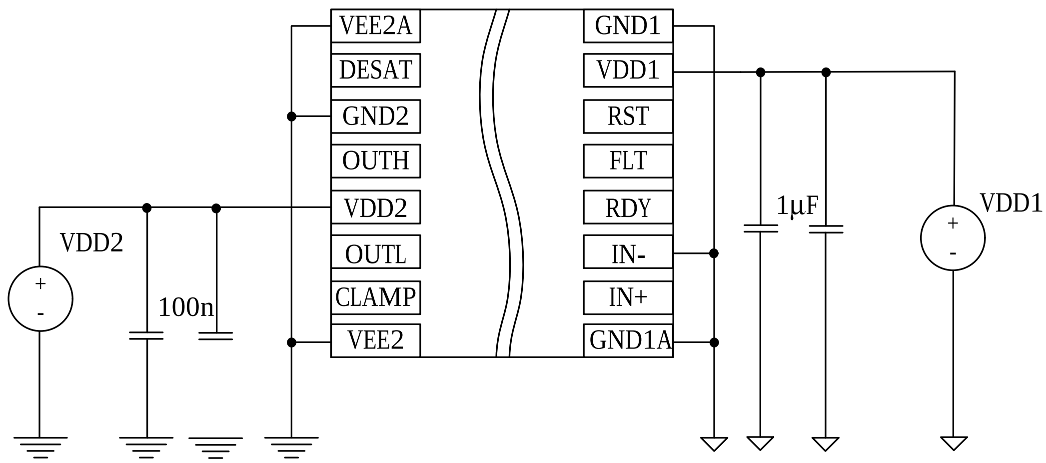


Figure 25. Unipolar Power Supply

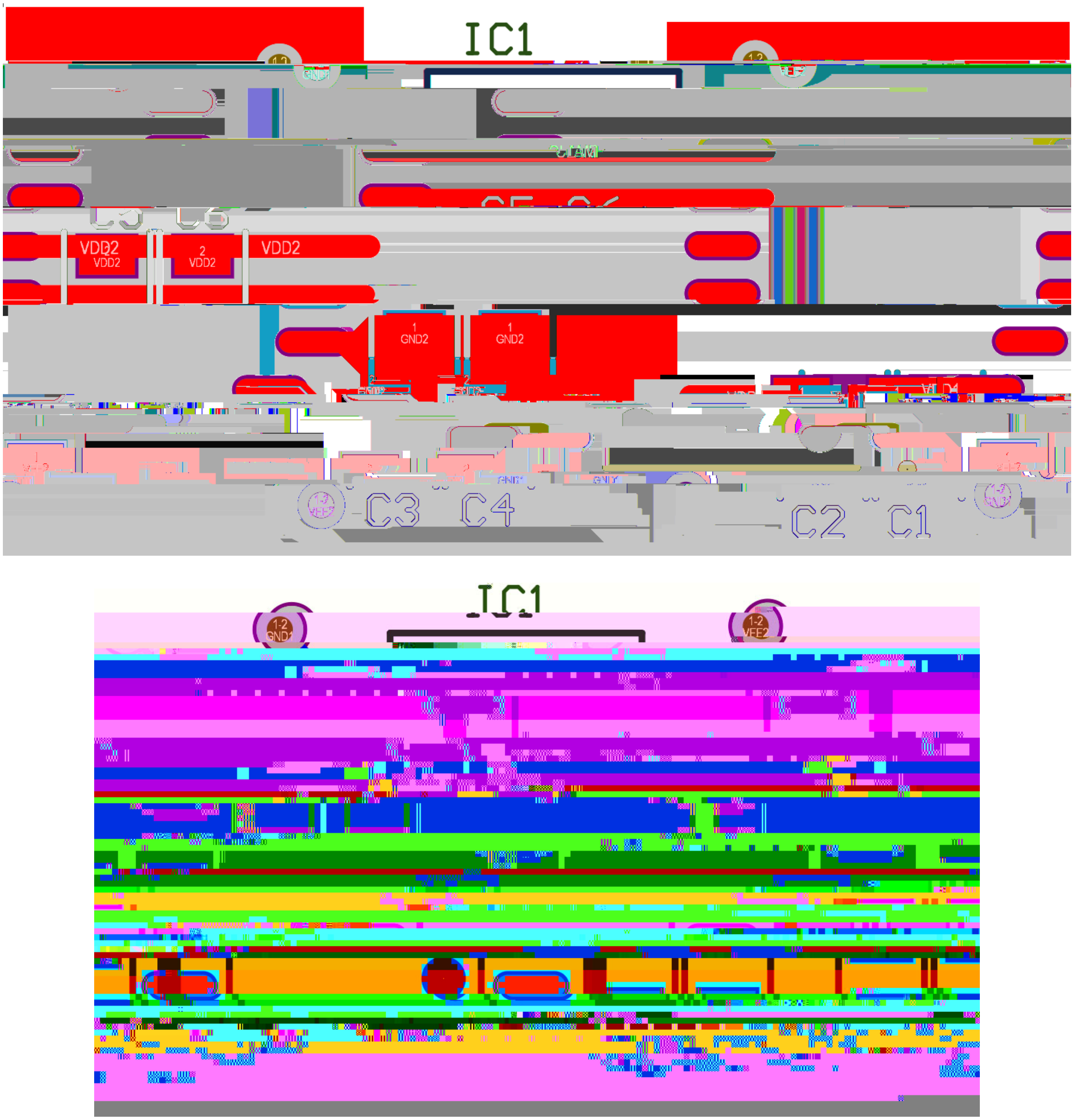
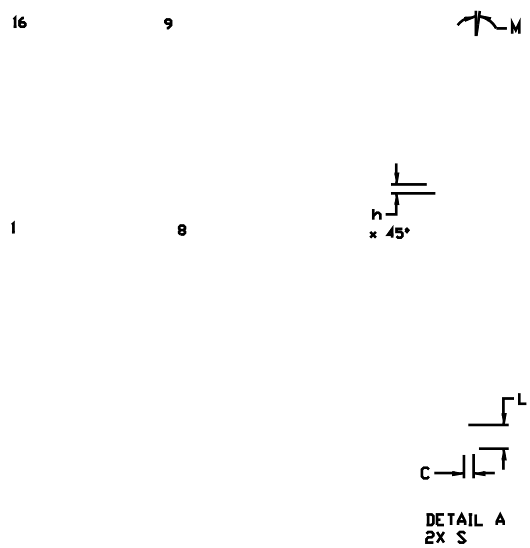


Figure 27. Recommended Basic Bipolar Power Supply PCB Design

SOIC



−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.