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Figure 1. Simplified Block Diagram

Symbol	Parameter	Min	Unit	
	Installation Classifications per DIN VDE 0110/1.89 Table 1 Rated Mains Voltage	< 150 V _{RMS}	I – IV	
		< 300 V _{RMS}	I – IV	
		< 450 V _{RMS}	I – IV	
		< 600 V _{RMS}	I – IV	
		< 1000 V _{RMS}	I – III	
СТІ	Comparative Tracking Index (DIN IEC 112/VDE 0303 Part 1)	600		
	Climatic Classification	40/100/21		
	Polution Degree (DIN VDE 0110/1.89)	2		
V _{PR}	Input-to-Output Test Voltage, Method b, $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with tm = 1 s, Partial Discharge < 5 pC		2250	V _{pk}
	Input–to–Output Test Voltage, Method a, $V_{IORM} \times 1.6 = V_{PR}$, Type and Sample Test with tm = 10 s, Partial Discharge < 5 pC			V _{pk}
VIORM	Maximum Repetitive Peak Voltage	1200	V _{pk}	
V _{IOWM}	Maximum Working Insulation Voltage	870	V _{RMS}	
V _{IOTM}	Highest Allowable Over Voltage	8400	V _{pk}	
E _{CR}	External Creepage	8.0	mm	
E _{CL}	External Clearance		8.0	mm
DTI	Insulation Thickness	17.3	um	
T _{Case}	Safety Limit Values – Maximum Values in Failure; Case Temperature	150	°C	
P _{S,INPUT}	Safety Limit Values – Maximum Values in Failure; Input Power	36	mW	
P _{S,OUTPUT}	Safety Limit Values – Maximum Values in Failure; Output Power	1364	mW	
R _{IO}	Insulation Resistance at TS, V _{IO} = 500 V	10 ⁹	Ω	

Table 2. SAFETY AND INSULATION RATINGS

Table 3. ABSOLUTE MAXIMUM RATINGS (Note 1) Over operating free-air temperature range	e unless otherwise noted
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Symbol	Parameter	Minimum	Maximum	Unit
V _{DD1} -GND1	V _{DD1} -GND1 Supply voltage, input side		6	V
V				

Table 5. OPERATING RANGES (Note 6)

Symb	ol	Parameter	Min	Max	Unit
V _{DD1} –G	ND1		·		

Table 6. ELECTRICAL CHARACTERISTICS ($V_{DD1} = 5 V$, $V_{DD2} = 15 V$, $V_{EE2} = -8 V$.) (continued)For typical values $T_A = 25^{\circ}C$, for min/max values, T_A is the operating ambient temperature range that applies, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit	
LOGIC INPUT AND OUTPUT							
V _{IL}	IN+, IN-, RST Low Input Voltage				$0.3 \times V_{DD1}$	V	
V _{IH}	IN+, IN-, RST High Input Voltage		$0.7 \times V_{DD1}$			V	
V _{IN-HYST}	Input Hysteresis Voltage			0.15 × V _{DD1}		V	
I _{IN-L} , I _{RST-L}	IN–, \overline{RST} Input current (50 k Ω pull–up resistor)	V _{IN} _/V _{RST} = 0 V		-100		μΑ	
I _{IN+H}	IN+ Input Current (50 kΩ pull-down resistor)	V _{IN+} = 5 V		100		μΑ	
I _{RDY-L} , I _{FLT-L}	RDY, FLT Pull–up Current (50 kΩ pull–up resistor)	V _{RDY} /V _{FLT} = Low		100		μΑ	
V _{RDY-L} , V _{FLT-L}	RDY, FLT Low Level Output Voltage	$I_{RDY}/I_{FLT} = 5 \text{ mA}$			0.3	V	
t _{ON-MIN1}	Input Pulse Width of IN+, IN– for No Response at Output				10	ns	
t	ï for	-	-	-	- '	-	

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Figure 5. UVLO Waveform

FEATURE DESCRIPTIONS

Under Voltage Lockout (UVLO)

UVLO ensures correct switching of IGBT connected to the driver output.

- The IGBT is turned–off, if the supply V_{CC1} drops below V_{UVLO1–OUT–OFF} and the RDY pin output goes to low.
- The driver output does not start to react to the input signal on V_{IN} until the V_{CC1} rises above the V_{UVLO1-OUT-ON} again. If the supply V_{CC1} increase over V_{UVLO1-OUT-ON}, the RDY pin output goes to be open-drain and outputs continue to switch IGBT
- The IGBT is turned–off, if the supply V_{CC2} drops below $V_{UVLO2-OUT-OFF}$ and the RDY pin output goes to low.
- The driver output does not start to react to the input signal on V_{IN} until the V_{CC1} rises above the V_{UVLO1-OUT-ON} again. If the supply V_{DD1} increases over V_{UVLO1-OUT-ON}, the RDY pin output goes to be open-drain and outputs continue to switch IGBT
- VEE2 is not monitored.



Figure 6. UVLO Diagram



Figure 7. Current Path without Miler Clamp Protection

Non inverting and Inverting Input Pin (IN+, IN)

NCV57001F has two possible input modes to control IGBT. Both inputs have defined minimum input pulse width to filter occasional glitches.

- Non-inverting input IN+ controls the driver output while inverting input IN- is set to LOW
- Inverting input IN- controls the driver output while non-inverting input IN+ is set to HIGH

<u>Warning</u>: When the application use an independent or separate power supply for the control unit ant the input side of the driver, all inputs should be protected by a serial resistor (In case of a power failure of the driver, the driver may be damaged due to overloading of the input protection circuits)



Figure 8. Current Path with Miler Clamp Protection

Desaturation Protection (DESAT)

Desaturation protection ensures the protection of IGBT at short circuit. When the V_{CESAT} voltage goes up and reaches the set limit, the output is driven low and /FLT output is activated. Blanking time can be set by internal current source and an external capacitor. To avoid false DESAT triggering and minimize blanking time, fast switching diodes with low internal capacitance are recommended. All DESAT protective diodes internal capacitances builds voltage divider with the blanking capacitor.

<u>Warning</u>: Both external protective diodes are recommended for the protection against voltage spikes caused by IGBT transients passing through parasitic capacitances.

DESAT Circuit Parameters Specification

 $t_{BLANK} = C_{BLANK} \cdot \frac{V_{DESAT-THR}}{I_{DESAT-CHG}}$

 $V_{\text{DESAT-THR}} > R_{\text{S-DESAT}} \cdot I_{\text{DESAT-CHG}} + V_{\text{F HV diode}} + V_{\text{CESAT_IGBT}}$

Fault Output Pin (FLT)

FLT open-drain output provides feedback to the controller about driver DESAT protection conditions. The open-drain FLT outputs of multiple NCV57001F devices can be wired together forming a single, common fault bus for interfacing directly to the microcontroller. FLT output has $50k\Omega$ internal pull-up resistor to VDD1.

Ready Output Pin (RDY)

RDY open-drain output provides feedback to the controller about driver UVLO and TSD protections conditions.

- If either side of device have insufficient supply (VDD1 or VDD2), the RDY pin output goes low; otherwise, RDY pin output is open drain.
- If the temperature crosses the TSD threshold, the RDY pin output goes low; otherwise, RDY pin output is open drain.

The open-drain RDY outputs of multiple NCV57001F devices can be "OR"ed together.

Reset Input Pin (RST)

Reset input pin has internal pull–up resistor to VDD1. In normal condition the RST pin is connected to HIGH, to reset FAULT conditions or disable output pulses connect RST pin to LOW. In applications that does not allow to control the reset,

Y



Figure 13. Common Mode Transient Immunity Test Circuit





ORDERING INFORMATION

Device	Package	Shipping [†]
NCV57001FDWR2G*	SOIC-16 Wide Body (Pb-Free)	1,000 / Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable.

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-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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