Ideal Diode NMOS Controller

NCV68061

The NCV68061 is a Reverse Polarity Protection and Ideal Diode NMOS Controller, intended as a lower loss and lower forward voltage replacement for power rectifier diodes. The controller operates in conjunction with an N channel MOSFET for low power loss.

The main function of the NCV68061 is to control the ON/OFF state of the external NMOS according to the Source to Drain differential voltage polarity.

Depending on the Drain pin connection, the device can be configured as two different application modes. With the Drain pin connected to the load, the application is in Ideal Diode mode, whereas with the Drain pin connected to ground, the application is merely in Reverse Polarity Protection mode.

Features

- Operating Voltage Range: up to 32 V
- Immune to 60 V Load Dump Pulse
- Immune to 40 V Negative Transient
- Ideal Diode Function
  - Protecting against Reverse Current Flow (from Output to Input)
- Reverse Polarity Protection (RPP) Function
  - Protecting against Negative Supply
- Enable Function (3.3 V Logic Compatible Thresholds)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC Q100 Grade 1 Qualified and PPAP Capable
- These Devices are Pb Free and are RoHS Compliant

Typical Applications

- Automotive Battery Regulation
- Industrial Power Supply
- Power Supply OR ing Application
- Rectifier

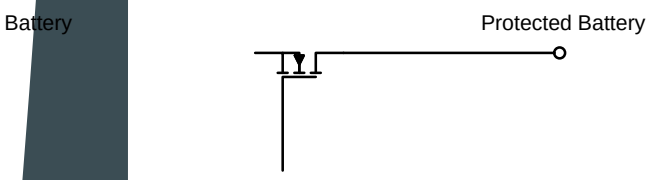


Figure 1. NCV68061 Application Schematic (Ideal Diode)

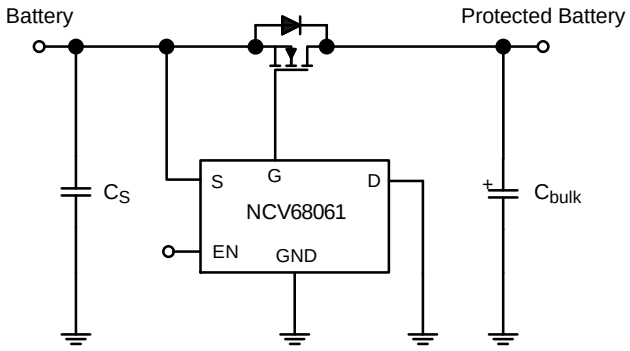


Figure 2. NCV68061 Application Schematic (Reverse Polarity Protection)

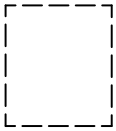


Figure 3. NCV68061 Block Diagram

Table 2. MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Source Voltage DC (Note 1)	V_S	−18	45	V
Source, Drain, Gate and Enable Voltage (Note 2) Load Dump − Suppressed	U_{S*}	−	60	V
Source, Gate and Enable Voltage (Note 3) Test Pulse 1	U_S	−40	−	V
Gate Voltage	V_G	−18	45	V
Gate to Source Voltage	V_{GS}	−0.3	19	V
Drain Voltage	V_D	−5	45	V
Source to Drain Voltage DC	V_{SD}	−45	45	
Source to Drain Voltage transient (Test Pulse 1)	V_{SD}	−60	−	
Enable Voltage	V_{EN}	−18	45	V
Operating Junction Temperature	T_J	−40	150	°C
Storage Temperature	T_{STG}	−55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. Load Dump Test B (with centralized load dump suppression) according to ISO 16750−2 standard. Guaranteed by design. Not tested in production. Passed Class A according to ISO 16750−1.
3. Test Pulse 1 according to ISO 7637−2 standard. Guaranteed by design. Not tested in production. Passed Class A according to ISO 16750−1. More ISO 7637−2: 2011(E) PULSE TEST RESULTS are in Table 8.

Table 3. ESD CAPABILITY (Note 4)

Rating	Symbol	Min	Max	Unit
ESD Capability, Human Body Model	ESD_{HBM}	−2	2	kV
ESD Capability, Charged Device Model	ESD_{CDM}	−1	1	kV

4. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JS−001−2017)
   Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes smaller than 2×2 mm due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS−002−2018.

Table 4. LEAD SOLDERING TEMPERATURE AND MSL (Note 5)

Rating	Symbol	Min	Max	Unit
Moisture Sensitivity Level	MSL	1		−

5. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Table 5. THERMAL CHARACTERISTICS (Note 6)

Rating	Symbol	Value	Unit
Thermal Characteristics, TSOP−6 Thermal Resistance, Junction−to−Ambient Thermal Reference, Junction−to−Case Top	 $R_{\theta JA}$ $\Psi_{\theta JT}$	 199.1 57.3	°C/W

6. Mounted onto a 80 x 80 x 1.6 mm single layer FR4 board (645 sq mm, 1 oz. Cu, steady state).

Table 6. RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Source Voltage	V_S	3	32	V
Junction Temperature	T_J	−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 7. ELECTRICAL CHARACTERISTICS
(V_S = 13.5 V, V_{EN} = 5 V, C_S = 0.1 μF, C_{bulk} = 1 μF, Min and Max values are valid for temperature range −40°C ≤ T_J ≤ +150°C unless noted otherwise and are guaranteed by test, design or statistical correlation. Typical values are referenced to T_J = 25°C)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
CHARGE PUMP OPERATION						
Undervoltage Lockout	V_S rising V_S falling (Gate Discharge)	V_{S_UVLO}	– 3	3.3 3.2	3.5 –	V
Gate to Source Charged Voltage	V_S = 4 V V_S ≥ 8 V	V_{GS}	3 9	4.0 11.4	– 15	V
Source to Drain Voltage Threshold Gate Charge Gate Discharge	 V_{SD} rising V_{SD} falling	$V_{th(SD)}$	 100 −40	 140 −10	 220 0	mV
Gate Charge Current	V_{GS} = 0 V, V_{SD} = 220 mV V_S = 4 V V_S = 13.5 V	I_{G_Charge}	 70 170	 105 325	 – –	μA
Gate Discharge Peak Current	V_{GS} = 10 V, V_{SD} ≤ −100 mV	I_{G_Disch}	–	1.85	–	A
Discharge Switch $R_{DS(on)}$	V_{GS} = 100 mV, V_{SD} ≤ −100 mV	$R_{DS(on)}$	1	2.2	5	Ω
Response Time (Time from Reverse Voltage Condition to V_{GS} = 9 V)	V_{GS} = 10 V, V_S = 13.5 V, V_{SD} = step from 250 mV to −150 mV	t_{rt_OFF}	–	0.2	0.6	μs
Gate to Source Static Resistance			–	1.05	–	MΩ
DISABLE AND QUIESCENT CURRENTS						
Disable Current	V_{EN} = 0 V	I_{DIS}	–	–	5	μA
Quiescent Current	I_G = 0 mA, V_{SD} = 220 mV (CP active)	I_q	–	215	295	μA
ENABLE						
Enable Input Threshold Voltage Logic Low Logic High	 V_{GS} ≤ 0.1 V V_{GS} ≥ 4.9 V	$V_{th(EN)}$	 0.99 –	 1.55 1.70	 – 2.31	V
Enable Input Current Logic High Logic High Logic Low	 V_{EN} = 13.5 V V_{EN} = 5 V V_{EN} = 0 V	 I_{EN_ON} I_{EN_ON} I_{EN_OFF}	 – – –	 12 3.5 0.010	 – 5 1	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

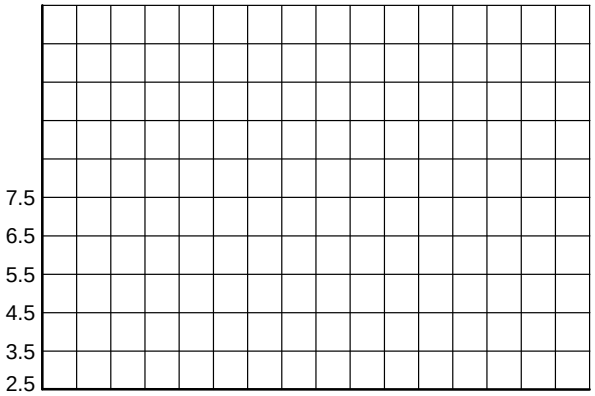


Figure 4. Gate−to−Source Charged Voltage vs. Source Voltage

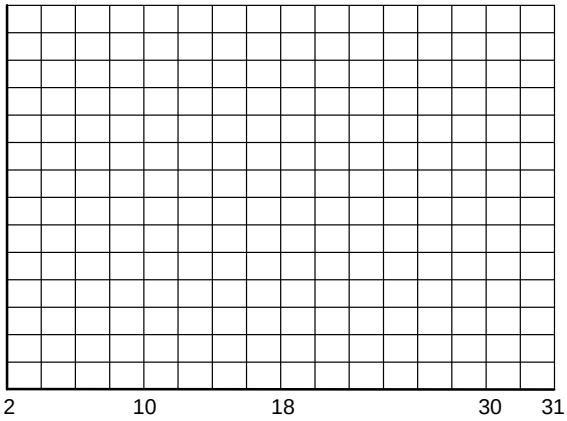
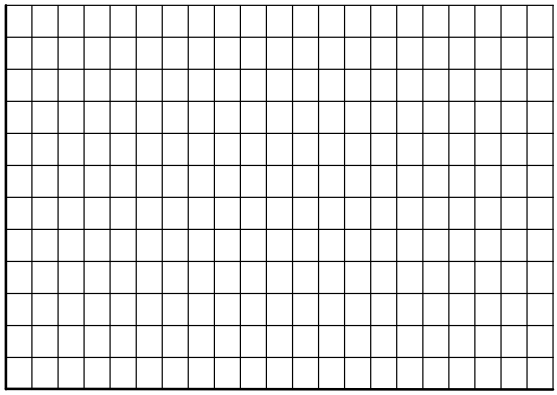
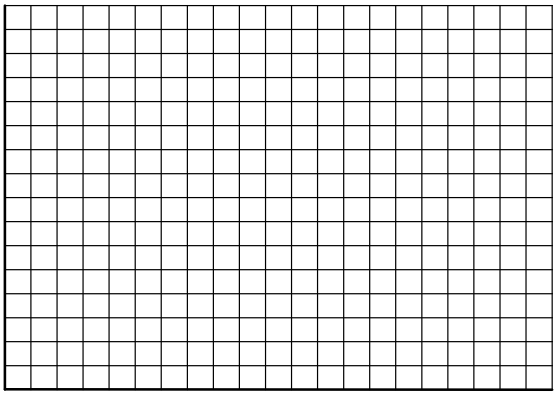
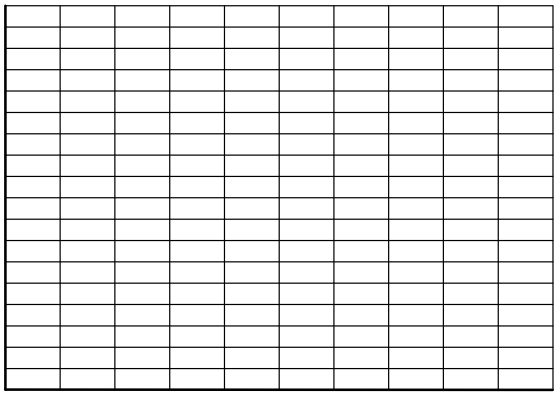
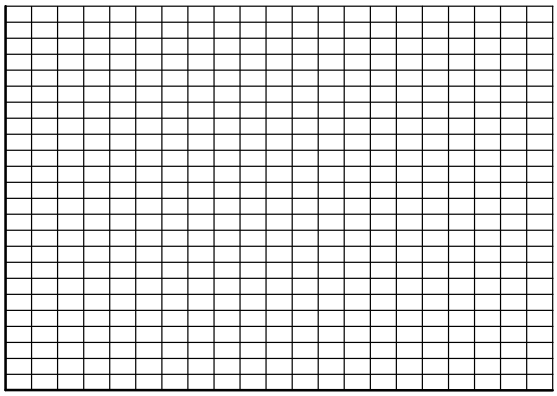


Figure 5. Gate Charge Current vs. Source Voltage









APPLICATION INFORMATION
Integrated Circuit and Block Diagram Description

Integrated Circuit Description

The NCV68061 operates in conjunction with an external NMOS transistor. Two basic applications can be configured. An

APPLICATION INFORMATION

Operation

The main function of the NCV68061 is to control the ON/OFF state of an external NMOS transistor depending on the difference between the voltages at the NCV68061 Source and Drain pins as shown in Figures 1 and 2. Figure 3 illustrates the internal connections between the functional blocks described above.

When the Enable input is low, the IC is in disable mode. All the internal blocks are turned OFF, and the current consumption is reduced typically down to tens of nano amps. In this state, the external transistor is kept OFF by an integrated 1 MΩ resistor between the Gate and Source pins.

When the Enable input is high, the IC is active. Further operation depends on the output state of the UVLO and Source/Drain comparators. Table 10 shows the charge pump, gate discharge, and NMOS transistor states resulting from the 4 possible output states of these comparators. The charge pump is turned ON only when the Source voltage level is above both the UVLO threshold and above the Drain voltage level.

Undervoltage Lockout: When the Source voltage falls below the UVLO thresholds (typ. 3.2 V), the charge pump is disabled and the external NMOS transistor is turned OFF by an internal PMOS transistor. By decreasing the Source voltage further, the chip is insufficiently powered, and the external NMOS is kept in OFF state by the integrated 1 MΩ resistor (see Figure 3).

Application Configurations

Ideal Diode

In the Ideal Diode configuration (Figure 1), the input voltage is not allowed to discharge the output.

Prior to entering the conduction mode, the Source voltage is lower than the Drain voltage, and the charge pump and the NMOS transistor are disabled. As Source voltage becomes greater than Drain voltage, forward current flows through the body diode of the NMOS transistor. Once this forward voltage drop exceeds the Source to Drain Gate Charge Voltage Threshold level (typ. 140 mV), the charge pump is turned ON and the NMOS transistor becomes fully conductive.

When the Source voltage becomes less than the Drain voltage, reverse current initially flows through the conductive channel of the NMOS transistor. This current creates a voltage drop across the conductive channel of the NMOS transistor which is proportional to its $R_{DS(ON)}$ resistance. When this voltage crosses below the Source to Drain Gate Discharge Voltage Threshold (typ. 10 mV), the charge pump is disabled and the external NMOS transistor is turned OFF by an internal PMOS transistor (see Figure 3).

Reverse Polarity Protection (RPP)

By connecting the Drain pin to the GND potential (Figure 2), the NCV68061 does not allow a falling input voltage to discharge the output below GND potential, but does allow the output to follow any positive input voltage above the UVLO threshold. When Source voltage is above the UVLO threshold (typ. 3.3 V), the Source/Drain and UVLO comparators enable the Charge Pump to provide Gate Source voltage to the external NMOS transistor, which is fully conductive. For Source voltage below the UVLO threshold (typ. 3.2 V), the Charge Pump and the NMOS transistor are disabled, and any load current flows through the body diode of the NMOS transistor.

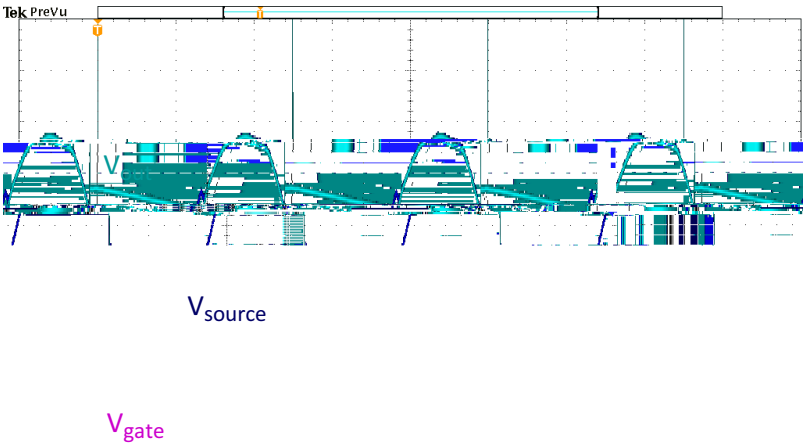


Figure 18. Application Response to 13.5 V + 5 Vpp Sine Wave on the Input (V_{Source}) – Ideal Diode Application (see Figure 1)

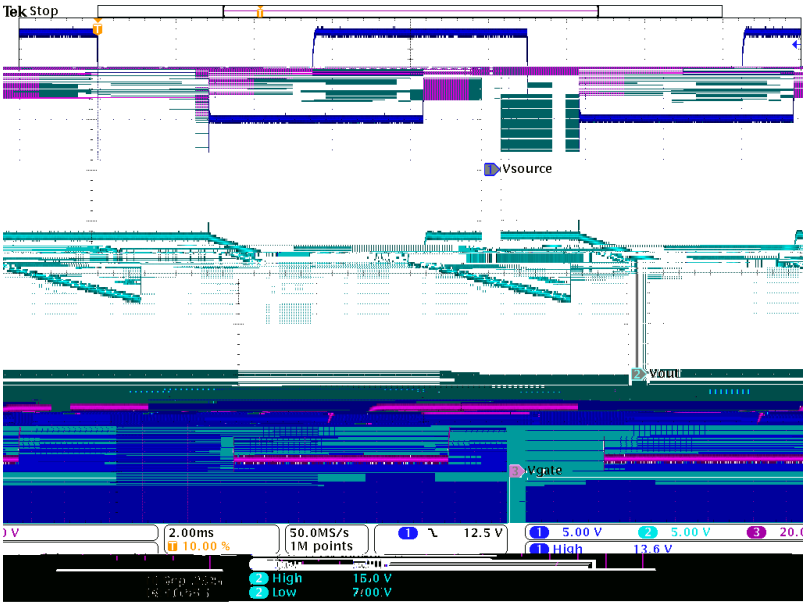


Figure 19. Application Response to Transient on the Input (V_{Source}) from 13.5 V to 5 V – Ideal Diode Application (see Figure 1)

NCV68061

C_S (Input) Capacitor Considerations

For proper device performance, it is recommended that a 0.1 μF ceramic capacitor be placed as close as possible to the NCV68061, and connected with the shortest possible traces.

C_{bulk} (Output) Capacitor Considerations

Besides presenting a sufficiently low impedance for the load input rail, in an Ideal Diode application the C_{bulk} capacitance should be high enough to maintain adequate voltage while providing load current for the duration of battery sag plus the charge from reverse current spike before the NMOS transistor turns off. Capacitor ESR is also limited by the $R_{DS(ON)}$ of the NMOS, as high ESR can reduce

TSOP−6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

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NOTES:
1. DIMENSIONING AND TOLERAN

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GENERIC
MARKING DIAGRAM*

XXX = Specific Device Code
A =Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O