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DATA SHEET







Figure 4. NCV68261 Application Schematic (Reverse Polarity Protection + High Side Switch)



GND Figure 5. NCV68261 Block Diagram



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NCV68261

# **TYPICAL CHARACTERISTICS**





Figure 6. Gate-to-Source Charged Voltage vs. Input Voltage

-		 	 	 	 	 	 			



#### Figure 7. Gate Charge Current vs. Input Voltage





# **TYPICAL CHARACTERISTICS**



V<sub>IN</sub>, INPUT VOLTAGE (V)

Figure 12. Quiescent Current vs. Input Voltage







#### Figure 13. Quiescent Current vs. Temperature







#### **TYPICAL CHARACTERISTICS**





#### **TYPICAL CHARACTERISTICS**

#### Table 8. ISO 7637-2: 2011(E) PULSE TEST RESULTS

ISO 7637-2:2011(E) Test Pulse

#### **APPLICATION INFORMATION**

# INTEGRATED CIRCUIT AND BLOCK DIAGRAM DESCRIPTION

#### Integrated Circuit Description

The NCV68261 can operate in conjunction with one or two external NMOS transistors. Two basic applications can be configured: an Ideal diode application or a Reverse Polarity Protection application defined by the Drain pin connection as shown in the Table 9. The applications with single NMOS are always forward conductive. The applications with two NMOS transistors provide a High Side Switch function to control the power supplied to the application.

#### Enable

The Enable block turns the controller ON and OFF. If the

#### Operation

The main function of the NCV68261 is to control the ON/OFF state of one or two external NMOS transistors depending on the state of the Enable pin and the difference between the voltages at the Input and Drain pins – as shown in Figures 22 to 25. Figure 5 illustrates the internal connections between the functional blocks described above.

OFF state: When the Enable input is low, the IC is in disable mode. All the internal blocks are turned OFF, and the current consumption is reduced – typically down to tens of nano–amps. In this state, the external transistors are kept OFF by an integrated 1 M $\Omega$  resistor between the Gate and Source pins.

ON state: When the Enable input is high, the IC is active.

The Ideal Diode application in Figure 22 has rectifying properties as a common diode application, while reducing the forward voltage drop on the diode. Th application is in reverse mode as long as the Input voltage is lower than the Drain voltage.

The Ideal Diode + High Side Switch (HSS) application in Figure 23 combines the features of the Ideal Diode and an Ideal Switch depending on the Enable (EN) state. If the EN is high the application is in Ideal Diode mode. If the EN is low, the application behaves as an Ideal Switch and the protected battery line is disconnected from the battery line.

The **Reverse Polarity Protection** (RPP) application in Figure 24 protects the load from negative voltages at the battery line.

The Reverse Polarity Protection + High Side Switch application in Figure 25 combines the features of the RPP and HSS, similarly to the Ideal Diode + HSS.



Figure 22. Ideal Diode





Figure 26. Application Response to 13 V + 6 V<sub>pp</sub> Sine Wave on the Input (V<sub>IN</sub>) – Ideal Diode + High Side Switch Application (see Figure 23)



Figure 27. Application Response to 11 V to 0 V Transient on the Input (VIN) – Ideal Diode + High Side Switch **Application (see Figure 23)** 



Figure 28. Application response to 11 V to –18 V transient on the Input (V<sub>IN</sub>) – Reverse Polarity Protection + High Side Switch Application (see Figure 25)







#### Table 11. RECOMMENDED COMPONENTS FOR OPTIMAL EMC PERFORMANCE (Note 7)

C <sub>IN</sub> (μF)	C <sub>bulk</sub> (μF)	C <sub>G</sub> (nF)	R <sub>S</sub> (Ω)	R <sub>G_Q1</sub> (Ω)	
0.1	1				
0.1	10				
4.7	10		10	10	
10	101010				
•	•	•			





Figure 32. Startup with EN –  $C_G = 1$  nF Inrush Current Reduction



Figure 33. Startup with EN –  $C_G$  = 4.7 nF Inrush Current Reduction

#### **Thermal Considerations**

The NCV68261 has no thermal protection function as it is not designed to handle large currents itself. Regarding the application, the most heated elements are the external NMOS transistors. In case an SMD transistors are used, maximum power dissipation, thermal resistance of the NMOSs and cooling area of the PCB should be considered to keep the junction temperature of the controller below **WDFNW6 2x2, 0.65P** C

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