

NCV68261

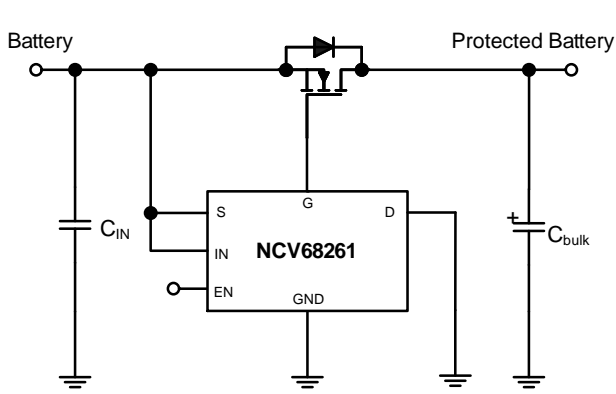


Figure 3. NCV68261 Application Schematic (Reverse Polarity Protection)

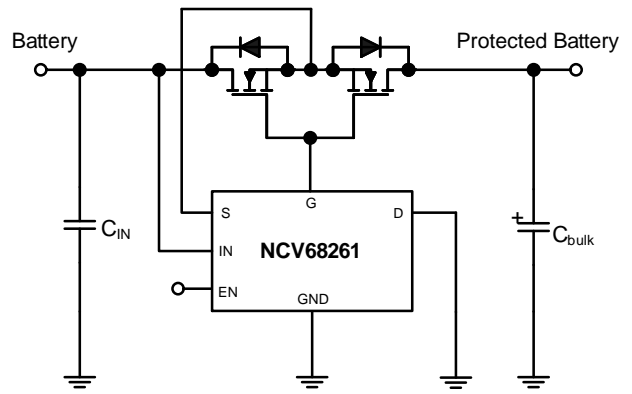


Figure 4. NCV68261 Application Schematic (Reverse Polarity Protection + High Side Switch)

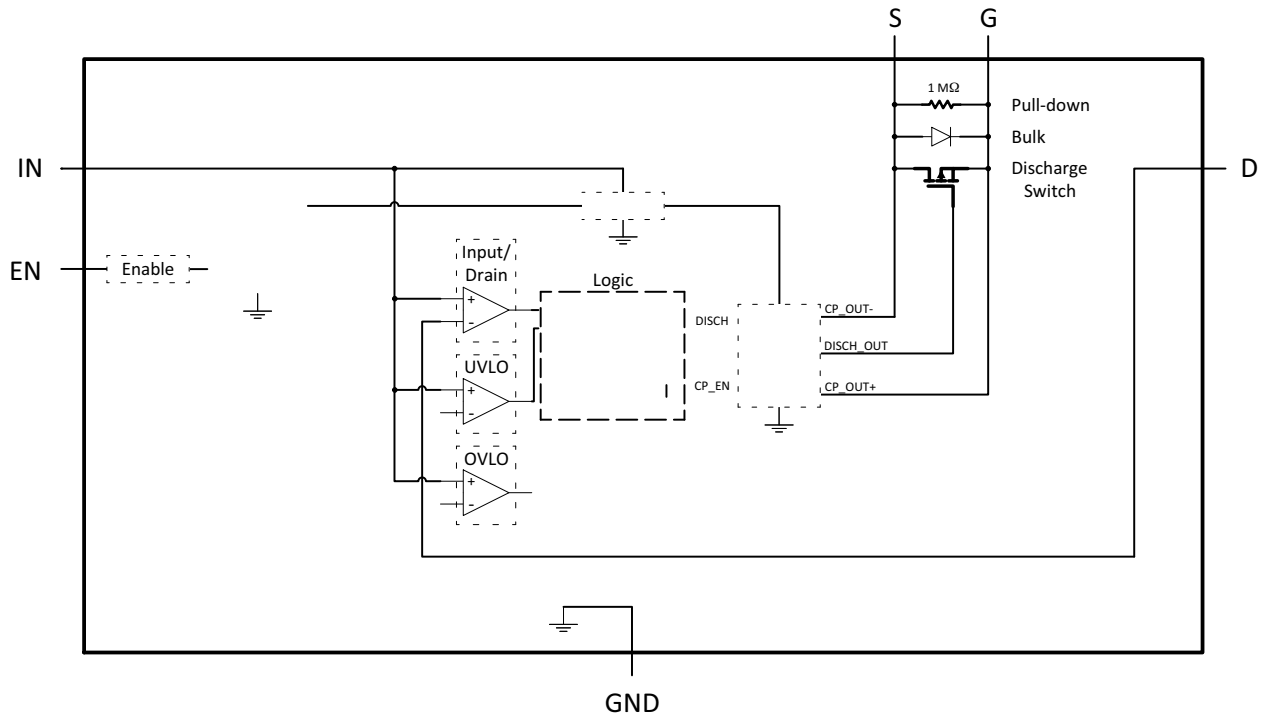
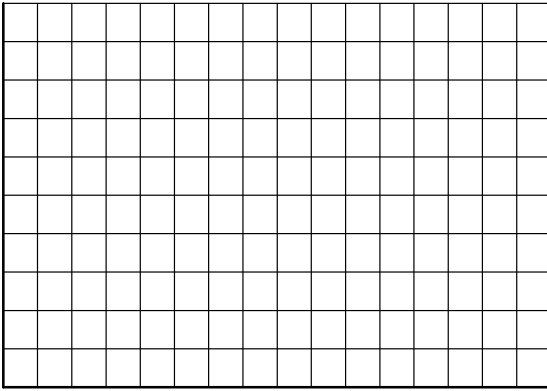


Figure 5. NCV68261 Block Diagram

TYPICAL CHARACTERISTICS



V_{IN}

Figure 6. Gate-to-Source Charged Voltage vs. Input Voltage

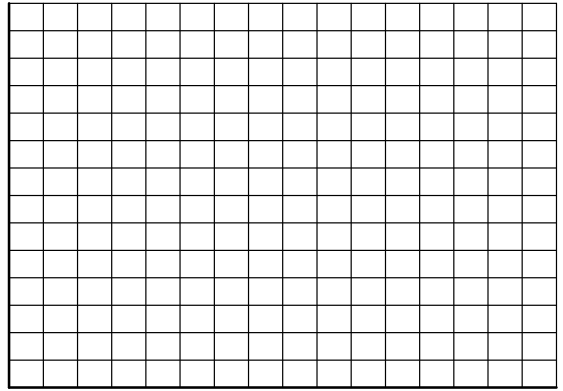
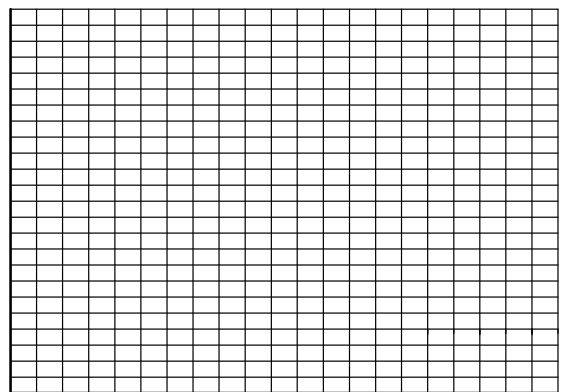
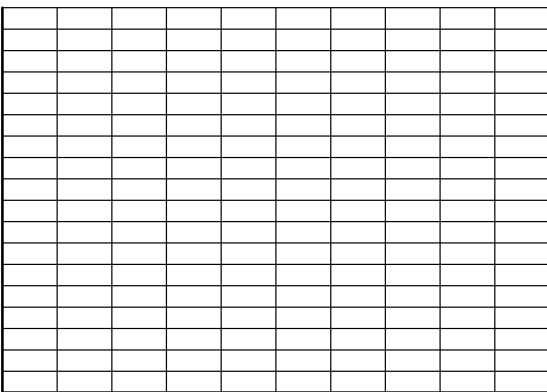
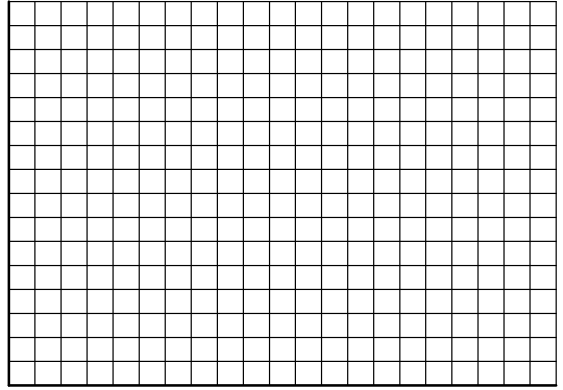
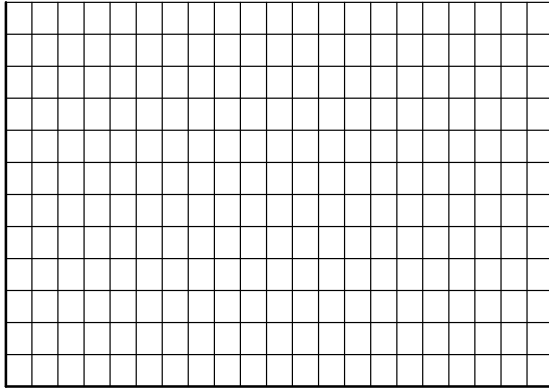
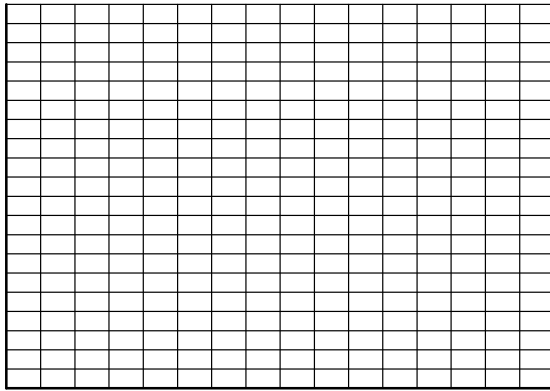


Figure 7. Gate Charge Current vs. Input Voltage



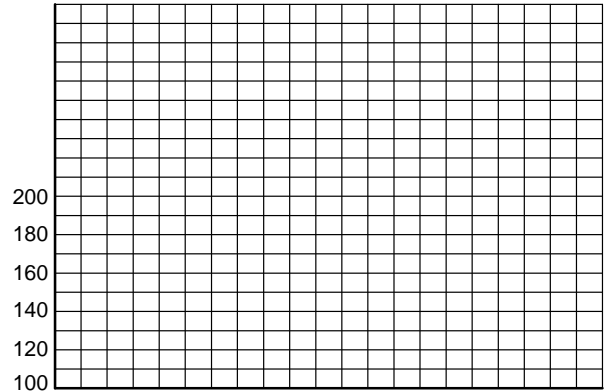
TYPICAL CHARACTERISTICS



2 4 6 8 10 12 14

V_{IN} , INPUT VOLTAGE (V)

Figure 12. Quiescent Current vs. Input Voltage



200

180

160

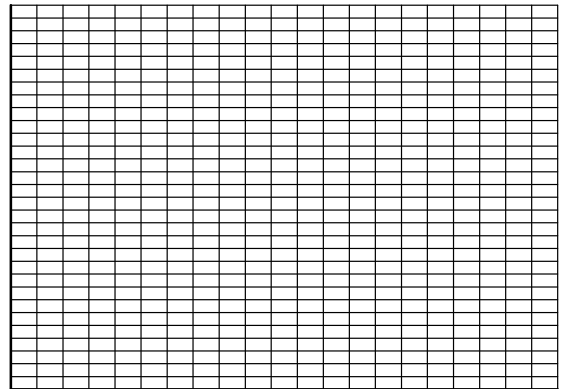
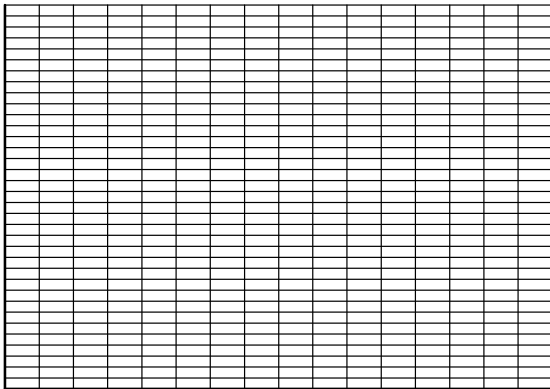
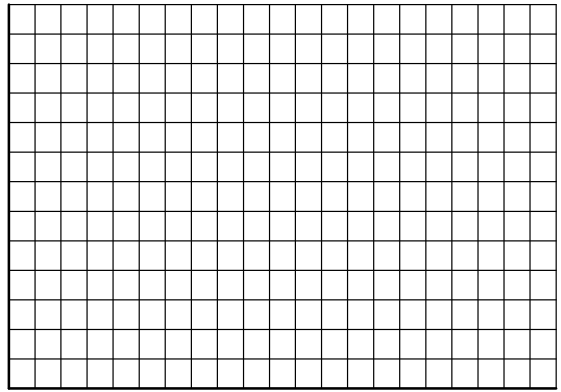
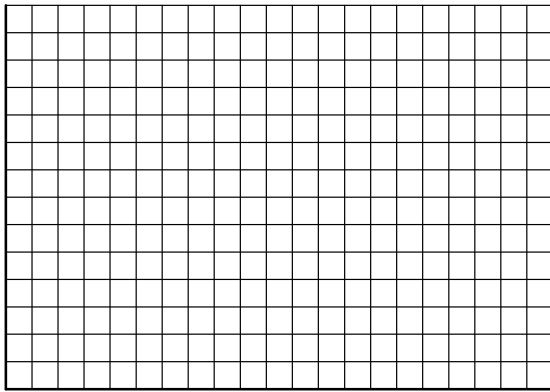
140

120

100

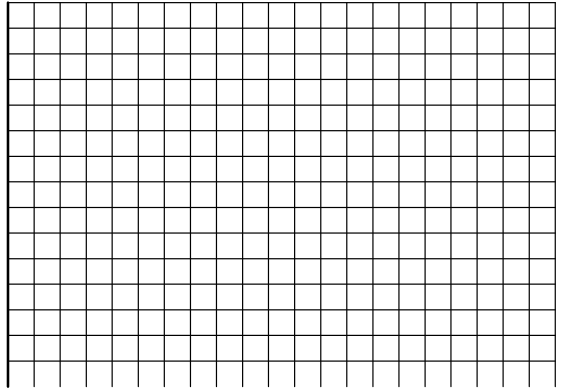
T_J , JUNCTION TEMPERATURE (°C)

Figure 13. Quiescent Current vs. Temperature



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TYPICAL CHARACTERISTICS



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Table 8. ISO 7637-2: 2011(E) PULSE TEST RESULTS

ISO 7637-2:2011(E) Test Pulse

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APPLICATION INFORMATION

INTEGRATED CIRCUIT AND BLOCK DIAGRAM DESCRIPTION

Integrated Circuit Description

Enable

Operation

-

OFF state

-

-

Ω

ON state

Ideal Diode

Reverse Polarity Protection

Ideal Diode + High Side Switch

Reverse Polarity Protection + High Side Switch

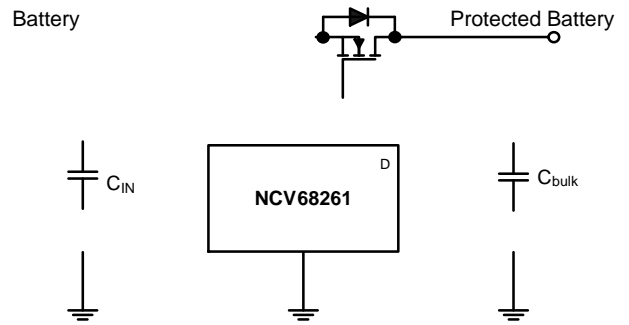


Figure 22. Ideal Diode

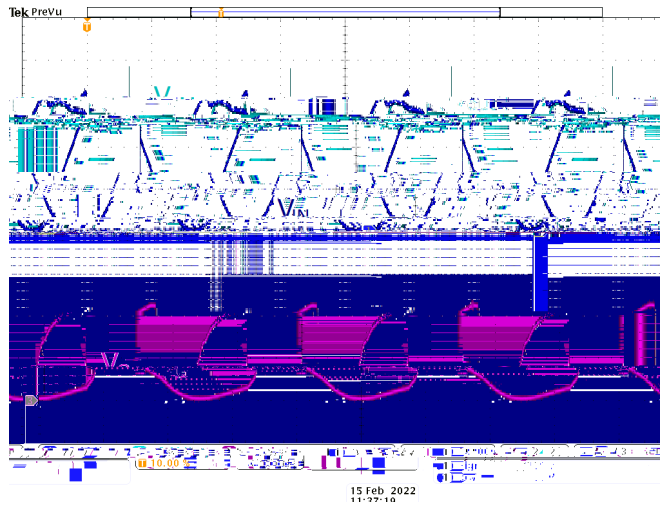


Figure 26. Application Response to 13 V + 6 V_{pp} Sine Wave on the Input (V_{IN}) – Ideal Diode + High Side Switch Application (see Figure 23)

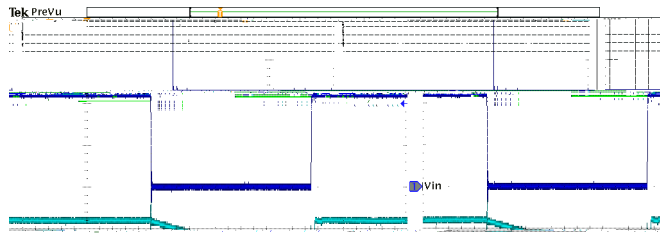


Figure 27. Application Response to 11 V to 0 V Transient on the Input (V_{IN}) – Ideal Diode + High Side Switch Application (see Figure 23)

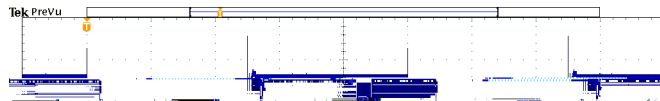


Figure 28. Application response to 11 V to -18 V transient on the Input (V_{IN}) – Reverse Polarity Protection + High Side Switch Application (see Figure 25)

C

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Table 11. RECOMMENDED COMPONENTS FOR OPTIMAL EMC PERFORMANCE (Note 7)

C_{IN} (μF)	C_{bulk} (μF)	C_G (nF)	R_S (Ω)	R_{G_Q1} (Ω)
0.1	1	1	10	10
0.1	10			
4.7	10			
10	101010			

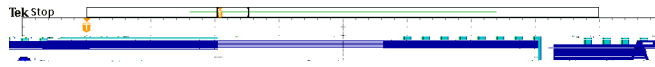


Figure 32. Startup with EN – $C_G = 1\text{ nF}$ Inrush Current Reduction



Figure 33. Startup with EN – $C_G = 4.7\text{ nF}$ Inrush Current Reduction

Thermal Considerations



WDFNW6 2x2, 0.65P

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