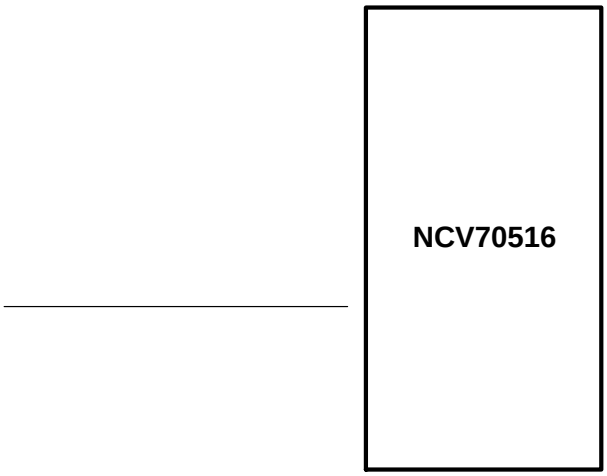
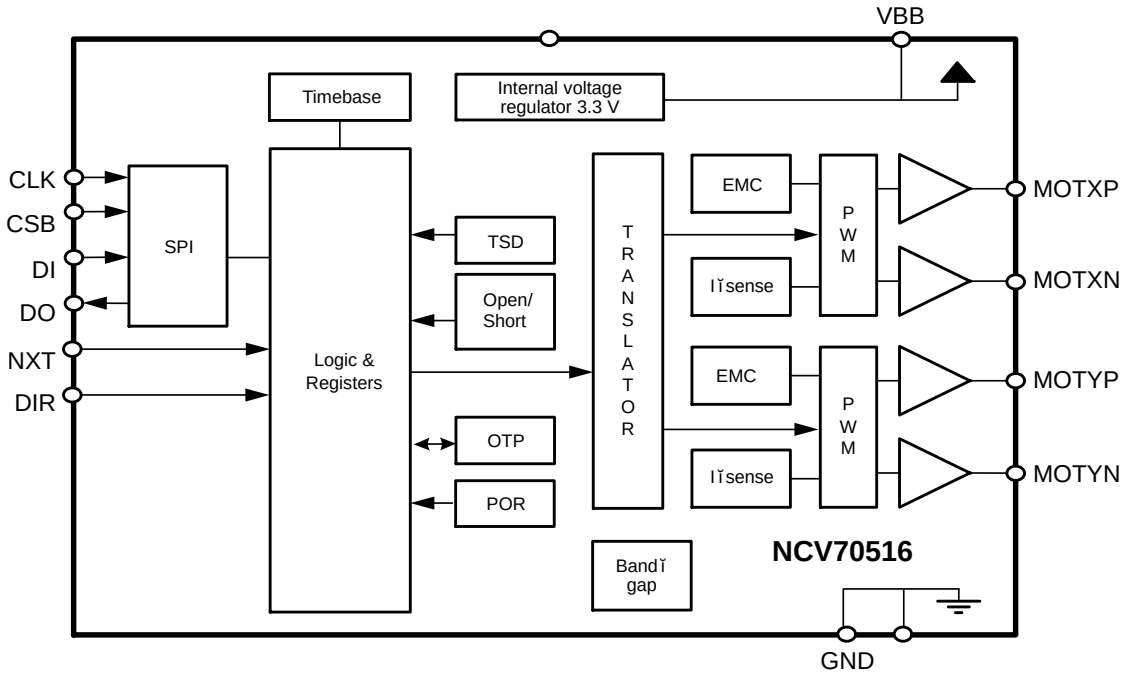
TYPICAL APPLICATION SCHEMATIC

The application schematic below shows typical connections for applications with low axis counts and/or with software SPI implementation. For applications with many stepper motor drivers, some “minimal wiring” examples are shown at the last sections of this datasheet.




VBB
Timebase
Internal voltage regulator 3.3 V
CLK
CSB
DI
DO
NXT
DIR
SPI
Logic & Registers
TSD
Open/ Short
OTP
POR
TRANSLATOR
EMC
Iĭsense
EMC
Iĭsense
PWM
PWM
MOTXP
MOTXN
MOTYP
MOTYN
Bandĭ gap
NCV70516
GND

PACKAGE AND PIN DESCRIPTION

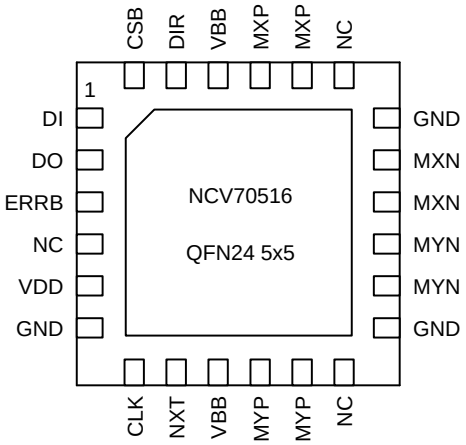


Figure 3. Pin Connections – QFN24

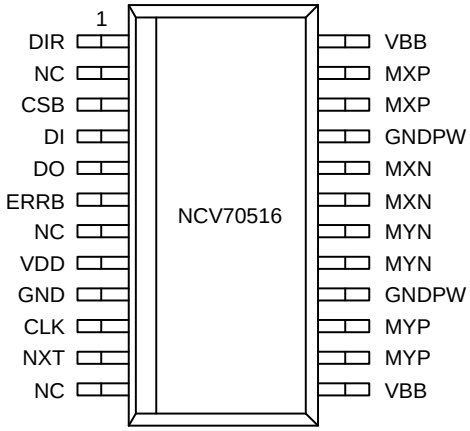


Figure 4. Pin Connections – SSOP24

Table 2. PIN DESCRIPTION

Pin No. QFN24 5x5	Pin No. SSOP24 NB EP	Pin Name	Description	I/O Type
1	4	DI	SPI data input	Digital Input
2	5	DO	SPI data output	Digital Output
3	6	ERRB	Error Output (Open Drain)	Digital Output
4, 12, 19	2, 7, 12	NC	Not connected	
5	8	VDD	Internal supply (needs external decoupling capacitor)	Supply
6	9	GND	Ground	Supply
7	10	CLK	SPI clock input	Digital Input
8	11	NXT	Next micro ĭ step input	Digital Input
9, 22	13, 24	VBB	Battery voltage supply	Supply
10, 11	14, 15	MOTYP	Positive end of phase Y coil	Driver output
13, 18	16, 21	GNDPW	Ground	Supply
14, 15	17, 18	MOTYN	Negative end of phase Y coil	Driver output
16, 17	19, 20	MOTXN	Negative end of phase X coil	Driver output
20, 21	22, 23			

EQUIVALENT SCHEMATICS

The following figure gives the equivalent schematics of the user relevant inputs and outputs. The diagrams are simplified representations of the circuits used.

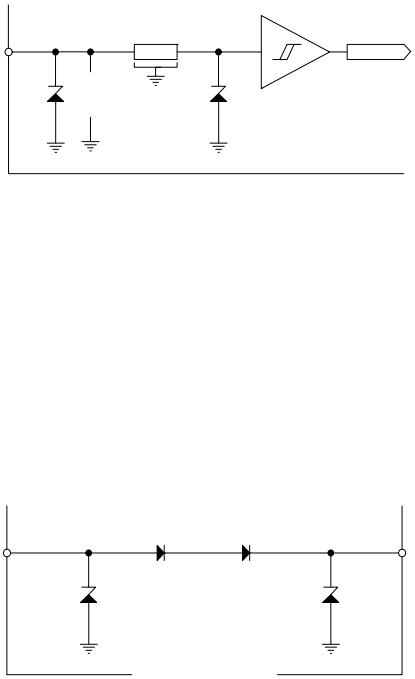


Figure 5. Input and Output Equivalent Diagrams

ELECTRICAL CHARACTERISTICS

DC PARAMETERS

The DC parameters are guaranteed over junction temperature from −40 to 145°C and VBB in the operating range from 6 to 29 V, unless otherwise specified. Convention: currents flowing into the circuit are defined as positive.

Table 6. DC PARAMETERS

Symbol	Pin(s)	Parameter	Test Conditions	Min	Typ	Max	Unit
MOTORDRIVER							
$I_{MS-max,Peak}$	MOTXP MOTXN MOTYP MOTYN	Max current through motor coil in normal operation	V_{BB} = 14 V		800		mA
$I_{MS-boost,Peak}$		Max current during booster function	V_{BB} = 14 V, T_j = ĭ45°C		1100		mA
I_{MSabs}		Absolute error on coil current	V_{BB} = 14 V, T_j = 145°C $I_{MSmax,Peak}$ = 800 mA and 100 mA	ĭ10		10	%
I_{MSrel}		Matching of X & Y coil currents	V_{BB} = 14 V $I_{MSmax,Peak}$ = 800 mA and 100 mA	ĭ7		7	%
$R_{DS(on)}$		On resistance of High side + Low side Driver at the highest current range	T_j = 145°C			2.4	Ω
LOGIC INPUTS							
V_{inL}	Ct4t9jÆT107.943 4961792 .90709 23.291 23f107.943 496.926 48.52 .90704 7efBT8 0 0 8 156.8693 514796211Tm-.0015 Tc(DSLogic l siin						

AC PARAMETERS

The AC parameters are guaranteed over junction temperature from −40 to 145°C and VBB in the operating range from 6 to 29 V, unless otherwise specified.

Table 7. AC PARAMETERS

Symbol	Pin(s)	Parameter	Test Conditions	Min	Typ	Max	Unit
INTERNAL OSCILLATOR							
f_{osc}		Frequency of internal oscillator	V_{BB} = 14 V	9	10	11	MHz
MOTORDRIVER							
f_{pwm}	MOTxx	PWM frequency	(Note 25)		28.4		kHz
f_{jit_depth}		PWM jitter modulation depth	SPI bit PWMJen = 1 (Note 25)			20	%
t_{OCdet}		Open coil detection with PWM=100% (Note 25)	SPI bit OpenDet[1:0] = 00		5		ms
			SPI bit OpenDet [1:0] = 01SPI bit PWMJen = 1				

Table 8. SPI INTERFACE

Symbol	Parameter	Min	Typ	Max	Unit
t_{CSS}	CSB setup time (Note 26)	0.5			μs
t_{CSH}	CSB hold time	0.5			μs
t_{CS}	CSB high time				

Translator Position

The translator position can be read and set by the SPI register <MSP[5:0]>. This is a 6−bit number equivalent to the 1/16th micro−step from Table 9: Translator Table. The translator position is updated immediately following a next micro−step trigger (see below).

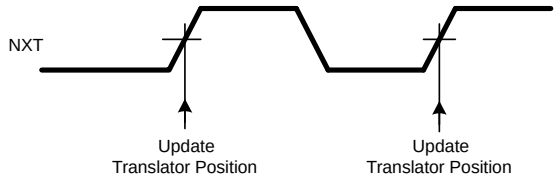


Figure 10. Translator Position Timing Diagram

Direction

The direction of rotation is selected by means of input pin DIR and its “polarity bit” <DIRP> (SPI register). The polarity bit <DIRP> allows changing the direction of rotation by means of only SPI commands instead of the dedicated input pin.

Direction = DIR−pin EXOR <DIRP>

Positive direction of rotation means counter−clockwise rotation of electrical vector Ix + Iy. Also when the motor is

To enable the motor again after reading out of the status flags, <MOTEN>=1 has to be written.

Notes:

1. Successive reading of the <SHRTij> flags and re−enabling the motor in case of a short circuit condition may lead to damage of the drivers.
2. Example: SHRTXPT means: Short at X coil, Positive output pin, Top transistor.
3. In case of the short from any stepper motor pin to the top side during switching event from bottom to top on motor pin, the flag “short to bottom side” is set instead of the expected “short to top side” flag.

Step Loss Detection

When Next pulse is applied (by means of NXT pin or <NXTP> bit via SPI) or <MSP> register is written during error condition, the step loss bit <SL> is set.

<SL> = (<UV> OR <TSD> OR <ELDEF>) AND ((NXT OR <NXTP>) OR <MSP> write)

Step loss bit <SL> is cleared after read out.

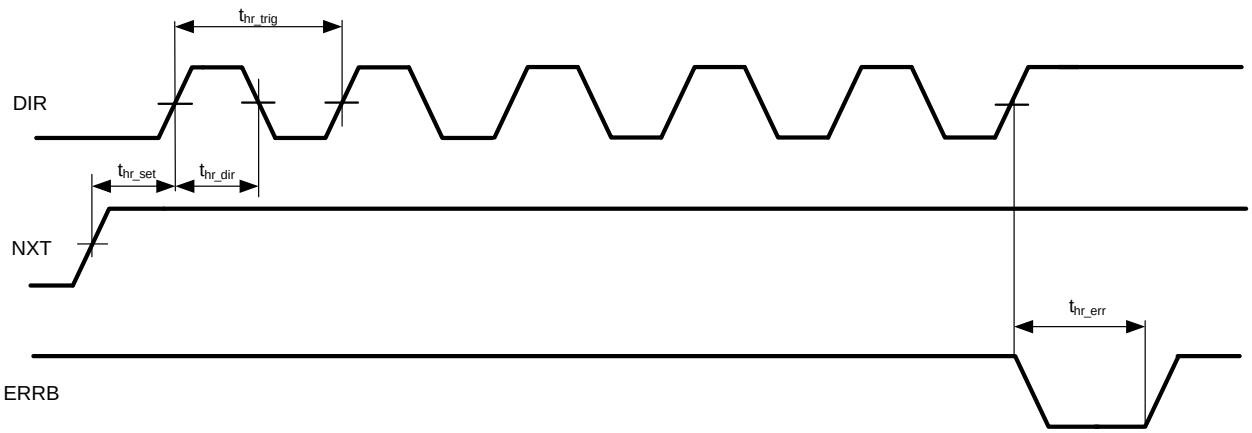

t_{hr_trig}
DIR
t_{hr_set}
t_{hr_dir}
NXT
t_{hr_err}
ERRB

Figure 15. SPI Daisy Chain Data Shift Between

SPI Control Registers (CR)

All SPI control registers have Read/Write access.

Table 12. SPI CONTROL REGISTERS (CR)

5−bit Address	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default after Res.
00h	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	00 0000 0000
01h (CR1)	NotUsed	NXTP	MOTEN	DIRP	IBOOST	ACTBR	IMOT3	IMOT2	IMOT1	IMOT0	00 0000 0000
02h (CR2)	NotUsed	PWMJen	OpenDet1	OpenDet0	OpenDis	OpenHiZ	SLP	SM2	SM1	SM0	00 1000 1000
03h (CR3)	NotUsed	NotUsed	NotUsed	NotUsed	NotUsed	NotUsed	NotUsed	NotUsed	NotUsed	NotUsed	00 0000 0000
04h (CR4)	NotUsed	NotUsed	NotUsed	NotUsed	MSP5	MSP4	MSP3	MSP2	MSP1	MSP0	00 0000 1000

Table 13. BIT DEFINITION

Symbol	MAP position	Description
NOP	Bits [9:0] – ADDR_0x00	NOP register (read/write operation ignored)
NXTP	Bit 8 – ADDR_0x01 (CR1)	Push button pin, generating next step in position table
MOTEN	Bit 7 – ADDR_0x01 (CR1)	Enables the H−bridges (motor activated)
DIRP		

SPI Status Registers (SR)

All SPI status registers have Read Only Access, with the odd parity on Bit8. Parity bit makes the numbers of 1 in the byte odd.

Table 14. SPI STATUS REGISTERS (SR)

5−bit Address	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default after Res.
05h (SR1)	0x0	PAR	SL, L	SPI,L	ELDEF, R*	TAMB, R	TSD,L	TW,R	UV, L	0x0	
06h (SR2)	0x0	PAR	0x0	0x0	HR,L	OPENX,L	SHRTXPB,L	SHRTXNB,L	SHRTXPT,L	SHRTXNT,L	
									SHRTYPT,L	SHRTYNT,L	

APPLICATION EXAMPLES FOR MULTI−AXIS CONTROL

The wiring diagrams below show possible connections of multiple slaves to one microcontroller. In these examples,

PACKAGE DIMENSIONS

QFN24 5x5, 0.65P
CASE 485CS
ISSUE O