Octal Low-Side Relay

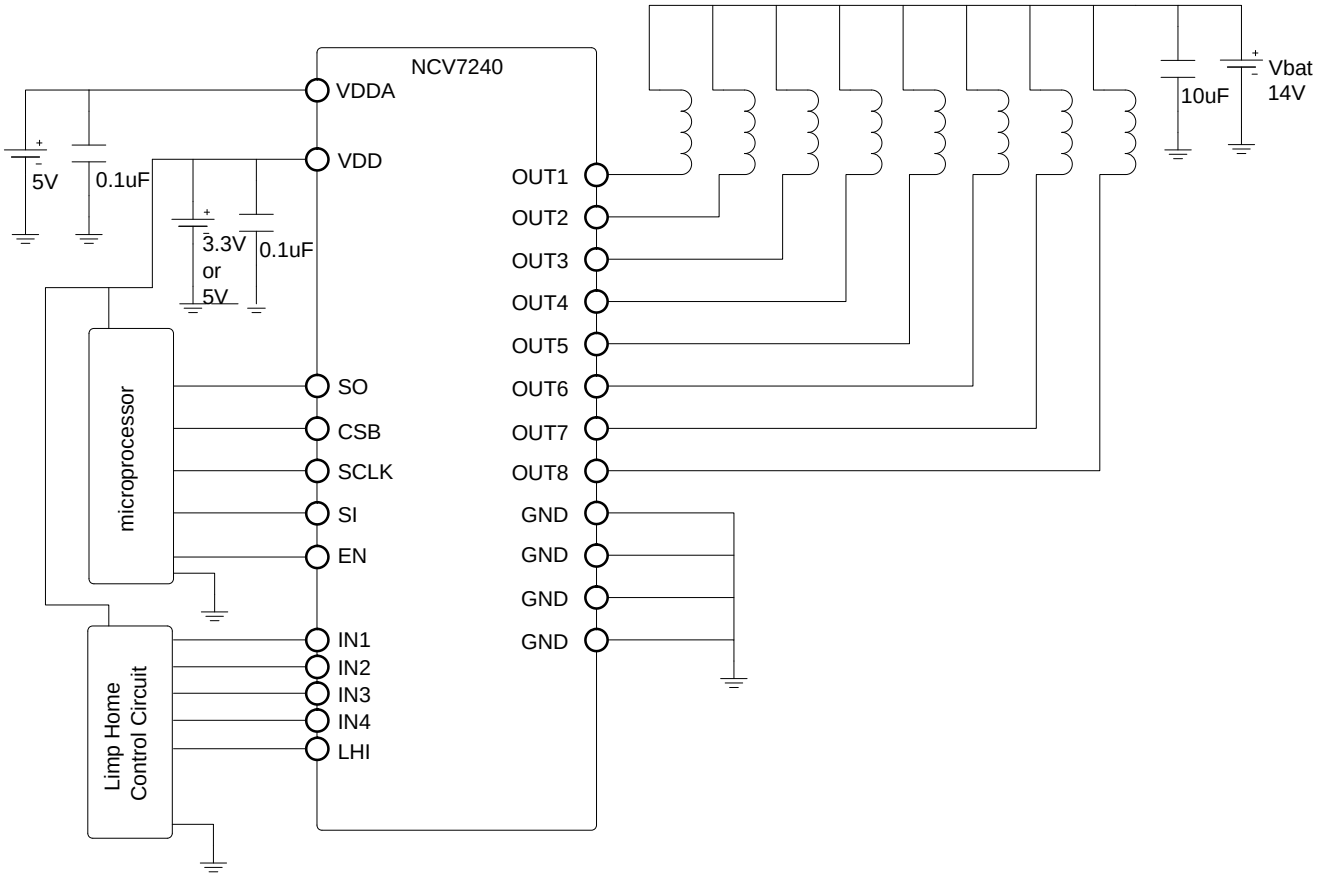


Figure 2. Application Diagram (relay loads)

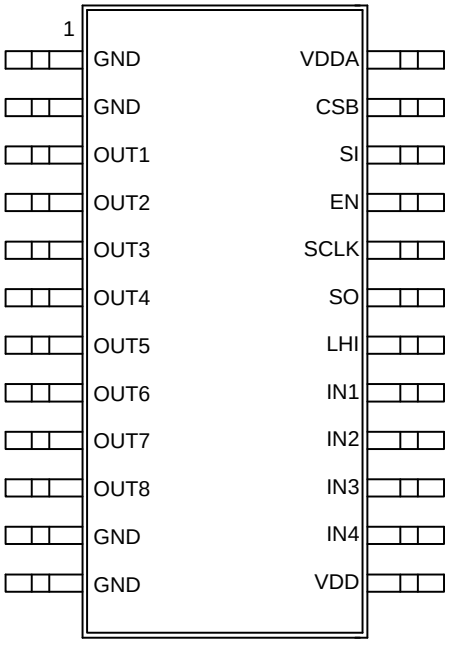


Figure 3. Pinout

PACKAGE PIN DESCRIPTION

SSOP−24	Symbol	Description
1	GND	Ground.
2	GND	Ground.
3	OUT1	Channel 1 low−side drive output. Requires an external pull−up device for operation.
4	OUT2	Channel 2 low−side drive output. Requires an external pull−up device for operation.
5	OUT3	Channel 3 low−side drive output. Requires an external pull−up device for operation.
6	OUT4	Channel 4 low−side drive output. Requires an external pull−up device for operation.
7	OUT5	Channel 5 low−side drive output. Requires an external pull−up device for operation.
8	OUT6	Channel 6 low−side drive output. Requires an external pull−up device for operation.
9	OUT7	Channel 7 low−side drive output. Requires an external pull−up device for operation.
10	OUT8	Channel 8 low−side drive output. Requires an external pull−up device for operation.
11	GND	Ground.
12	GND	Ground.
13	VDD	Digital Power Supply for SO output (3.3 V or 5 V).
14	IN4	Parallel control of OUT4 and OUT8 Ground if not used for best EMI performance. Alternatively keep open and internal pull−down will hold the input low. (120 kΩ pull down resistor).
15	IN3	Parallel control of OUT3 and OUT7 Ground if not used for best EMI performance. Alternatively keep open and internal pull−down will hold the input low. (120 kΩ pull down resistor).
16	IN2	Parallel control of OUT2 and OUT6. Ground if not used for best EMI performance. Alternatively keep open and internal pull−down will hold the input low. (120 kΩ pull down resistor).
17	IN1	Parallel control of OUT1 and OUT5. Ground if not used for best EMI performance. Alternatively keep open and internal pull−down will hold the input low. (120 kΩ pull down resistor).
18	LHI	Limp Home Input. Active High. A high on this pin powers up the device and activates the respective output drive INx designator while disabling outputs OUT5−OUT8. Input SPI commands are ignored, but the output register reports faults. (Read capability only. No write capability.) All registers are reset coming out of LHI mode. Ground if not used for best EMI performance. Alternatively keep open and internal pull−down resistor (120 kΩ) will hold the input low.
19	SO	SPI serial data output. Output high voltage level referenced to pin VDD.
20	SCLK	SPI clock (120 kΩ pull down resistor).
21	EN	Global Enable (active high). (120 kΩ pull down resistor).
22	SI	SPI serial data input (120 kΩ pull down resistor).
23	CSB	SPI Chip Select ”Bar” (120 kΩ pull up resistor to VDD).
24	VDDA	Analog Power Supply Input voltage (5 V).

MAXIMUM RATINGS

Parameter	Min	Max	Unit
Supply Input Voltage (VDDA, VDD) DC	 −0.3	 5.5	V
Digital I/O pin voltage (EN, LHI, Inx, CSB, SCLK, SI) (SO)	 −0.3 −0.3	 5.5 V_{DD} + 0.3	V
High Voltage Pins (OUTx) DC Peak Transient	 −0.3	 36 44 (Note 1)	V
Output Current (OUTx)	−1	1.3	A
Clamping Energy Maximum (single pulse) Repetitive (multiple pulse) (Note 2)	 − −	 75 −	mJ
Operating Junction Temperature Range	−40	150	

ELECTRICAL CHARACTERISTICS (3.0 V < VDD < VDDA, 4.5 V < VDDA (Note 7) < 5.5 V, −40 C ≤ T_J ≤ 150 C, EN = VDD, LHI = 0 V unless otherwise specified).

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
GENERAL						
I_{VDDA_ON}	Operating Current (VDDA) ON Mode (All Channels On)		−	3	5	mA
$I_{VDDA\_GS\_25}$ $I_{VDDA\_GS\_85}$ $I_{VDDA\_GS\_150}$	Quiescent Current (VDDA) Global Standby Mode (All Channels Off)	SI = SCLK = 0 V, CSB = VDD T_J = 25 C T_J = 85 C T_J = 150 C	− − −		32 35 40	
$I_{VDDA\_LO\_25}$ $I_{VDDA\_LO\_85}$ $I_{VDDA\_LO\_150}$	Quiescent Current (VDDA) Low Iq Mode	SI = SCLK = EN = 0 V, CSB = VDD T_J = 25 C T_J = 85 C T_J = 150 C	− − −	− − −	10 10 20	µA
I_{VDD_ON}	Operating Current (VDD) ON Mode (All Channels On)	EN=high, SCLK = Inx = 0 V, CSB = VDD = VDDA	−	0.3	0.5	mA
$I_{VDD\_GS\_25}$ $I_{VDD\_GS\_85}$						

ELECTRICAL CHARACTERISTICS (3.0 V < VDD < VDDA, 4.5 V < VDDA (Note 7) < 5.5 V, −40 C ≤ T_J ≤ 150 C, EN = VDD, LHI = 0 V unless otherwise specified).

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
OUTPUT TIMING SPECIFICATIONS						
t_{WU}						

TYPICAL PERFORMANCE GRAPHS

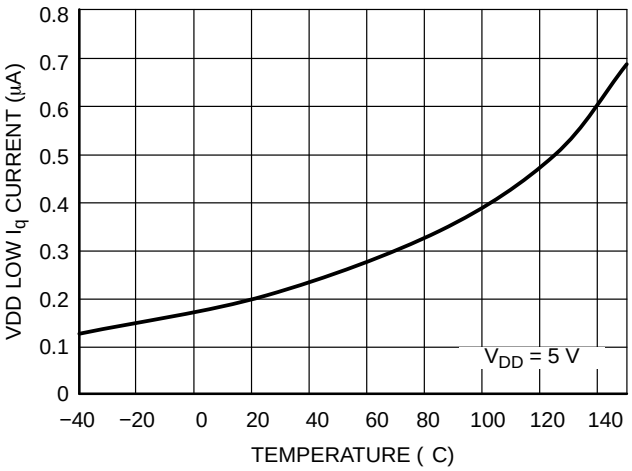


Figure 6. VDD Low I_q Current vs. Temperature

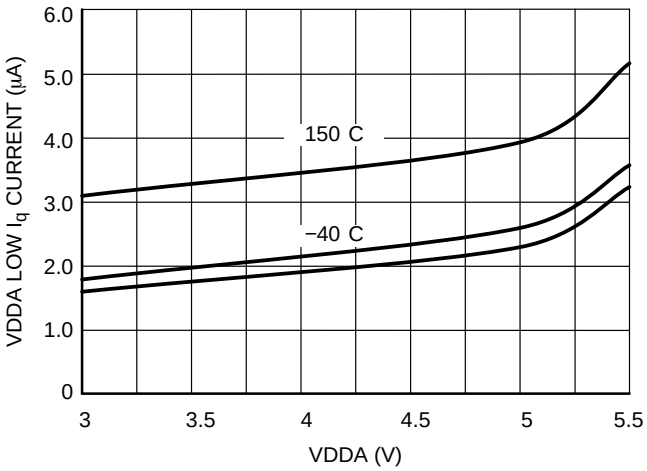
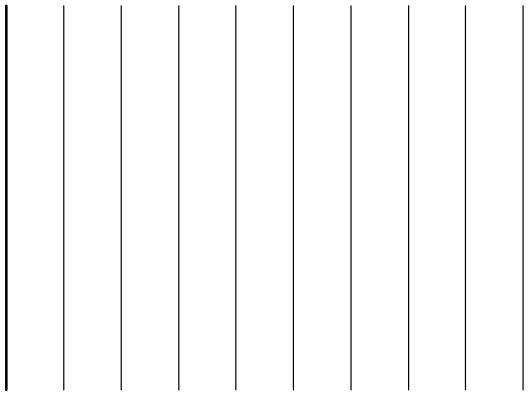
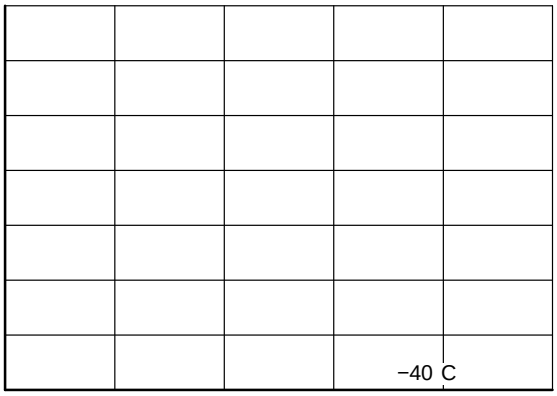
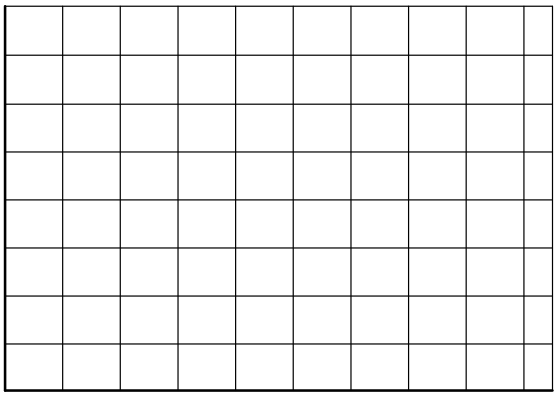


Figure 7. VDDA Low I_q Quiescent Current vs. VDDA







TYPICAL PERFORMANCE GRAPHS

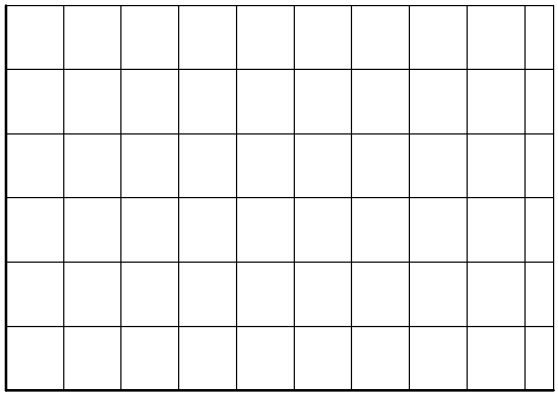


Figure 12. Output R

TYPICAL PERFORMANCE GRAPHS

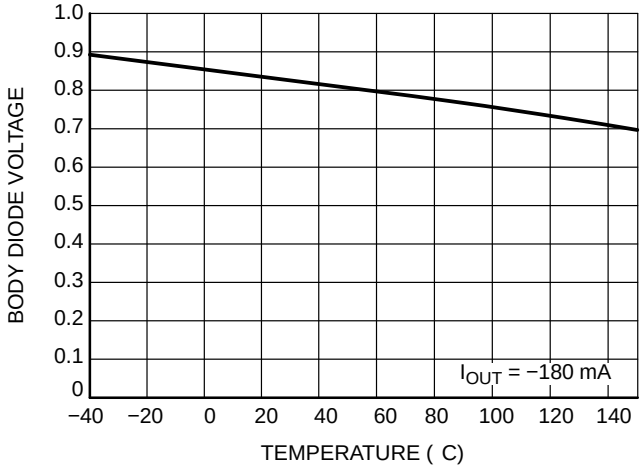


Figure 18. Output Body Diode Voltage vs. Temperature

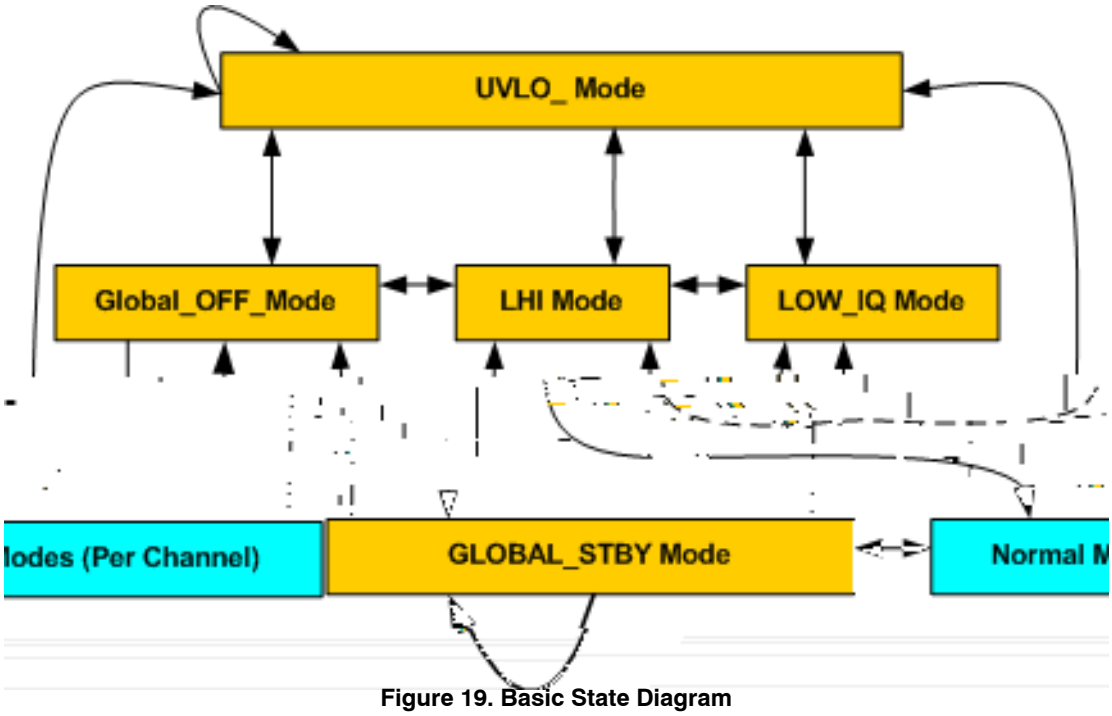


Figure 19. Basic State Diagram

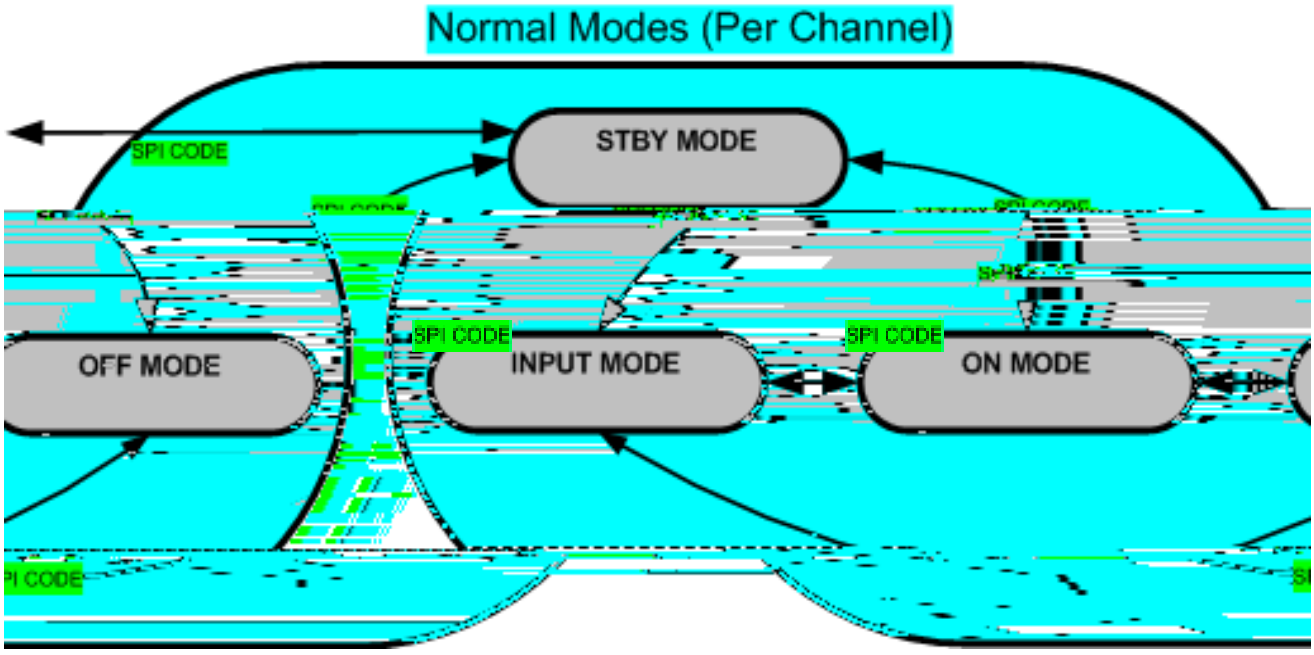


Figure 20. Normal Operation State Diagram

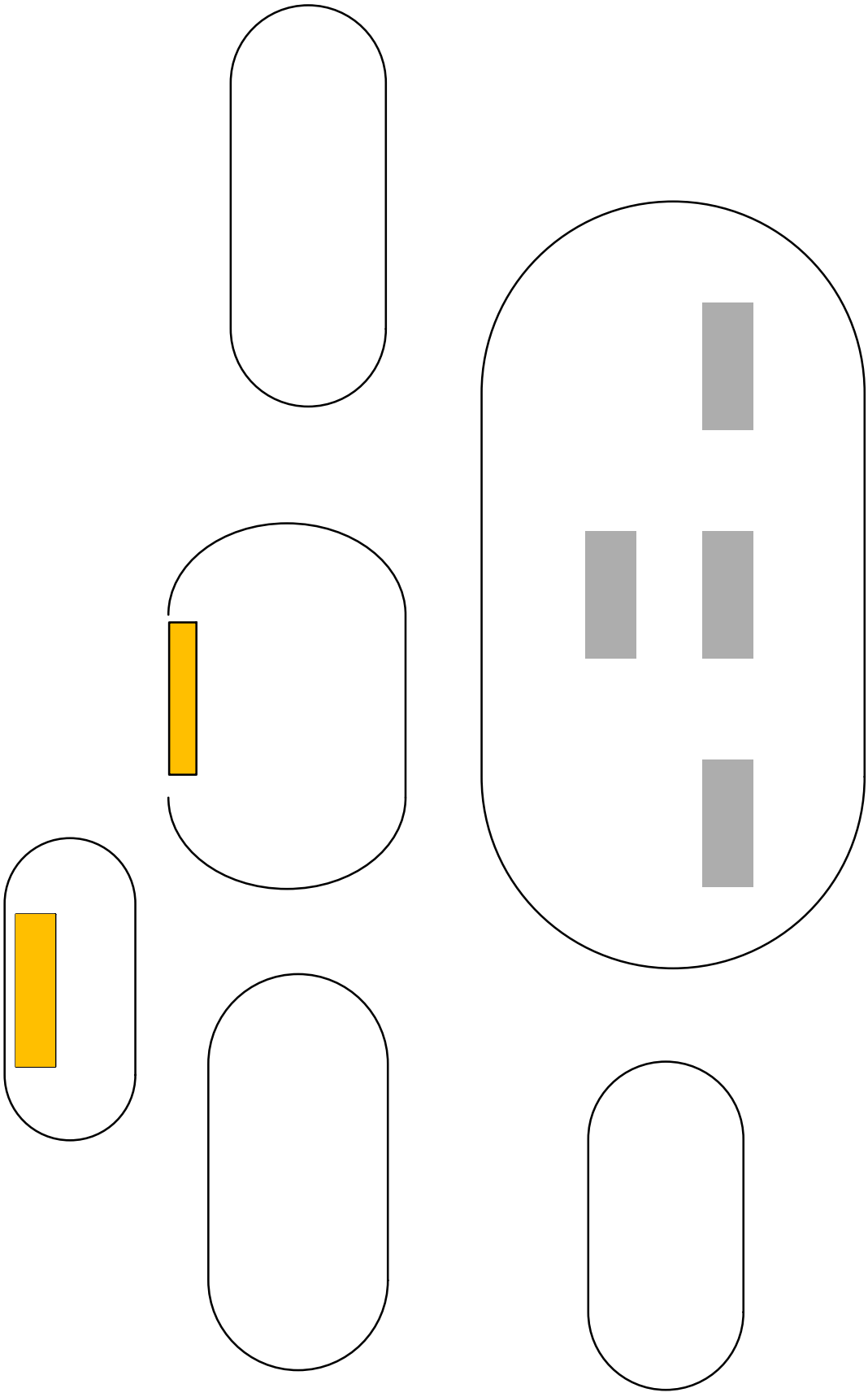
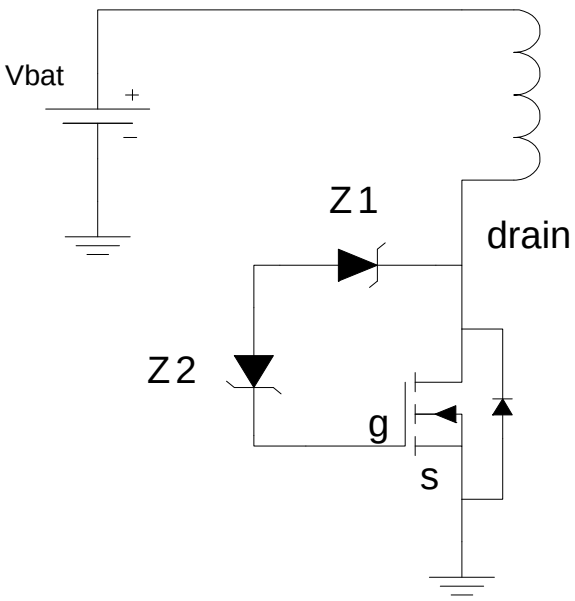
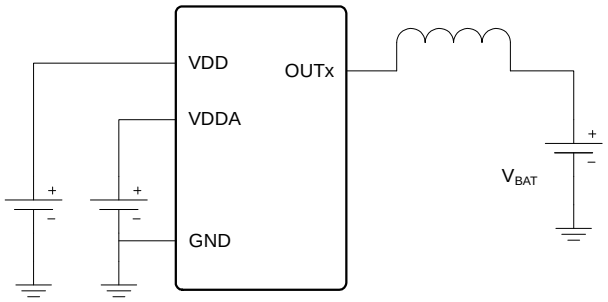


Figure 21. Detailed State Diagram

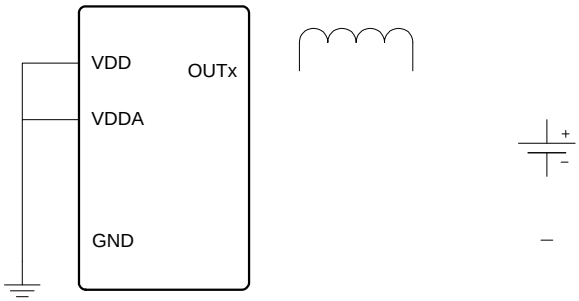
Limp Home and PWM operation (INx control)

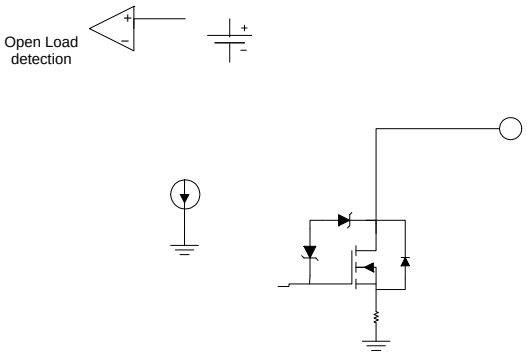


Vdrain = VZ1 + VZ2 + Vgs



$V_{C\,a,\,,} = 36V\,(.\ .)\quad 44V\,(.\ \hat{a}\,)\ P\qquad d$




Open Load
detection

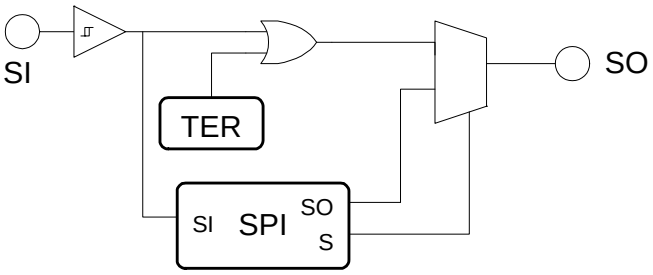


Figure 25. TER SPI Link

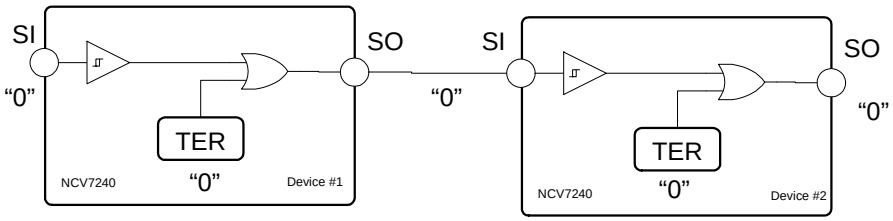
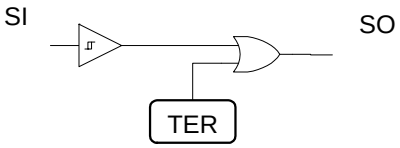


Figure 26. TER (no error)



TER Information Retrieval

TER information retrieval is as simple as bringing CSB high ĭ to ĭ low. No clock signals are required.

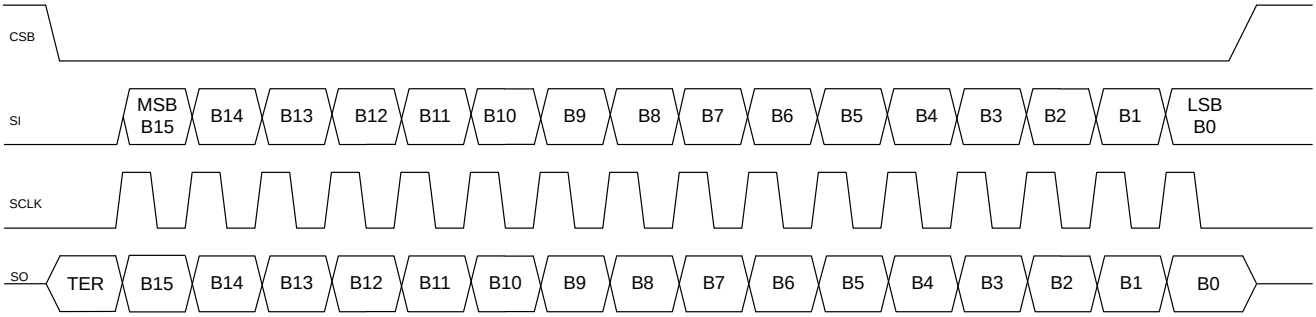


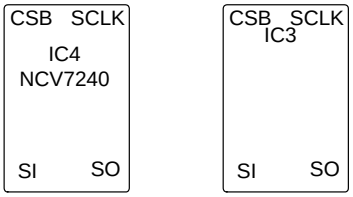
Figure 29. Serial Peripheral Interface

The timing diagram highlighted in Figure 29 shows the SPI interface communication.
Note:

DAISY CHAIN SETUP

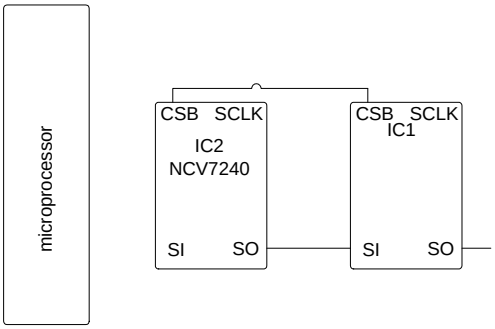
Serial Connection

Daisy chain setups are possible with the NCV7240. The serial setup shown in Figure 31 highlights the NCV7240 along with any 16 bit device using a similar SPI protocol. Particular attention should be focused on the fact that the first 16 bits which are clocked out of the SO pin when the CSB pin transitions from a high to a low will be the Diagnostic Output Data from the Fault Output Register. These are the bits representing the status of the IC. Additional programming bits should be clocked in which follow the Diagnostic Output bits. The timing diagram shows a typical transfer of data from the microprocessor to the SPI connected IC's.



8−bit Devices

The NCV7240 is also compatible with 8 bit devices due to the features of the frame detection circuitry. The internal bit counter of the NCV7240 starts counting clock pulses when CSB goes low. The 1st valid word consists of 16 bits and each subsequent word must be comprised of just 8ĭbits (reference the Frame Detection Section).



Stepper Motor Operation

The NCV7240 device is capable of driving stepper motors. Each stepper motor requires 4 low−side drive outputs. Consequently, each NCV7240 device is capable of driving two stepper motors. Figure 36 below illustrates a Unipolar stepper motor setup. For proper operation, the code listed in Table 3 should be used (and repeated) for one way operation (clockwise). For reverse direction, simply reverse the code and repeat (counterclockwise). Outputs 1−4 are utilized for one stepper usage. For a 2nd stepper motor, repeat the code used for outputs 1−4 to outputs 5−8. During operation waveforms similar to Figure 37 can be expected on the OUTx pins.

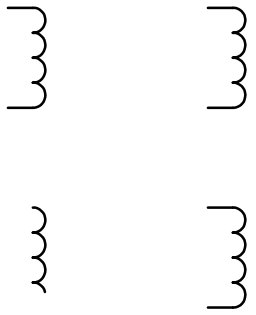


Figure 36. Stepper Motor Operation Setup

SI SPI Inp t t (1 - t t t t)

The 16−bit data received (SI) is decoded into instructions for each channel per the table below.
After a power−on reset, all register bits are set to a 1.

Table 4. SPI INPUT DATA

Channel 8		Channel 7		Channel 6		Channel 5		Channel 4		Channel 3		Channel 2		Channel 1	
MSB														LSB	
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

INPUT DATA REGISTER

Field	Bits	Description		
channel x (x = 1−8)	15, 14 13, 12 11, 10 9, 8 7, 6 5, 4 3, 2 1, 0	Command		
		00	Channel Stand−by Mode Fast channel turn off Corresponding Channel Fault Register reset	
			Diagnostic Current	Disabled
		01	Input Mode Channel Input directed to INx. (reference PWM operation section).	
			Diagnostic Current	Enabled in OFF State.
		10	ON Mode Channel turned on.	
			Diagnostic Current	Disabled
		11	OFF Mode Channel turned off.8)	

Table 6. FAULT CONDITIONS

Output Fault Condition	Fault Memory	Miscellaneous
Open Load	Latched	Detected in Driver Off State (1.75 V [Typ] threshold) when detection is enabled. Reported in Output Fault Diagnostics Register until cleared via the SPI port. Output will maintain turn−on capability.
Short to Ground	Latched	

SSOP24 NB
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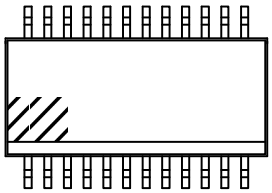
DATE 06 JUL 2010

SCALE 1:1



DIM	MILLIMETERS MIN	MAX
A		1.75
A1	0.10	0.25
b	0.20	0.30
c	0.19	0.25
e	0.65 BSC	
h	0.22	0.50
L	0.40	1.27
L2	0.25 BSC	