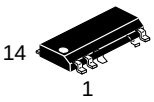
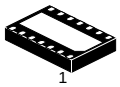
CA FD L , I H, AKE E D

C 7343

www.onsemi.com



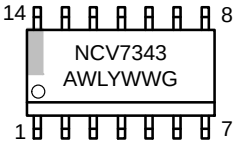
SOIC−14
D2 SUFFIX
CASE 751A−03



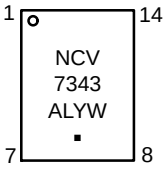
DFNW14 4.5x3, 0.65P
MW SUFFIX
CASE 507AC

MARKING DIAGRAMS

NCV7343D20



NCV7343MW0



SOIC−14 **DFNW14**

A	= Assembly Site
(W)L	= Wafer Lot
YW(W)	= Date Code
G or ▪	= Pb−Free Identification

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 21 of this data sheet.

Description

The NCV7343 CAN FD transceiver is the interface between a controller area network (CAN) protocol controller and the physical bus. The transceiver provides differential transmit capability to the bus and differential receive capability to the CAN controller.

The NCV7343 is an addition to the CAN high−speed transceiver family complementing NCV734x CAN stand−alone transceivers and previous generations such as AMIS42665, AMIS3066x, etc.

The NCV7343 guarantees additional timing parameters to ensure robust communication at data rates beyond 1 Mbit/s to cope with CAN flexible data rate requirements (CAN FD). These features make the NCV7343 an excellent choice for all types of HS−CAN networks, in nodes that require a low−power mode with wake−up capability via the CAN bus.

Features

- Compliant with International Standard ISO11898−2:2016
- CAN FD Timing Specified up to 5 Mbit/s
- Extended Bus Load Range
- Standby and Sleep Mode with very Low Current Consumption
- CAN Wake−up with Wake−up Pattern (WUP), Short CAN Activity Filter Time, Long Wake−up Timeout and Normal Bus Biasing.
- Local Wake−up
- V_{IO} Pin Allowing Direct Interfacing with 3 V to 5 V MCUs
- Low Electromagnetic Emission (EME) and High Electromagnetic Susceptibility (EMS)
- High Impedance Bus Lines in Unpowered State
- Transmit Data (TxD) Dominant Timeout Function (Long)
- Bus Error Detection
- Under all Supply Conditions the Chip behaves Predictably
- ESD Robustness of Bus Pins > 8 kV
- Thermal Protection
- Bus Pins Short Circuit Proof to Supply Voltage and Ground
- Bus Pins Protected against Transients in an Automotive Environment
- AEC−Q100 Grade 0 Qualified and PPAP Capable
- These are Pb−Free Devices

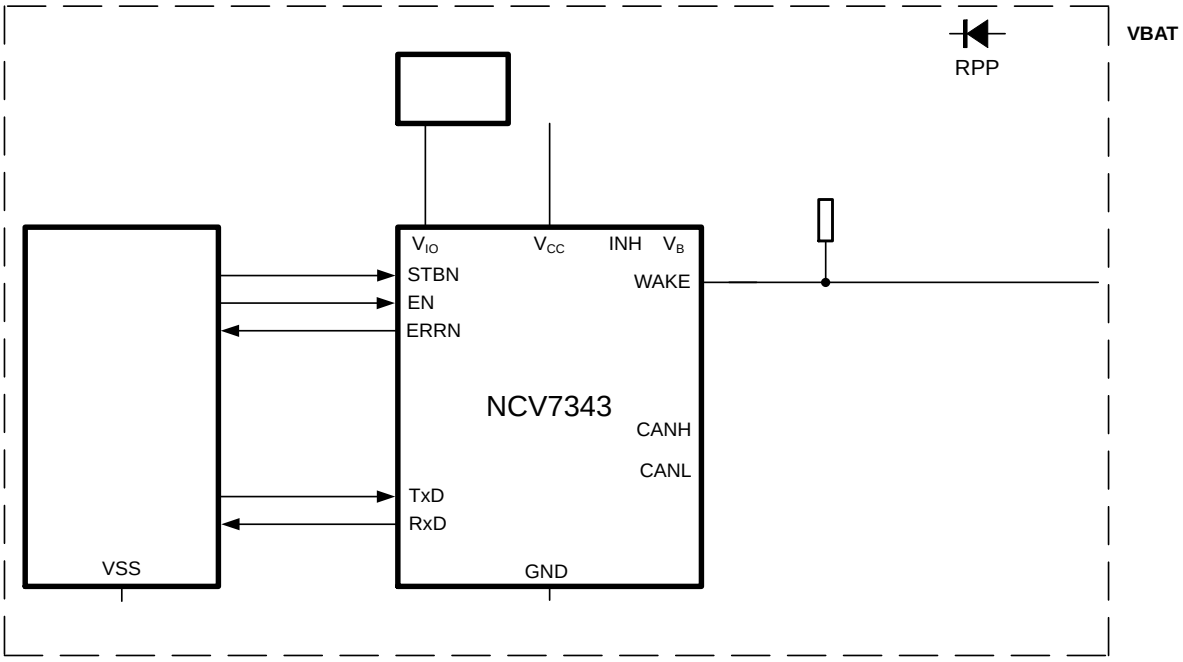
Quality

- Wettable Flank Package for Enhanced Optical Inspection

Typical Applications

- Automotive
- Industrial Networks

TYPICAL APPLICATION



BLOCK DIAGRAM

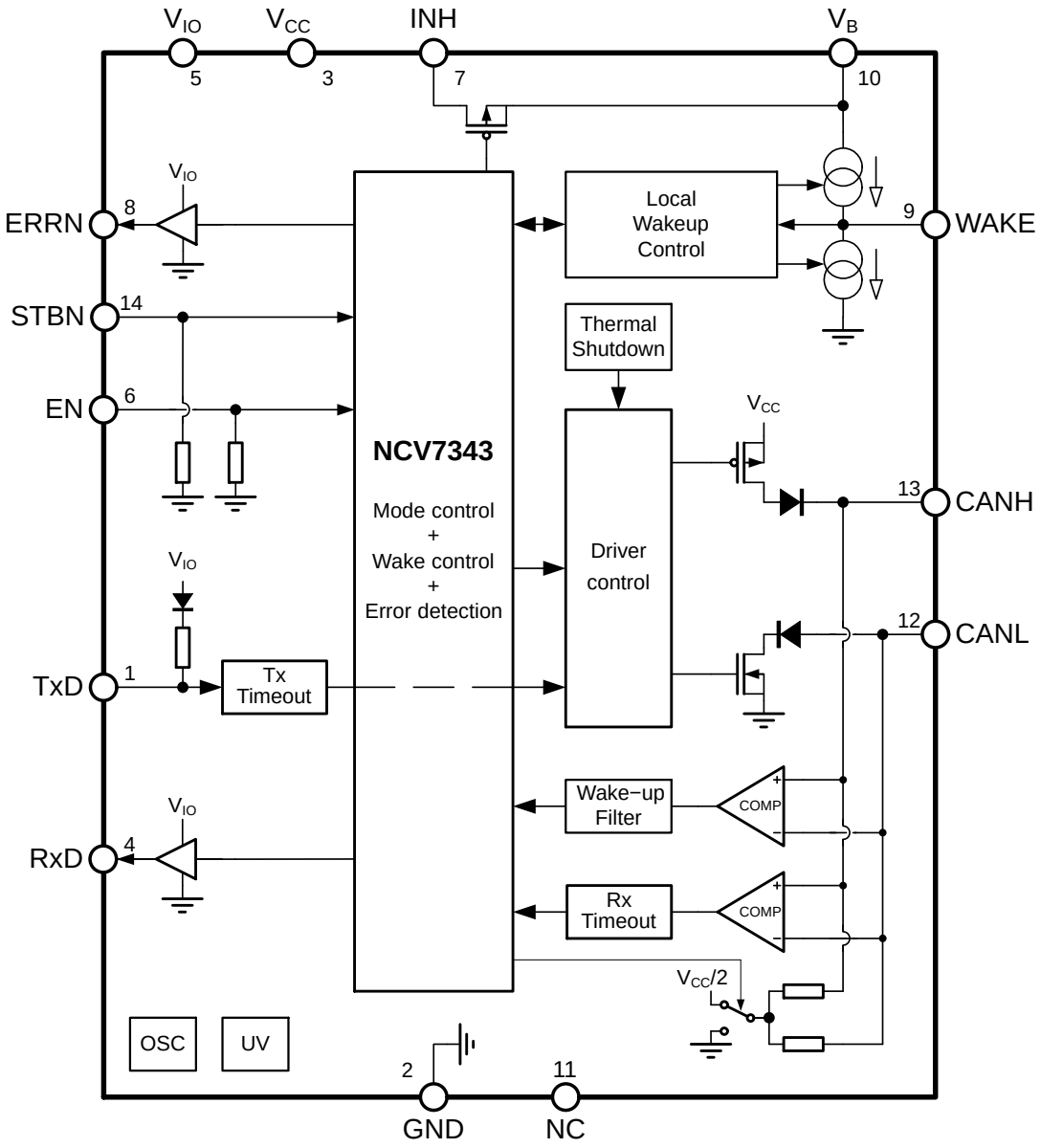
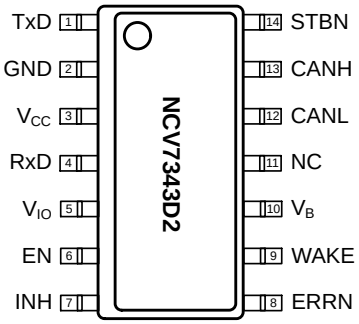
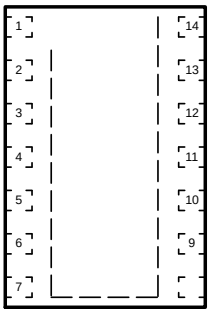


Figure 2. NCV7343 Block Diagram

PIN CONNECTIONS





MAXIMUM RATINGS (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{ESD_INT}	Electrostatic Discharge Voltage at All Other Pins; Component HBM, According to JEDEC JESD22−A114.	(Note 4)	−4	+4	kV
V_{ESD_CDM}	Electrostatic Discharge Voltage at All Pins; Component CDM, According to JEDEC JESD22−C101.		−750	+750	V
V_{ESD_MM}	Electrostatic Discharge Voltage at All Pins; Component MM, According to JEDEC JESD22−A115.	(Note 5)	−200	+200	V
V_{TRAN}	Voltage Transients, Pins CANH, CANL. Test Pulses According to ISO7637−2, Class C, (Note 6)	Test pulses 1	−100	−	V
		Test pulses 2a	−	+75	V
		Test pulses 3a	−150	−	V
		Test pulses 3b	−	+100	V
	Voltage Transients, Pin V_B, According to ISO7637−2	Test pulse 5 Load dump	−	40	V
Latch−up	Static Latch−up at All Pins, According to JEDEC JESD78		−	150	mA
T_J	Maximum Junction Temperature		−40	+160	°C
T_{STG}	Storage Temperature		−55	+150	°C
MSL	Moisture Sensitivity Level	SOIC−14	2		
		DFNW14	1		
T_{SLD}	Peak Soldering Temperature (Note 7)		−	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
3. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor, referenced to GND. WAKE pin stressed through an external series resistor 3.3 kΩ and with 10 nF capacitor on the module input. VB pin decoupled with 100 nF during stressing. Results were verified by an external test house.
4. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
5. Equivalent to discharging a 200 pF capacitor through a 10 Ω resistor and 0.75 μH coil.
6. Results were verified by an external test house.
7. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, SOIC−14 (Note 8) Thermal Resistance Junction−to−Air, (Note 9) Thermal Resistance Junction−to−Air, (Note 10)	$R_{\theta JA\_1}$ $R_{\theta JA\_2}$	100 63	K/W
Thermal Characteristics, DFNW14 (Note 8) Thermal Resistance Junction−to−Air, (Note 9) Thermal Resistance Junction−to−Air, (Note 10)	$R_{\theta JA\_1}$ $R_{\theta JA\_2}$	115 65	K/W

8. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
9. Test board according to EIA/JEDEC Standard JESD51−3 (1S0P PCB), signal layer with 10% trace coverage.
10. Test board according to EIA/JEDEC Standard JESD51−7 (2S2P PCB), signal layers with 10% trace coverage.

RECOMMENDED OPERATING RANGES

Symbol	Parameter	Conditions	Min	Max	Unit
V_B	Supply Voltage, Pin V_B		5.0	40	V
V_{CC}	Supply Voltage, Pin V_{CC}		4.5	5.5	V
V_{IO}	Supply Voltage, Pin V_{IO}		2.8	5.5	V
V_{CAN}	DC Voltage at Pins CANH and CANL		−36	36	V
V_{DIG_IN}	DC Voltage at Pins TxD, STBN, and EN		0	5.5	V
V_{DIG_OUT}	DC Voltage at Pins RxD and ERRN		0	V_{IO}	V
V_{INH}, 27.2835 0 m.0CurracitorH 59.754 0l	DC Voltage at Pin INH				

RECOMMENDED OPERATING RANGES (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{WAKE}	DC Voltage at Pin WAKE		−42	V_B	V
T_J	Junction Temperature		−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8 V to 5.5 V; V_B= 5.0 V to 40 V; for typical values T_A = 25° C, for min/max values T_J = −40 to +150° C; R_{LT} = 60 Ω, C_{RxD} = 15 pF; unless otherwise noted. All voltages are referenced to GND (pin 2). Positive current flow into the respective pin) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_B SUPPLY VOLTAGE (Pin V_B)						
V_{uvd_VB}	Undervoltage Detection Threshold	V_B falling	3.7	4.1	4.5	V
V_{uvr_VB}	Undervoltage Recovery Threshold	V_B rising	3.9	4.4	4.9	V
V_{uvh_VB}	Undervoltage Threshold Hysteresis		100	300	400	mV
TRANSMITTER DATA INPUT (PIN TxD)						
V_{IH}	High−level Input Voltage	Output recessive	2.0	−	−	V
V_{IL}	Low−level Input Voltage	Output dominant	−	−	0.8	V
I_{IH}	High−level Input Current	V_{TxD} = V_{IO}	−5.0	0	+5.0	μA
R_{PU}	Pull−up Resistor		10	25	50	kΩ
I_{LEAK}	Leakage Current	V_{TxD} = 5.5 V, V_{IO} = 0 V	−1.0	0	+1.0	μA
C_i	Input Capacitance	(Note 11)	−	5	10	pF
RECEIVER DATA OUTPUT (Pin RxD)						
I_{OH}	High−level Output Current	V_{RxD} = V_{IO} − 0.4 V	−8.0	−3.0	−1.0	mA
I_{OL}	Low−level Output Current	V_{RxD} = 0.4 V	1.0	6.0	12	mA
TRANSMITTER MODE SELECT (Pin STBN, EN)						
V_{IH}	High−level Input Voltage	Standby mode	2.0	−	−	V
V_{IL}	Low−level Input Voltage	Normal mode	−	−	0.8	V
R_{PD}	Pull−down Resistor		300	650	1000	kΩ
I_{IL}	Low−level Input Current	V_{STBN} = 0 V	−1.0	0	+1.0	μA
I_{LEAK}	Leakage Current	V_{STBN} = 5.5 V, V_B = V_{CC} = V_{IO} = 0 V	−1.0	0	+1.0	μA
C_i	Input Capacitance	(Note 11)	−	5	10	pF
ERROR SIGNALING (Pin ERRN)						
I_{OH}	High Level Output Current	V_{ERRN} = V_{IO} − 0.4 V	−100	−50	−10	μA
I_{OL}	Low Level Output Current	V_{ERRN} = 0.4 V	0.1	0.5	1.0	mA
LOCAL WAKE−UP INPUT (Pin WAKE)						
V_{IH}	High−level Input Voltage	Standby or Sleep	V_B − 2	−	−	V
V_{IL}	Low−level Input Voltage	Standby or Sleep	−	−	V_B − 4	V
I_{IH}	High−level Input Current	V_{WAKE} = V_B − 2 V; V_{WAKE} = High for t ≥ t_{wake_filt} (Pull−up active)	−11	−	−3.0	μA
I_{IL}	Low−level Input Current	V_{WAKE} = V_B − 4 V; V_{WAKE} = Low for t ≥ t_{wake_filt} (Pull−down active)	3.0	−	11	μA
INHIBIT OUTPUT (Pin INH)						
V_{OH}	High−level Output Voltage	I_{INH} = −1 mA	V_B − 0.6	V_B − 0.27	V_B − 0.1	V
I_{LEA}	[redacted]ge Current	Sleep or Power−off mode, V_{INH} = 0 V	−5	0	+5	μA
CAN [redacted]s CANH and CANL)						
$V_{o(dom)(CANH)}$	[redacted]nant Output Voltage at Pin CANH	Normal mode; V_{TxD} = Low; t < $t_{dom(TxD)}$; 45 Ω ≤ R_{LT} ≤ 65 Ωt	2.75	3.65	4.5	

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8 V to 5.5 V; V_B= 5.0 V to 40 V; for typical values T_A = 25° C, for min/max values T_J = −40 to +150° C; R_{LT} = 60 Ω, C_{RxD} = 15 pF; unless otherwise noted. All voltages are referenced to GND (pin 2). Positive current flow into the respective pin) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CAN TRANSMITTER (Pins CANH and CANL)						
$V_{o(dom)(CANL)}$	Dominant Output Voltage at Pin CANL	Normal mode; V_{TxD} = Low; $t < t_{dom(TxD)}$; 45 Ω ≤ R_{LT} ≤ 65 Ω	0.5	1.35	2.25	V
$V_{o(rec)}$	Recessive Output Voltage at Pins CANH and CANL	Normal or Silent mode; V_{TxD} = High or V_{TxD} = Low and $t > t_{dom(TxD)}$; no load	2.0	2.5	3.0	V
$V_{o(off)}$	Recessive Output Voltage at Pins CANH and CANL	Standby or Sleep mode; no load	−0.1	0	+0.1	V
$V_{o(dom)(diff)}$	Differential Dominant Output Voltage ($V_{CANH} - V_{CANL}$)	Normal mode; V_{TxD} = Low; $t < t_{dom(TxD)}$; 50 Ω ≤ R_{LT} ≤ 65 Ω	1.5	2.3	3.0	V
$V_{o(dom)(diff)\_E}$		Normal mode; V_{TxD} = Low; $t < t_{dom(TxD)}$; 45 Ω ≤ R_{LT} ≤ 70 Ω	1.4	2.3	3.3	V
$V_{o(dom)(diff)\_ARB}$		Normal mode; V_{TxD} = Low; $t < t_{dom(TxD)}$; R_{LT} = 2 240 Ω	1.5	−	5.0	V
$V_{o(rec)(diff)}$	Differential Recessive Output Voltage ($V_{CANH} - V_{CANL}$)	Normal or Silent mode; V_{TxD} = High or V_{TxD} = Low and $t > t_{dom(TxD)}$; no load;r90707 refq415.2193 71.717 .90707 r45W nBT/F2Tc(CANH)Tj8 0 00707 r45W n77 ref0.0	−50			

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8 V to 5.5 V; V_B= 5.0 V to 40 V; for typical values T_A = 25° C, for min/max values T_J = −40 to +150° C; R_{LT} = 60 Ω, C_{RxD} = 15 pF; unless otherwise noted. All voltages are referenced to GND (pin 2). Positive current flow into the respective pin) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit

272.8063 rem.0041

FUNCTIONAL DESCRIPTION

POWER SUPPLY

NCV7343 implements three power supply inputs – battery supply input V_B, CAN transceiver supply input V_{CC} and digital IOs supply input V_{IO}.

V_B Supply Pin

V_B is the main supply pin of the NCV7343. The NCV7343 proceeds from Power−off mode to Standby mode as soon as the V_B supply is available. This supply input is used to provide the minimum power required for the operation in case of absence of the remaining supplies. Typically this is the only active supply in a low−power Sleep mode providing power supply to the low−power wake−up detector.

V_{CC} Supply Pin

V_{CC} pin is the CAN transceiver main supply input in Normal and Silent mode.

V_{IO} Supply Pin

Digital pins interfacing with the microcontroller have a separate IO supply. The V_{IO} pin should be connected to microcontroller supply pin. By using V_{IO} supply pin shared with microcontroller the IO levels between microcontroller and transceiver are properly adjusted. See Figure 1.

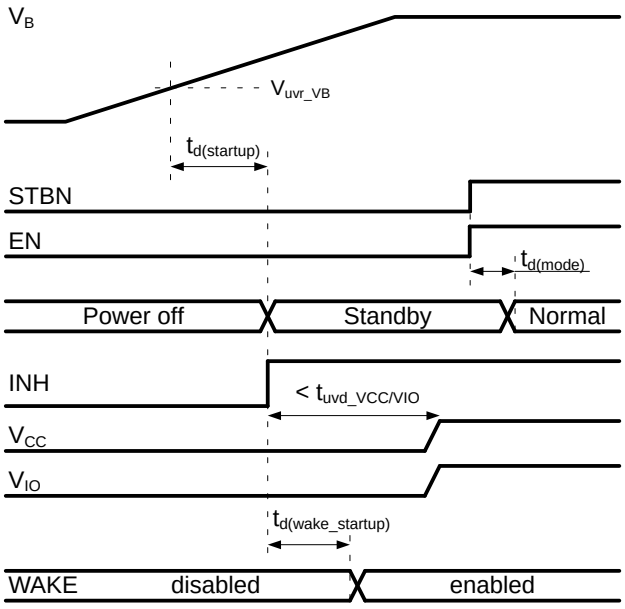


Figure 5. Typical Power−up Sequence

Power Supplies Monitoring

V_B, V_{CC} and V_{IO} supply inputs are monitored by undervoltage detectors with individual thresholds and filtering times both for undervoltage detection and undervoltage recovery.

In Normal mode, the transmitter is disabled t_{uv_det} after V_{CC} or V_{IO} voltage falls below respective undervoltage detection thresholds. The transmitter is re−enabled t_{uv_rec} after both V_{CC} and V_{IO} voltage rises above the undervoltage recovery thresholds (Figure 6).

V_B undervoltage is detected if V_B supply voltage falls below undervoltage detection threshold, V_{uvd_VB}. V_B undervoltage recovery is detected if V_B supply voltage rises above the undervoltage recovery threshold, V_{uvr_VB}.

V_{CC} undervoltage flag is set if V_{CC} supply voltage is lower than V_{uv_VCC} for longer than V_{CC} undervoltage detection time t_{uvd_VCC}. V_{CC} undervoltage recovery is detected and the flag is reset if V_{CC} supply voltage is higher than V_{uv_VCC} for longer than V_{CC} undervoltage recovery time t_{uvr_VCC}.

Similarly, V_{IO} undervoltage flag is set if V_{IO} supply voltage is lower than V_{uv_VIO} for longer than V_{IO} undervoltage detection time t_{uvd_VIO}. V_{IO} undervoltage recovery is detected and the flag is reset if V_{IO} supply voltage is higher than V_{uv_VIO} for longer than V_{IO} undervoltage recovery time t_{uvr_VIO}.

Both V_{CC} and V_{IO} undervoltage flags and the undervoltage detection timers are also reset after local or remote wake−up detection event or STBN pin rising edge detection in Sleep mode.

Once the V_{CC} and/or V_{IO} undervoltage flag is set the device changes to Sleep mode. The Sleep mode can be left and the operation mode control by STBN and EN pin is re−enabled as soon as both V_{CC} and V_{IO} supplies are recovered. The operating mode control state machine is not reset when an undervoltage condition is detected. Thus if Sleep mode was requested by the host prior to V_{CC} and/or V_{IO} undervoltage condition detection and the EN pin was set Low in Sleep mode, the device stays in Sleep once the undervoltage is recovered, although STBN and EN pins are both set Low, which is otherwise considered a Standby mode request.

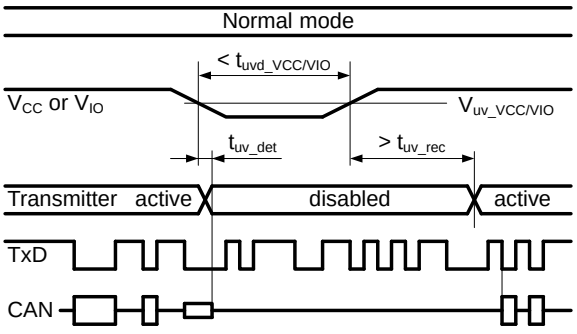


Figure 6. Transmitter Deactivation/Activation in Case of Undervoltage Event

INH Pin

The INH output pin is a high−voltage high−side switch to V_B supply. It can be used to control the V_{CC} or V_{IO} external supply voltage regulators. The output is switched high in all operating modes except for the Sleep mode. In Sleep mode the pin is left floating (high−impedance) which can be used to deactivate the external regulators in order to minimize the ECU current consumption. The INH switch is also deactivated in Power−off mode.

HIGH SPEED CAN TRANSCEIVER

NCV7343 implements high−speed physical layer CAN FD transceiver compatible with ISO11898−2:2016, implementing following optional features or alternatives:

Extended bus load range

Transmit dominant timeout, long

Support of bit rates up to 5 Mbit/s

Low−power modes with wake−up via wake−up pattern,

Short CAN activity filter time and long wake−up

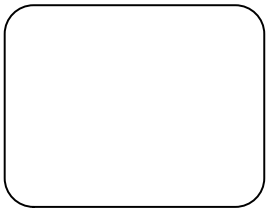


Figure 11. Operation Modes

WAKE−UP

A Wake−up flag is set if Local wake−up via WAKE pin (positive or negative edge) is detected or Remote wake−up via bus (wake−up pattern) is detected. If the Wake−up flag is set in Sleep mode, the device changes to Standby mode. Undervoltage detection flags are cleared and the corresponding timers are restarted upon detection

FAILURE DETECTION

Local Failures

A Local failure flag is set if any of the flowing flags are set:

TxD Dominant Timeout

Bus Dominant Timeout

Short−TxD to RxD

Overtemperature Detection

The local failure flag is signaled on ERRN pin in Silent mode entered from Normal mode. The flag is cleared if all of the mentioned flags are cleared.

TxD Dominant Timeout

A TxD dominant timeout timer circuit prevents the bus lines being driven to a permanent dominant state if pin TxD is forced permanently low. The timer is triggered by a negative edge on pin TxD in Normal mode. If the duration

INTERNAL FLAGS AND THEIR VISIBILITY

Internal Flag	Set Conditions	Reset Conditions	Visibility on ERRN Pin
V_{CC} or V_{IO} Undervoltage	$V_{CC} < V_{uv\_VCC}$ for $t > t_{uvd\_VCC}$ or $V_{IO} < V_{uv\_VIO}$ for $t > t_{uvd\_VIO}$	($V_{CC} > V_{uv\_VCC}$ for $t > t_{uvr\_VCC}$ and $V_{IO} > V_{uv\_VIO}$ for $t > t_{uvr\_VIO}$	

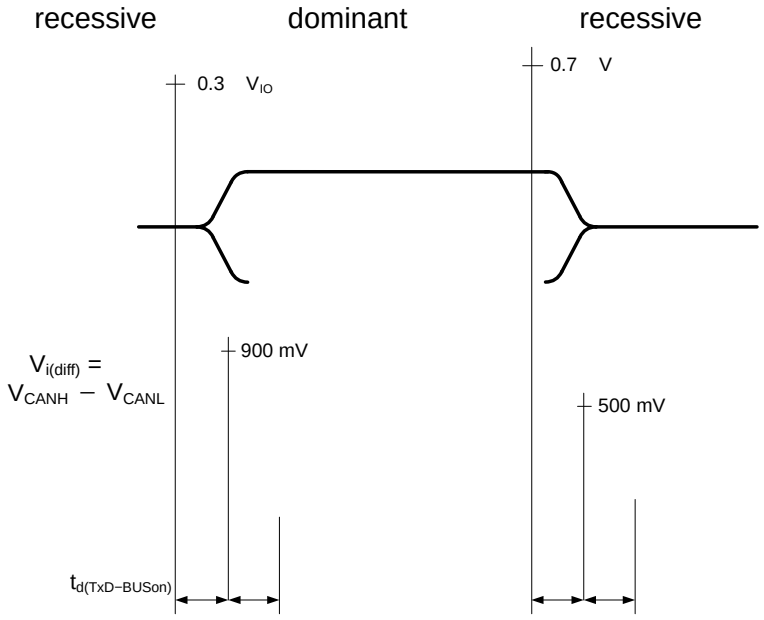
FAIL SAFE

A current−limiting circuit protects the transmitter output stage from damage caused by accidental short circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

Undervoltage on supply pins prevents the chip from sending data on the bus when there is not enough V_{CC} supply voltage to build required bus differential voltage, or when V_{IO} supply voltage is low and thus the digital input or output signals might be interpreted falsely. After supply is recovered TxD pin must be first released to High to allow sending dominant bits again.

The pins CANH and CANL are protected from automotive electrical transients (according to ISO 7637; see Figure 19). Pin TxD is pulled high and pins STBN and EN are pulled low internally should the input become disconnected. Digital pins, TxD, STBN and EN will be floating, preventing reverse supply should the V_{IO} supply be removed. RxD and ERRN have forward diode to V_{IO} supply.

MEASUREMENT SETUPS AND DEFINITIONS



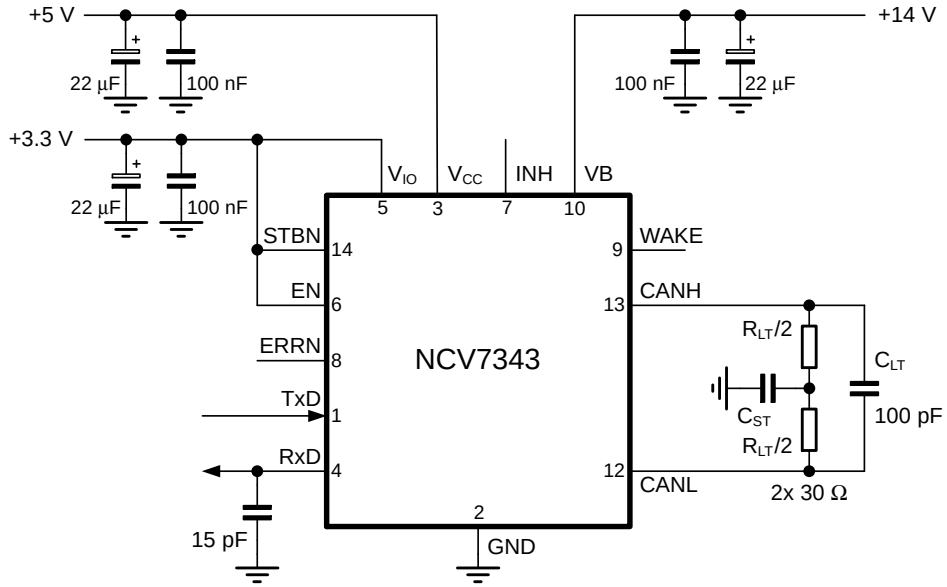
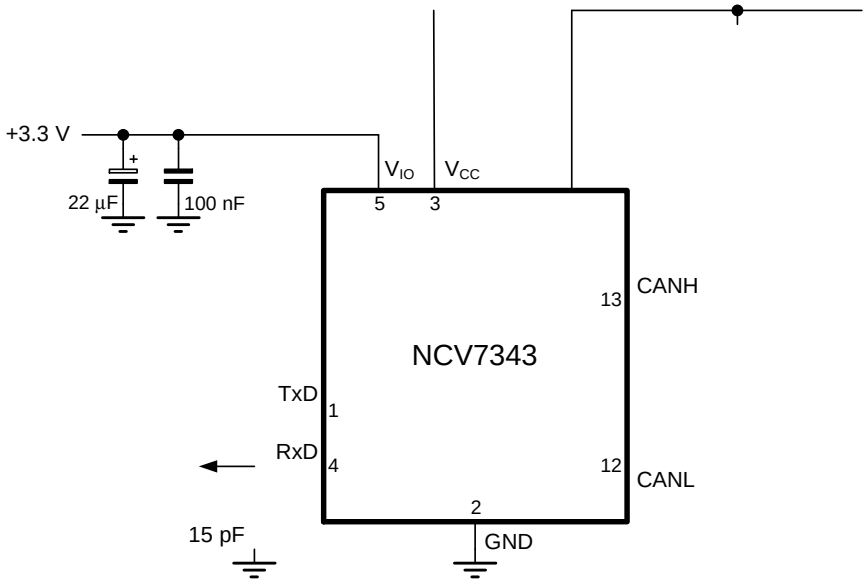


Figure 18. Test Circuit for Timing Characteristics



ISO 11898−2:2016 PARAMETER CROSS−REFERENCE TABLE (continued)

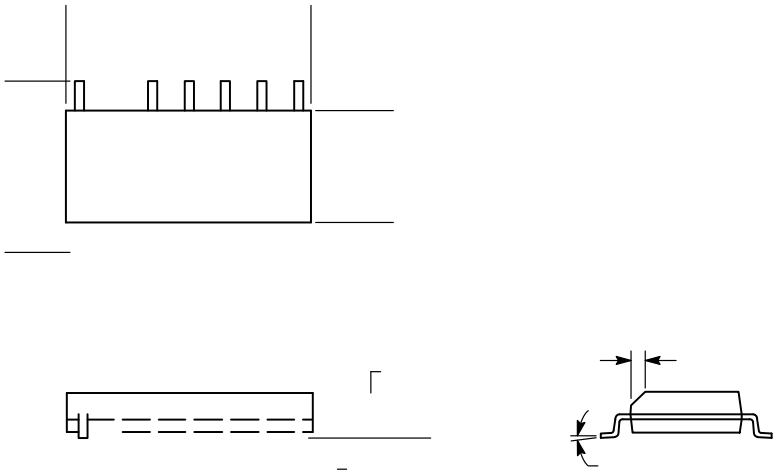
Parameter	Notation	Symbol
DATA SIGNAL TIMING REQUIREMENTS FOR USE WITH BIT RATES ABOVE 2 Mbit/s AND UP TO 5 Mbit/s		
Transmitted Recessive Bit Width @ 5 Mbit/s	$t_{Bit(Bus)}$	$t_{bit(Vi(diff))}$
Received Recessive Bit Width @ 5 Mbit/s	$t_{Bit(RXD)}$	$t_{bit(RxD)}$
Receiver Timing Symmetry @ 5 Mbit/s	Δt_{Rec}	Δt_{rec}
MAXIMUM RATINGS OF V_{CAN_H}, V_{CAN_L} AND V_{Diff}		
Maximum Rating V_{Diff}	V_{Diff}	V_{Diff}
General Maximum Rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H} V_{CAN_L}	V_{CAN} V_{CAN}
Optional: Extended Maximum Rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H} V_{CAN_L}	NA
MAXIMUM LEAKAGE CURRENTS ON CAN_H and CAN_L, UNPOWERED		
Leakage Current on CAN_H, CAN_L	I_{CAN_H} I_{CAN_L}	$I_{LEAK(off)}$
BUS BIASING CONTROL TIMINGS		
CAN Activity Filter Time, Long	t_{Filter}	NA
CAN Activity Filter Time, Short	t_{Filter}	t_{wup_filt}
Wake−up Timeout, Short	t_{Wake}	NA
Wake−up Timeout, Long	t_{Wake}	t_{wup_to}
Timeout for Bus Inactivity (Required for Selective Wake−up Implementation Only)	$t_{Silence}$	NA
Bus Bias Reaction Time (Required for Selective Wake−up Implementation Only)	t_{Bias}	NA

Table 1. ORDERING INFORMATION

Part Number	Description	Package	Shipping†
NCV7343D20R2G	CAN FD Transceiver, High Speed, Low Power, with WAKE, INH and V_{IO} Pin	SOIC−14 (Pb−free)	3000 / Tape & Reel
NCV7343MW0R2G	CAN FD Transceiver, High Speed, Low Power, with WAKE, INH and V_{IO} Pin	DFNW14 Wettable Flank (Pb−free)	5000 / Tape & Reel
NCV7343D21R2G	CAN FD Transceiver, High Speed, Low Power, with WAKE, INH and V_{IO}		

PACKAGE DIMENSIONS

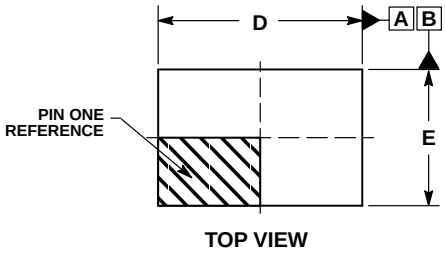
SOIC−14 NB
CASE 751A−03
ISSUE L



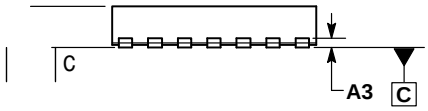
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

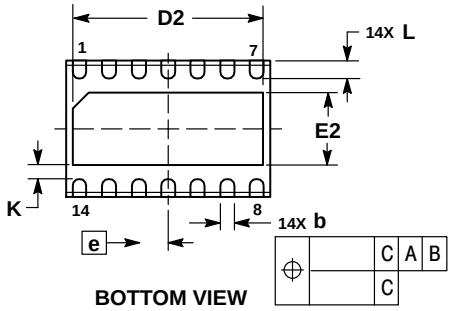
PACKAGE DIMENSIONS

DFNW14 4.5x3, 0.65P
CASE 507AC
ISSUE D



TOP VIEW





BOTTOM VIEW

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMESNION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

SOLDERING FOOTPRINT*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.