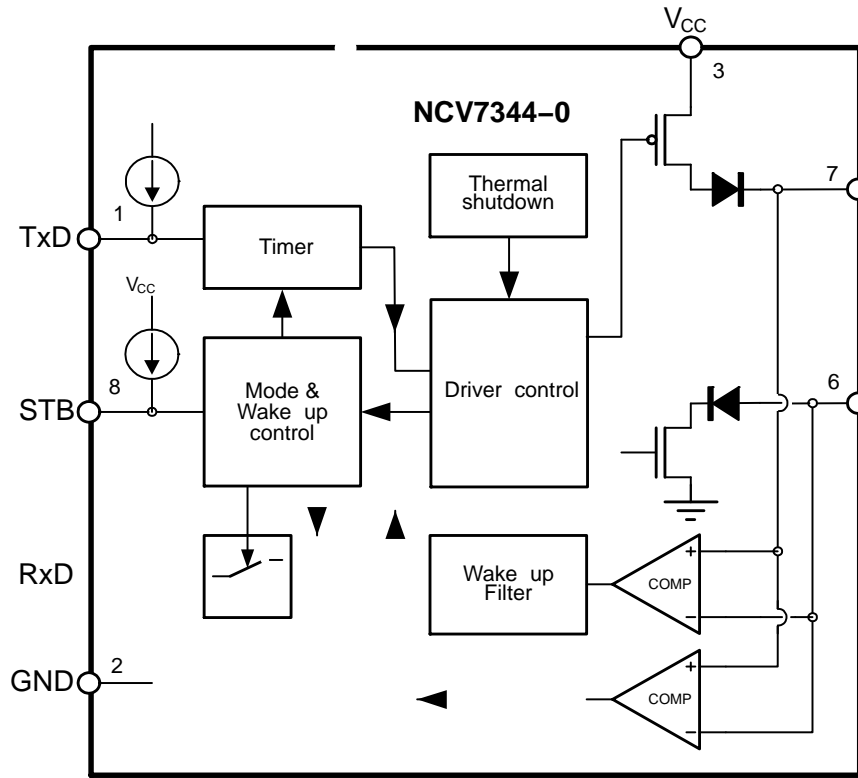




NCV7344

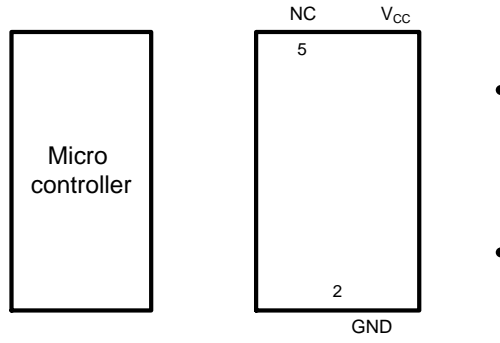
BLOCK DIAGRAM



NCV7344

TYPICAL APPLICATION

VBAT _____



NCV7344

ELECTRICAL CHARACTERISTICS

Definitions

All voltages are referenced to GND (pin 2). Positive currents flow into the IC. Sinking current means the current is flowing into the pin; sourcing current means the current is flowing out of the pin.

ABSOLUTE MAXIMUM RATINGS

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{SUP}	Supply voltage V_{CC} , V_{IO}		0.3	+6	V
V_{CANH}	DC voltage at pin CANH	$0 < V_{CC} < 5.25$ V; no time limit			

NCV7344

Table 5. ELECTRICAL CHARACTERISTICS $V_{CC} = 4.75\text{ V to }5.25\text{ V}$; $V_{IO} = 2.8\text{ to }5.25\text{ V}$; $T_J = -40\text{ to }+150^\circ\text{C}$; $R_{LT} = 60\ \Omega$, $C_{LT} = 100\text{ pF}$, C_1 not used, $C_{RxD} = 15\text{ pF}$ unless specified otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BUS LINES (Pins CANH and CANL)						
$V_{o(off)}(CANL)$	Recessive output voltage at pin CANL	Standby mode; R_{LT} and C_{LT} not used	0.1	0	0.1	V
$V_{o(off)}(diff)$	Differential bus output voltage ($V_{CANH} - V_{CANL}$)	Standby mode; R_{LT} and C_{LT} not used	0.2	0	0.2	V
$V_{o(dom)}(CANH)$	Dominant output voltage at pin CANH	$V_{TxD} = 0\text{ V}$; $t < t_{dom}(TxD)$; $50\ \Omega < R_{LT} < 65\ \Omega$	2.75	3.5	4.5	V
$V_{o(dom)}(CANL)$	Dominant output voltage at pin CANL	$V_{TxD} = 0\text{ V}$; $t < t_{dom}(TxD)$; $50\ \Omega < R_{LT} <$				

NCV7344

Table 5. ELECTRICAL CHARACTERISTICS $V_{CC} = 4.75\text{ V to }5.25\text{ V}$; $V_{IO} = 2.8\text{ to }5.25\text{ V}$; $T_J = 40\text{ to }+150^\circ\text{C}$; $R_{LT} = 60\ \Omega$, $C_{LT} = 100\text{ pF}$, C_1 not used, $C_{RxD} = 15\text{ pF}$ unless specified otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TIMING CHARACTERISTICS (see Figures 6 and 8)						
$t_{d(TxD\ BUSon)}$	Delay TxD to bus active			75		ns
$t_{d(TxD\ BUSoff)}$	Delay TxD to bus inactive			85		ns
$t_{d(BUSon\ RxD)}$	Delay bus active to RxD			24		ns
$t_{d(BUSoff\ RxD)}$	Delay bus inactive to RxD			32		ns
t_{pd_dr}	Propagation delay TxD to RxD dominant to recessive transition		50	100	210	ns
t_{pd_rd}	Propagation delay TxD to RxD recessive to dominant transition		50	120	210	ns
$t_{d(stb\ nm)}$	Delay standby mode to normal mode		5	11	20	μs
t_{wake_filt}	Filter time for wake up via bus	NCV7344 version	0.5		5	μs
		NCV7344A version	0.15		1.8	μs
$t_{dwakerd}$	Delay to flag wake event (recessive to dominant transitions)	Valid bus wake up event	0.5	2.6	6	μs
$t_{dwakedr}$	Delay to flag wake event (dominant to recessive transitions)	Valid bus wake up event	0.5	2.6	6	μs
t_{wake_to}	Bus time for wake up timeout	Standby mode	1		10	ms
$t_{dom(TxD)}$	TxD dominant time for timeout	$V_{TxD} = \text{Low}; \text{Normal mode}$	1		10	ms
$t_{Bit(RxD)}$	Bit time on RxD pin	$t_{Bit(TxD)} = 500\text{ ns}$	400		550	ns
		$t_{Bit(TxD)} = 200\text{ ns}$	120		220	ns
$t_{Bit(VI(diff))}$	Bit time on bus (CANH – CANL pin)	$t_{Bit(TxD)} = 500\text{ ns}$				

NCV7344

MEASUREMENT SETUPS AND DEFINITIONS

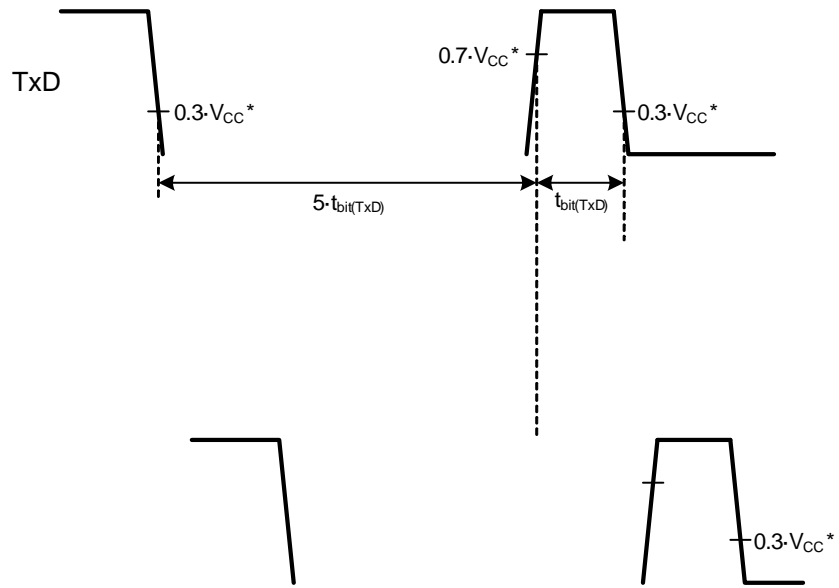


Table 6. ISO 11898–2:2016 Parameter Cross–Reference Table

ISO 11898–2:2016 Specification		NCV7344 Datasheet	
Parameter	Notation	Symbol	
Dominant output characteristics			
Single ended voltage on CAN_H	V_{CAN_H}	$V_{o(dom)}(CANH)$	
Single ended voltage on CAN_L	V_{CAN_L}	$V_{o(dom)}(CANL)$	
Differential voltage on normal bus load	V_{Diff}	$V_{o(dom)}(diff)$	
Differential voltage on effective resistance during arbitration	V_{Diff}	$V_{o(dom)}(diff_arb)$	
Differential voltage on extended bus load range (optional)	V_{Diff}	$V_{o(dom)}(diff)$	
Driver symmetry			
Driver symmetry	V_{SYM}	$V_{o(dom)}(sym)$	
Driver output current			
Absolute current on CAN_H	I_{CAN_H}	$I_o(SC)(CANH)$	
Absolute current on CAN_L	I_{CAN_L}	$I_o(SC)(CANL)$	
Receiver output characteristics, bus biasing active			
Single ended output voltage on CAN_H	V_{CAN_H}	$V_{o(rec)}(CANH)$	
Single ended output voltage on CAN_L	V_{CAN_L}	$V_{o(rec)}(CANL)$	
Differential output voltage	V_{Diff}	$V_{o(rec)}(diff)$	
Receiver output characteristics, bus biasing inactive			
Single ended output voltage on CAN_H	V_{CAN_H}	$V_{o(off)}(CANH)$	
Single ended output voltage on CAN_L	V_{CAN_L}	$V_{o(off)}(CANL)$	
Differential output voltage	V_{Diff}	$V_{o(off)}(diff)$	
Optional transmit dominant timeout			
Transmit dominant timeout, long	t_{dom}	$t_{dom}(TxD)$	
Transmit dominant timeout, short	t_{dom}	NA	
Static receiver input characteristics, bus biasing active			
Recessive state differential input voltage range	V_{Diff}	$V_{i(rec)}(diff)_NM$	
Dominant state differential input voltage range	V_{Diff}	$V_{i(dom)}(diff)_NM$	
Static receiver input characteristics, bus biasing inactive			
Recessive state differential input voltage range	V_{Diff}	$V_{i(rec)}(diff)_LP$	
Dominant state differential input voltage range	V_{Diff}	$V_{i(dom)}(diff)_LP$	
Receiver input resistance			
Differential internal resistance	R_{Diff}	$R_{i(diff)}$	
Single ended internal resistance	R_{CAN_H} R_{CAN_L}	$R_{i(cm)}(CANH)$ $R_{i(cm)}(CANL)$	
Receiver input resistance matching			
Matching a of internal resistance	m_R	$R_{i(cm)}(m)$	
Implementation loop delay requirement			
Loop delay	t_{Loop}	t_{pd_rd} t_{pd_dr}	
Optional implementation data signal timing requirements for use with bit rates above 1 Mbit/s and up to 2 Mbit/s			
Transmitted recessive bit width @ 2 Mbit/s	$t_{Bit}(Bus)$	$t_{Bit}(Vi(diff))$	
Received recessive bit width @ 2 Mbit/s	$t_{Bit}(RXD)$	$t_{Bit}(RxD)$	

NCV7344

Table 6. ISO 11898–2:2016 Parameter Cross–Reference Table

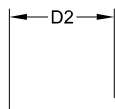
Parameter	Notation	Symbol
Receiver timing symmetry @ 2 Mbit/s	Δt_{Rec}	Δt_{Rec}



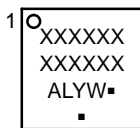
SCALE 2:1

DFNW8 3x3, 0.65P
CASE 507AB
ISSUE E

DATE 02 JUL 2021



**GENERIC
MARKING DIAGRAM***



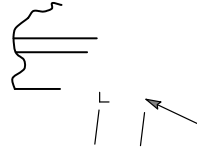
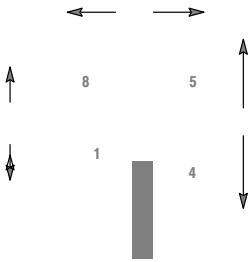
- XXXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

SOIC 8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011



SEATING
PLANE



onsemi, **onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi**
