



# NCV7357

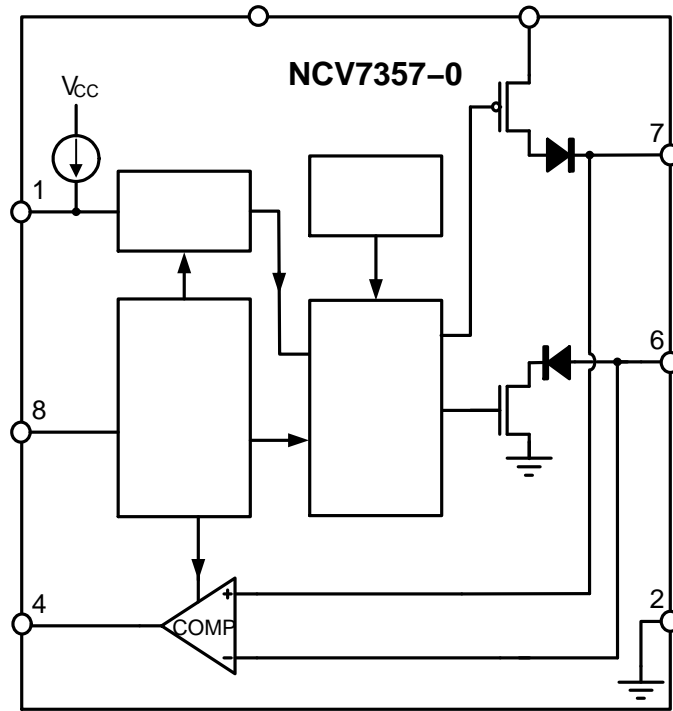
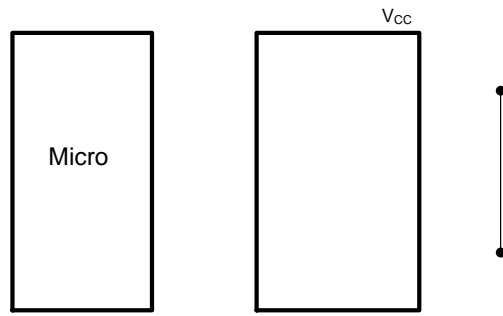


Figure 1. NCV7357-0 Block Diagram

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## FUNCTIONAL DESCRIPTION

### High speed CAN FD transceiver

NCV7357 implements high-speed physical layer CAN FD transceiver compatible with ISO11898-2, implementing following optional features or alternatives:

- Extended bus load range
- Transmit dominant timeout, long
- Support of bit rates up to 5 Mbps
- Normal Bus biasing

### Operating Modes

NCV7357 provides two modes of operation as illustrated in Table 2. These modes are selectable through pin S.

**Table 2. OPERATING MODES**

Pin S	Mode	Pin TxD	BUS	Pin RxD
Low	Normal	0	Dominant	0
		1	Recessive	1
High	Silent	X	Dominant (1)	0
		X	Recessive	1

1. CAN BUS driven by another transceiver on the BUS

2. 'X' = don't care

### Power-off

This virtual mode is entered as soon as the  $V_{CC}$  or  $V_{IO}$  undervoltage condition is detected. The internal logic is reset and the transceiver is disabled. CAN bus pins are kept floating. As soon as both  $V_{CC}$  and  $V_{IO}$  voltages rise above corresponding undervoltage recovery thresholds, the device proceeds to Normal or Silent mode, depending on S pin state.

state.

Figure 7). Pins TxD and S are biased internally should the input become disconnected. Pins TxD, S and RxD will be floating, preventing reverse supply should the VCC supply be removed.

**V**



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**Table 5. ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 4.75\text{ V to }5.25\text{ V}$ ;  $V_{IO} = 2.8\text{ V to }5.5\text{ V}$ ; for typical values  $T_A = 25^\circ\text{C}$ , for min/max values  $T_J = -40\text{ to }+150^\circ\text{C}$ ;  $R_{LT} = 60\ \Omega$ ,  $C_{RxD} = 15\text{ pF}$ ; unless otherwise noted. All voltages are referenced to GND (pin 2). Positive currents flow into the respective pin)

### RECEIVER DATA OUTPUT (Pin RxD)

$I_{OH}$	High level output current	Normal mode $V_{RxD} = V_{CC} / V_{IO} - 0.4\text{ V}$	8.0	3.0	1.0	mA
$I_{OL}$	Low level output current	$V_{RxD} = 0.4\text{ V}$	1.0	6.0	12	mA

### CAN TRANSMITTER (PINS CANH AND CANL)

$V_{o(dom)}(CANH)$	Dominant output voltage at pin CANH	Normal mode; $V_{TxD} = \text{Low}$ ; $t < t_{dom}(TxD)$ ; $50\ \Omega < R_{LT} < 65\ \Omega$	2.75	3.5	4.5	V
$V_{o(dom)}(CANL)$	Dominant output voltage at pin CANL	Normal mode; $V_{TxD} = \text{Low}$ ; $t < t_{dom}(TxD)$ ; $50\ \Omega < R_{LT} < 65\ \Omega$	0.5	1.5	2.25	V
$V_{o(rec)}$	Recessive output voltage at pins CANH and CANL	Normal or Silent mode; $V_{TxD} = \text{High}$ or $V_{TxD} = \text{Low}$ and $t > t_{dom}(TxD)$ ; no load	2.0	2.5	3.0	V
$V_{o(dom)}(diff)$	Differential dominant output voltage ( $V_{CANH} - V_{CANL}$ )	Normal mode; $V_{TxD} = \text{Low}$ ; $t < t_{dom}(TxD)$ ; $45\ \Omega < R_{LT} < 65\ \Omega$	1.5			

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**Table 5. ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 4.75\text{ V to }5.25\text{ V}$ ;  $V_{IO} = 2.8\text{ V to }5.5\text{ V}$ ; for typical values  $T_A = 25^\circ\text{C}$ , for min/max values  $T_J = -40\text{ to }+150^\circ\text{C}$ ;  $R_{LT} = 60\ \Omega$ ,  $C_{RxD} = 15\text{ pF}$ ; unless otherwise noted. All voltages are referenced to GND (pin 2). Positive currents flow into the respective pin)

$R_{i(cm)(m)}$	Matching between pin CANH and pin CANL common mode input resistance	$V_{CANH} = V_{CANL} = +5\text{ V}$	1	0	+1	%
$R_{i(diff)}$	Differential input resistance	$R_{i(diff)} = R_{i(cm)(CANH)} + R_{i(cm)(CANL)}$ $2\text{ V} \leq V_{CANH}, V_{CANL} \leq +7\text{ V}$				



MEASUREMENTS SETUPS AND DEFINITIONS

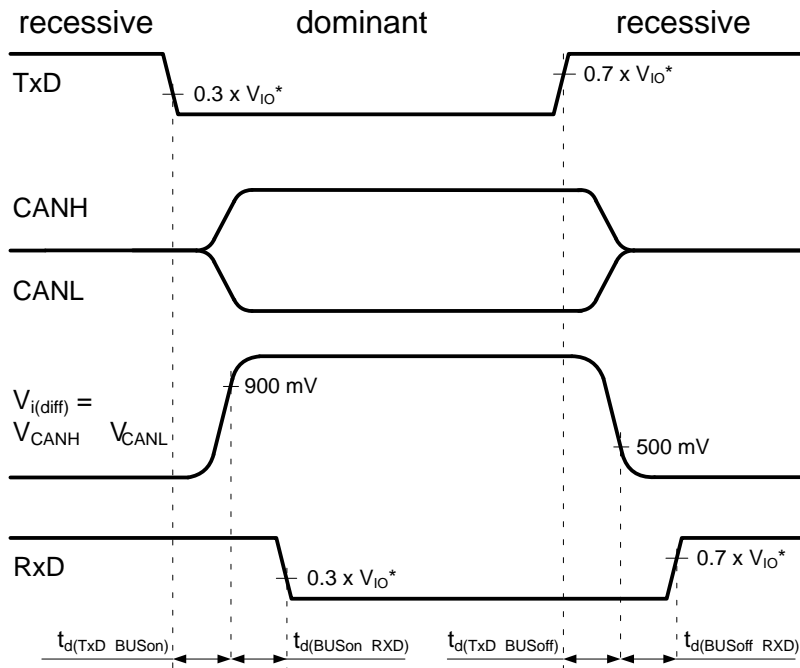
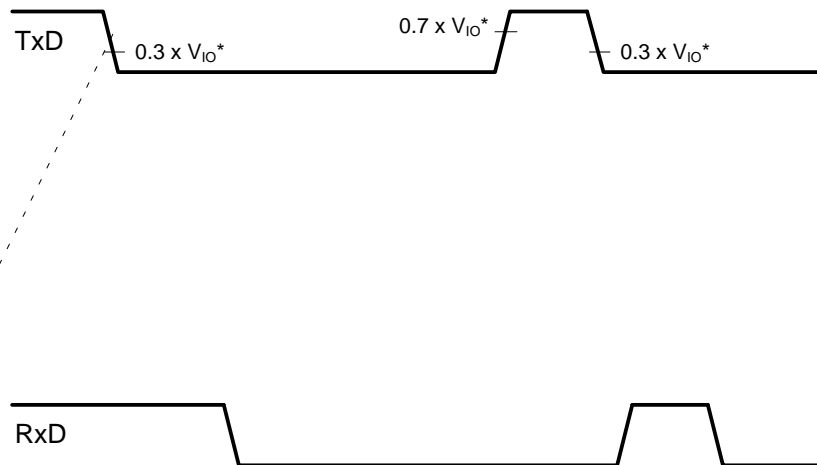


Figure 5. Transceiver Timing Diagram – Propagation Delays



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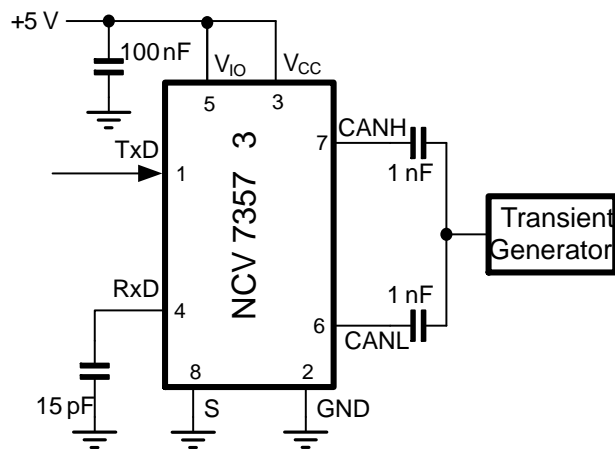


Figure 7. Test Circuit for Automotive Transients

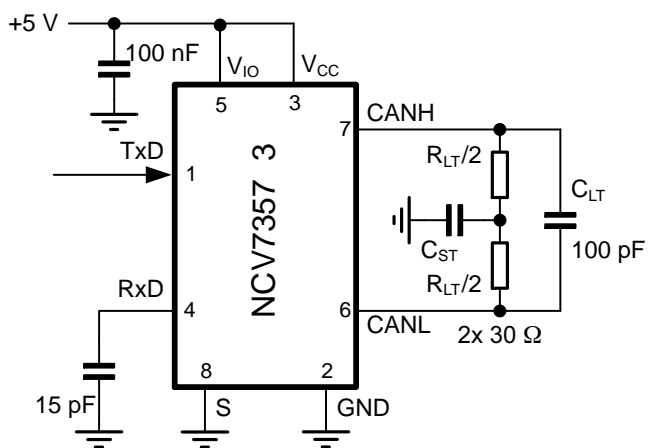


Figure 8. Test Circuit for Timing Characteristics

Table 6. ISO 11898–2:2016 Parameter Cross–Reference Table

ISO 11898–2:2016 Specification	
Parameter	
<b>DOMINANT OUTPUT CHARACTERISTICS</b>	
Single ended voltage on CAN_H	
Single ended voltage on CAN_L	
Differential voltage on normal bus load	
Differential voltage on effective resistance during arbitration	
Differential voltage on extended bus load range (optional)	
<b>DRIVER SYMMETRY</b>	
Driver symmetry	
<b>DRIVER OUTPUT CURRENT</b>	
Absolute current on CAN_H	$I_{CAN\_H}$
Absolute current on CAN_L	$I_{CAN\_L}$
<b>RECEIVER OUTPUT CHARACTERISTICS, BUS BIASING ACTIVE</b>	
Single ended output voltage on CAN_H	$V_{CAN\_H}$
Single ended output voltage on CAN_L	$V_{CAN\_L}$
Differential output voltage	$V_{Diff}$

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Received recessive bit width @ 5 Mbit / s	$\Delta t_{Rec}$	$\Delta t_{rec}$
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**MAXIMUM RATINGS OF  $V_{CAN\_H}$ ,  $V_{CAN\_L}$  AND  $V_{DIFF}$**

Maximum rating $V_{Diff}$	$V_{Diff}$	$V_{CANH}$ $CANL$
General maximum rating $V_{CAN\_H}$ and $V_{CAN\_L}$	$V_{CAN\_H}$ $V_{CAN\_L}$	$V_{CANH}$ $V_{CANL}$
Optional: Extended maximum rating $V_{CAN\_H}$ and $V_{CAN\_L}$	$V_{CAN\_H}$ $V_{CAN\_L}$	NA

**MAXIMUM LEAKAGE CURRENTS ON CAN\_H AND CAN\_L, UNPOWERED**

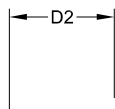
Leakage current on CAN_H, CAN_L	$I_{CAN\_H}$ , $I_{CAN\_L}$	$I_{LEAK(off)}$
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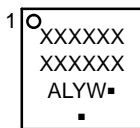
SCALE 2:1

DFNW8 3x3, 0.65P  
CASE 507AB  
ISSUE E

DATE 02 JUL 2021



**GENERIC  
MARKING DIAGRAM\***



XXXXXX = Specific Device Code

A = Assembly Location

L = Wafer Lot

Y = Year

W = Work Week

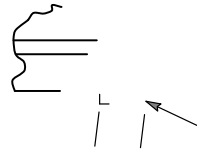
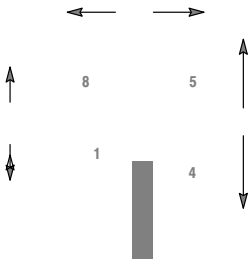
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**SOIC 8 NB**  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011



SEATING  
PLANE





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