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NC 7410

Description

The NCV7410 device is an IEEE 802.3cg−compliant Ethernet Transceiver with an integrated Media Access Controller (MAC−PHY).

The NCV7410 can communicate with multiple nodes connected to a shared medium (UTP) at 10 Mbps. It consists of CSMA/CD MAC and PHY with Physical Layer Collision Avoidance (PLCA). PLCA prevents collisions at the physical layer and, therefore, improves the throughput of CSMA/CD. The NCV7410 uses SPI (with a clock up to 25 MHz) as an interface to host MCU.

Features

- Compliant to IEEE 802.3cg 2019
  - Supports Half−Duplex, Multidrop Mode
- Physical Layer Collision Avoidance (PLCA)
- SPI Interface (OPEN Alliance 10BASE−T1x MAC−PHY Serial Interface)
- Distance Measurement between Nodes
- Single 3.3 V Supply Operation
- Transmitter Optimized for Capacitive Coupling to UTP Cable
- MDI Pins Protected against:
  - ±6 kV ESD (HBM, IEC61000−4−2)
  - Transient Pulses (ISO7637)
- Operating Ambient Temperature −40°C to +125°C (T_{AMB_Class1})
- Junction Temperature Range −40°C to +150°C

Environment

- These are Pb−Free Devices

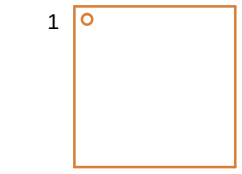
Typical Applications

- Automotive
- Agricultural Machinery
- Machine Control

Quality

- Wettable Flank Package for Enhanced Optical Inspection
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

MARKING DIAGRAM



V7410 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

ORDERw[881.85(4) INF Tj/TT6 1 Tf.5617 0 TD.0023

See detailed ordering and shipping information on page 64 of this data sheet.

CASE 484AB

V7410
AWLYYWW

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APPLICATION INFORMATION

Figure 1 shows an example of an application with the NCV7410.

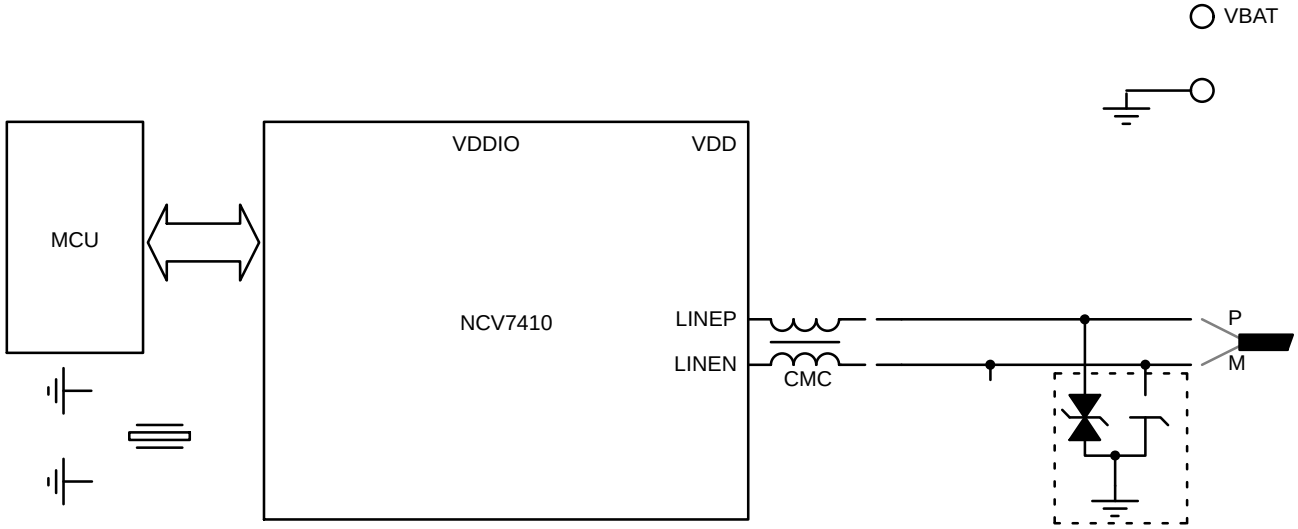


Figure 1. Basic Application Diagram

PIN ASSIGNMENT

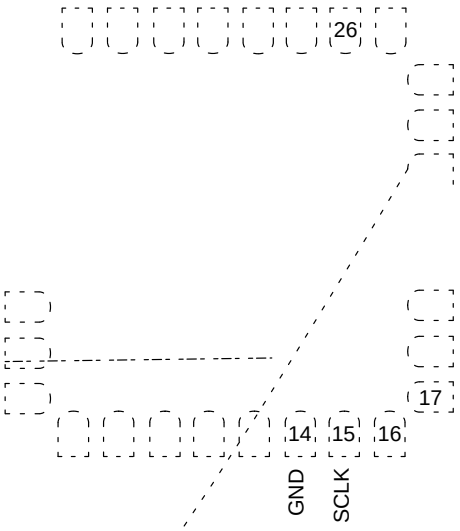


Figure 3. Pin Assignment ï QFN32 (Top View)

PIN DEFINITION

The pinout of the NCV7410 is shown in Figure 3. The pin list is given in Pin Function Description table below.

Table 2. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Pin Function	Description
1	XO	Output	Crystal XO
2	XI	Input	Crystal XI / Reference clock input
4	VDD	Power Supply	3.3 V Power Supply Input
6	LINEP	Analog Input / Output	Positive Medium Dependent Interface (MDI) terminal
7	LINEN		Negative Medium Dependent Interface (MDI) terminal
8	VDRVN	Supply (regulator output)	Output of internal TX LDO. Proper decoupling needed.
11	DIO1	GPIO	General Purpose IO. During BOOT, an internal pull ïdown is connected to both DIOs. See DIO Configuration Register.
12	DIO0		
13	RSTn	Digital Input, Open Drain	Reset pin (Active ïlow), internal 54 k pull ïup, driven low (25) during undervoltage event. To prevent damage, when driving this from an MCU or any active driver, make sure that such drive is configured to be an open drain driver.
15	SCLK	Digital Input	SPI interface Shift Clock
16	IRQn	Digital Output, open drain	Interrupt pin, active low
17, 21	VDDIO	Supply Input	Digital I/O voltage reference (3.3 V or 2.5 V)
18	MOSI	Digital Input	SPI interface Serial Data Input
19	CSn		SPI interface Chip Select (active low)
20	CLK_O	Digital Output	25 MHz clock output
23	MISO	Digital Output	SPI interface Serial Data Output
25, 26, 27	NC	Reserved	Do not connect
28, 29	DVDD	Supply (regulator output)	Output of internal 1.8 V LDO. Proper decoupling is needed.
32	NC	Reserved	Do not connect
3, 5, 9, 10, 14, 22, 24, 30, 31	GND		

Table 3. MAXIMUM RATINGS

Symbol	Rating	Min	Max	Unit
V_{VDD_MAX}	Voltage Supplies (VDD, VDDIO), (Note 1)	−0.3	3.65	V
V_{DVDD_MAX}	Low Voltage Supply Output (DVDD)	−0.3	1.98	V

ELECTRICAL CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (VDD = 2.97 V to 3.63 V; VDDIO = 2.25 V to 3.63 V; C_{VDD}, C_{VDDA}, C_{DRVN} = 2.2 μF; C_{VDDIO} = 100 nF; T_J = −40 to +150°C; for typical values T_J = 25°C; for min/max values. T_J = −40 to 150°C; unless otherwise noted. All voltages are referenced to GND (Exposed Pad). Positive currents flow into the respective pin.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
POWER SUPPLY – PIN VDD						
I_{VDD}	Supply Current	Transmitting	−	45		

ELECTRICAL CHARACTERISTICS (VDD = 2.97 V to 3.63 V; VDDIO = 2.25 V to 3.63 V; C_{VDD}, C_{VDDA}, C_{DRVN} = 2.2 μF; C_{VDDIO} = 100 nF; T_J = −40 to +150°C; for typical values T_J = 25°C; for min/max values. T_J = −40 to 150°C; unless otherwise noted. All voltages are referenced to GND (Exposed Pad). Positive currents flow into the respective pin.) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit

SPI INTERFACE TIMING

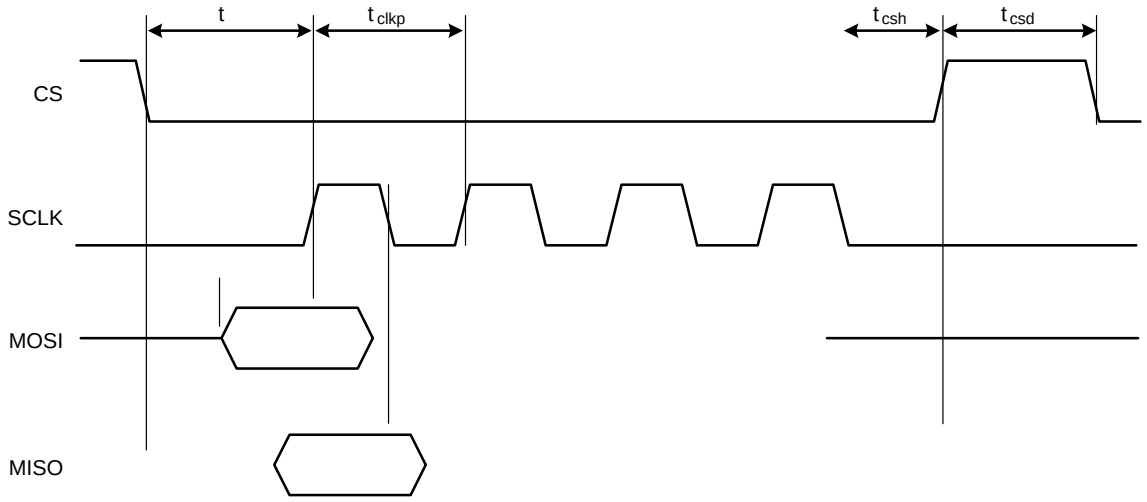


Figure 4. SPI Interface AC Timing Diagram

DETAILED DESCRIPTION

The NCV7410 is a 10BASE−T1S Physical Layer Transceiver as specified in IEEE 802.3cg with an integrated Media Access Controller (MAC). It supports operation over a shared media (multidrop) network with up to 25 m of a single twisted pair (UTP / STP) connection.

The NCV7410 provides a Serial Peripheral Interface (SPI) in slave mode, allowing low pin count connection to standard, off−the−shelf Microcontrollers or SoC. The NCV7410 provides a link speed of 10 Mbit/s in half−duplex operation.

The MAC−PHY's SPI protocol is compliant to the specification issued by the Open Alliance. The NCV7410 can be locally configured to run Physical Layer Collision Avoidance (PLCA), that supports at least 8 nodes on the shared medium, depending on environmental conditions.

PLCA improves data throughput under high network load and provides additional benefits:

- Nodes are granted transmit opportunities using a round−robin arbitration scheme, enabling fair−shared access to the medium.
- By avoiding multiple back−off and retry events in the embedded MAC, maximum latencies are significantly reduced.
- Protects against the "babbling idiot" problem, as a single station can only transmit when granted an opportunity to do so.

The integration of the PLCA reconciliation sublayer (PLCA RS) in the device enables connected hosts to take full advantage of collision−free Ethernet communication on a single twisted pair, shared medium.

The integrated CSMA/CD 10 Mbps MAC provides the following features:

- Multiple MAC address filtering
- Broadcast / Multicast filtering
- Promiscuous Mode, accepting every frame regardless of its type or address
- FCS generation / checking
- Statistics / Diagnostic Counters
- Status reporting
- Factory provided unique MAC address.

The SPI Protocol handler supports:

- 8−byte, 16−byte, 32−byte and 64−byte data chunks
- Both "Store & Forward" and "Cut−Through" operation
- Protected and Unprotected control transaction
- 4 kB TX−Buffer
- 4 kB RX−Buffer
- SPI clock up to 25 MHz

Additional non−standard features are implemented into the NCV7410:

- Enhanced Noise Immunity PMA operation (ENI)
- Collision detection masking
- PLCA Precedence Mode
- PLCA coordinator selection
- Proprietary topology discovery, allowing to measure the distance between nodes on the link segment − works only when all communication partners are **onsemi** 10BASE−T1S devices: NCV7410, NCV7311, NCN26010 or NCN26000.

The integrated Crystal Oscillator circuitry allows the use of an external CMOS oscillator, a quartz crystal, or any other external clock source, as long as its accuracy is in line with the specifications.

REGISTER MEMORY MAP

The NCV7410 provides the registers grouped in memory map selection groups. See the below table for details.

Table 9. REGISTER MAP OVERVIEW

MMS		Address		Name
Hex	Dec	Hex	Dec	
MMS0 REGISTERS				
0x0	0	0x0	0	SPI Identification Register, IDVER
		0x1	1	SPI Identification Register, PHY ID
		0x2	2	SPI Capabilities, SPICAP
		0x3	3	Reset Control and Status, RESET
		0x4	4	SPI Protocol Configuration Register, CONFIG0
		0x8	8	SPI Protocol Status Register, STATUS0
		0xB	11	Buffer Status Register, BUFSTS
		0xC	12	Interrupt Mask Register, IMASK
		0xFF00	65280	PHY Control Register
		0xFF01	65281	PHY Status Register
		0xFF02	65282	PHY Identifier 0 Registers
		0xFF03	65283	PHY Identifier 1 Registers
MMS1 REGISTERS ï REGISTERS RELATED TO THE MAC				
0x1	1	0x0	0	MAC Control0 Register
		0x10	16	Address Filter 0 Low, ADDRFILT0L
		0x11	17	Address Filter 0 High, ADDRFILT0H
		0x12	18	Address Filter 1 Low, ADDRFILT1L
		0x13	19	Address Filter 1 High, ADDRFILT1H
		0x14	20	Address Filter 2 Low, ADDRFILT2L
		0x15	21	Address Filter 2 High, ADDRFILT2H
		0x16	22	Address Filter 3 Low, ADDRFILT3L
		0x17	23	Address Filter 3 High, ADDRFILT3H
		0x20	32	Address Mask 0 Low, ADDRMASK0L
		0x21	33	Address Mask 0 High, ADDRMASK0H
		0x22	34	Address Mask 1 Low, ADDRMASK1L
		0x23	35	Address Mask 1 High, ADDRMASK1H
		0x24	36	Address Mask 2 Low, ADDRMASK2L
		0x25	37	Address Mask 2 High, ADDRMASK0H
		0x26	38	Address Mask 3 Low, ADDRMASK3L
		0x27	39	Address Mask 0 High, ADDRMASK3H
		0x30	48	Statistic, Sent Bytes Counter Low, STOCTETSTXL
		0x31	49	Statistic, Sent Bytes Counter High, STOCTETSTXH
		0x32	50	Statistic, Frames Sent Ok, STFRAMESTXOK
		0x33	51	Statistic, Broadcast Frames Sent Ok, STBCASTTXOK
		0x34	52	Statistic, Multicast Frames Sent Ok, STMCASTTXOK
		0x35	53	Statistic, 64 ïbyte Frames Sent Ok, STFRAMESTX64
		0x36	54	Statistic, 65 ïbyte to 127 ïbyte Frames Sent Ok, STFRAMESTX65
		0x37	55	Statistic, 128 ïbyte to 255 ïbyte Frames Sent Ok, STFRAMESTX128
		0x38	56	Statistic, 256 ïbyte to 511 ïbyte Frames Sent Ok, STFRAMESTX256
		0x39	57	Statistic, 512 ïbyte to 1023 ïbyte Frames Sent Ok, STFRAMESTX512

Table 9. REGISTER MAP OVERVIEW (continued)

MMS		Address		Name
Hex	Dec	Hex	Dec	
MMS1 REGISTERS − REGISTERS RELATED TO THE MAC				
0x1	1	0x3A	58	Statistic, 1024−byte or More Frames Sent Ok, STFRAMESTX1024
		0x3B	59	Statistic, Aborted frames Due to TX−buffer Underflow, STUNDERFLOW
		0x3C	60	Statistic, Frames Transmitted after a Single Collision, STSINGLECOL
		0x3D	61	Statistic, Frames Transmitted after Multiple Collisions, STMULITCOL
		0x3E	62	Statistic, Frames Transmitted after Excessive Collisions, STEXCESSCOL
		0x3F	63	Statistic, Frames Transmitted after Deferral, STDEFEEREDTX
		0x40	64	Statistic, Counter of CRS De−assertion During Frame Transmission, STCRSERR
		0x41	65	Statistic, Received Bytes Counter Low, STOCTETSRXL
		0x42	66	Statistic, Received Bytes Counter High, STOCTETSRXH
		0x43	67	Statistic, Frames Received Ok, STFRAMESRXOK
		0x44	68	Statistic, Broadcast Frames Received Ok, STBCASTRXOK
		0x45	69	Statistic, Multicast Frames Received Ok, STMCASTRXOK
		0x46	70	Statistic, 64−byte Frames Received Ok, STFRAMESRX64
		0x47	71	Statistic, 65−byte to 127−byte Frames Received Ok, STFRAMESTX65
		0x48	72	Statistic, 128−byte to 255−byte Frames Received Ok, STFRAMESTX128
		0x49	73	Statistic, 256−byte to 511−byte Frames Received Ok, STFRAMESTX256
		0x4A	74	Statistic, 512−byte to 1023−byte Frames Received Ok, STFRAMESTX512
		0x4B	75	Statistic, 1024−byte or More Frames Received Ok, STFRAMESTX1024
		0x4C	76	Statistic, Dropped Too Short Frames, STRUNTERR
		0x4D	77	Statistic, Dropped Too Long Frames STRXTOOLONG
		0x4E	78	Statistic, Dropped FCS Error Frames STFCSERRS
		0x4F	79	Statistic, Symbol Errors During Frame Reception, STSYMBOLERRS
		0x50	80	Statistic, Align Errors During Frame Reception, STALIGNERRS
		0x51	81	Statistic, RX Buffer Overflow Errors, STRXOVERFLOW
		0x52	82	Statistic, RX Dropped Frame Count, STRXDROPPED
MMS2 REGISTERS − REGISTERS RELATED TO THE PHY: PCS				
0x2	2	0x5	5	Devices in Package 1 Register
		0x6	6	Devices in Package 2 Register
		0x8F3	2291	10BASE−T1S PCS Contr1 0 8 4 V3

Table 9. REGISTER MAP OVERVIEW (continued)

MMS		Address		Name
Hex	Dec	Hex	Dec	
MMS4 REGISTERS ï REGISTERS RELATED TO THE PHY: PLCA				
0x4	4	0x8000	32768	Chip Revision Register
		0x8001	32769	PHY Configuration 1 Register
		0x8002	32770	PLCA Extensions Register
		0x8003	32771	PMA Tune 0 Register
		0x8004	32772	PMA Tune 1 Register
		0xCA00	51712	PLCA Register Map and Identification Register, PLCIDVER
		0xCA01	51713	PCLA Control 0 Register, PLCACTRL0
		0xCA02	51714	PCLA Control 1 Register, PLCACTRL1
		0xCA03	51715	PCLA Status Register, PLCASTATUS
		0xCA04	51716	PCLA Transmit Opportunity Timer Register, PLCATOTMR
		0xCA05	51717	PCLA Burst Mode Register, PLCABURST
MMS12 REGISTERS ï VENDOR SPECIFIC REGISTERS				
0xC	12	0x10	16	MIIM Interrupt Control Register
		0x11	17	MIIM Interrupt Status Register
		0x12	18	DIO Configuration Register
		0x16	22	Topology Discovery Control Register
		0x17	23	Topology Discovery Status Register
		0x18	24	Topology Discovery Result Register
		0x19	25	Topology Discovery Precision Register
		0x1A	26	Topology Reference Counter Timer Register
		0x1001	4097	PHY Configuration 0 Register
		0x1002	4098	MACID0
		0x1003	4099	MACID1
		0x1004	4100	Chip Info Register
		0x1005	4101	NVM Health Register

MMS0 REGISTERS

SPI Identification Register, IDVER
MMS: 0

SPI Capabilities, SPICAP
MMS: 0
Address: 0x2
Default: 0x5A3

Bit(s)	Name	Description	Default	Access
31:11	−	Value always 0	0x0	RO
10	TXFCSVC	**TX Frame Check Sequence Verification** NCV7410 MAC supports checking the FCS on outgoing frames when not configured to compute and append the FCS to TX frames. When this feature is enabled and the MAC−PHY is operating in “store & forward” mode, frames from the SPI having an incorrect checksum are not forwarded to the line. If the MAC		

SPI Protocol Configuration Register, CONFIG0
MMS: 0
Address: 0x4
Default: 0x6

Bit(s)	Name	Description	Default	Access
31:16	−	Value always 0	0x0	RO
15	SYNC	**Configuration Synchronization** When set to 0, NCV7410 does not accept TX or RX frames, as its configuration may not be complete. Once the host completes the configuration of NCV7410 it		

SPI Protocol Status Register, STATUS0
MMS: 0
Address: 0x8
Default: 0x40

Bit(s)	Name	Description	Default	Access
31:13	−	Value always 0	0x0	RO
12	CDPE	**Control Data Protection Error** When configured to control data read/write protection (set bit PORTE of CONFIG0 Register), this bit indicates that the MAC−PHY has detected an error in the last control transaction.	0	R/W1C
11	TXFCSE	**Transmit Frame Check Sequence Error** When set, this bit indicates that the MAC−PHY has detected that the outgoing frame's FCS added by the host is invalid. To clear this bit, write a "1" to this field.		

Buffer Status Register, BUFSTS
MMS: 0
Address: 0xB
Default: 0x3C00

Bit(s)	Name	Description	Default	Access
31:16	–	Value always 0	0x0	RO
15:8	TXC	**Transmit Chunks Available**		

Interrupt Mask Register, IMASK
MMS: 0
Address: 0xC
Default: 0x1FBF

Bit(s)	Name	Description	Default	Access
31:13	−	Value always 0	0x0	RO
12	CDPEM	**Control Data Protection Error Mask** When set, the Control Data Protection status bit in SPI STATUS0 register does not set the EXST bit in the data footer and prevents IRQn from being asserted.	1	RW
11	TXFCSEM	**TX Frame Check Sequence Error Mask** When set, the Transmit FCS Error (TXFCSE) status bit in STATUS0 register does not set the EXST bit in the data footer and prevents IRQn from being asserted.	1	RW
10	Reserved	Value always 1	1	RO
9	Reserved	Value always 1	1	RO
8	Reserved	Value always 1	1	RO
7	PHYINTM	**PHY Interrupt Mask** When set, the physical layer interrupt (PHYINT) status bit in STATUS0 does not assert IRQn or EXST in the data chunk footer.	1	RW
6	RESETCM	**Reset Complete Mask** Reset Complete Mask. This bit is reserved as a mask for the Reset Complete (RESETC) status bit. This bit is read−only and always zero as the RESETC status bit is a non−maskable interrupt that will cause IRQn to always assert when RESETC is set.	0	RO
5	HDREM	**Header Error Mask** When set, a SPI Header Error (HDRE) does not assert IRQn or EXST in the data chunk footer.	1	RW
4	LOFEM	**Loss of Frame Error Mask** When set, the LOFE status bit in STATUS0 does not assert IRQn or EXST in the data chunk footer.	1	RW
3	RXDOEM	**Receive buffer Overflow Error Mask** When set, the RXDOE status bit in STATUS0 does not assert IRQn or EXST in the data chunk footer.	1	RW
2	TXBUEM	**Transmit Buffer Underflow Error Mask** When set, the TXBUE status bit in STATUS0 does not assert IRQn or EXST in the data chunk footer.	1	RW
1	TXBOEM	**Transmit Buffer Overflow Error Mask** When set, the TXBOE status bit in STATUS0 does not assert IRQn or EXST in the data chunk footer.	1	RW
0	TXPEM	**Transmit Protocol Error Mass** When set, the TXPE status bit in STATUS0 does not assert IRQn or EXST in the data chunk footer.	1	RW

PHY Control Register
MMS: 0
Address: 0xFF00 (65280)
Default: 0x0

Bit(s)	Name	Description	Default	Access
31:16	−	Value always 0	0x0	RO
15	RESET	**Soft Reset** 1 = PHY reset 0 = normal operation When set, a soft reset is initiated. Soft reset does not cause bootstrapping, avoiding changes in operation mode set during bootstrapping at power on or hard rest. All registers revert to their default values and any communication is interrupted. After the soft reset procedure is completed, this bit is automatically reset to 0 (its default).	0x0	RW SC
14	LOOP	**Loop−Back Mode** 1 = loopback mode enabled 0 = loopback mode disabled When set to 1, frames are looped back to the MAC rather than being sent over the line. In this mode, the transceiver is isolated from the line.	0x0	RW
13	SPD0	**Bit 0 of Speed Selection [1:0]** See Bit 6 below	0x0	RO
12	LCTL	**Link Control** 1 = PHY transmit/receive enabled 0 = PHY transmit/receive disabled Implementation is different from how it is specified in Clause 22.2.4.1.4 (Auto negotiation Enable).	0x0	RW
11	−	Value always 0	0x0	RO
10	ISOM	**Isolated Mode Enable** 1 = Isolated mode enabled 0 = Normal operation When set to 1, all pins are set to tristate except for the SPI interface and the IRQn pin. The default state depends on the bootstrap configuration.	0x0	RW
9	LRST	**Link Reset** 1 = Reset Link Status ed.		

PHY Status Register
MMS: 0

PHY Identifier 0 Registers
MMS: 0
Address: 0xFF02 (65282)
Default: −

Bit(s)	Name	Description	Default	Access
31:16	−	Value always 0	0x0	RO
15:0	OUI [3:18]	**Organizational Unique Identifier [2:17]** The bit order is reversed. Bit 15 maps bit 2 of the OUI, and bit 0 maps bit 17 of the OUI. Bits 0 and 1 are 0. NOTE: **onsemi**'s OUIs can be found at: https://standards−oui.ieee.org/	−	RO

PHY Identifier 1 Registers
MMS: 0
Address: 0xFF03 (65283)
Default: −

Bit(s)	Name	Description	Default	Access
31:16	−	Value always 0	0x0	RO
15:10	OUI [19:23]	**Organizational Unique Identifier [18:23]** The bit order is reversed. Bit 15 corresponds to bit 18 of the OUI, and bit 10 corresponds to bit 23 of the OUI. NOTE: **onsemi**'s OUIs can be found at: https://standards−oui.ieee.org/	−	RO
9:4	MODEL	**IC Model Number**	0x1A	RO
3:0	REV	**Chip Revision Number**	0x1	RO

MMS1 REGISTERS

Memory Map Selection 1 contains all registers related to the Media Access Controller (MAC) of the NCV7410 device

MAC Control0 Register

MMS: 1
Address: 0x0 (0)
Default: 0x100 (256)

Bit(s)

(continued)

Bit(s)	Ded)	Access

Address Filter 2 High, ADDRFILT2H
MMS: 1
Address: 0x15 (21)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31	EN	**Filter 2 Enable** 1 = Filter enabled 0 = Filter disabled This bit, when set, enables the corresponding Address filter, to filter incoming frames. ADRF in the MAC Control Register (MMS 1, 0x0000 bit 16) shall be enabled for address filtering to work.	0x0	RW
30:16	−	Value always 0	0x0	RO
15:0	ADDRFILT2 [47:32]	**Address Filter 2 High** Higher order bits of the Filter Address	0x0	RW

Address Filter 3 Low, ADDRFILT3L
MMS: 1
Address: 0x16 (22)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	ADDFILT3 [31:0]	**Address Filter 3 Low** Holds the 32 lower order bits of the Address Filter 0 that is split into ADDRFILT3L and ADDRFILT3H.	0x0	RW

Address Filter 3 High, ADDRFILT3H
MMS: 1
Address: 0x17 (23)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31	EN	**Filter 3 Enable** 1 = Filter enabled 0 = Filter disabled This bit, when set, enables the corresponding Address filter, to filter incoming frames. ADRF in the MAC Control Register (MMS 1, 0x0000 bit 16) shall be enabled for address filtering to work.	0x0	RW
30:16	−	Value always 0	0x0	RO
15:0	ADDRFILT3 [47:32]	**Address Filter 3 High** Higher order bits of the Filter Address	0x0	RW

Address Mask 0 Low, ADDRMASK0L
MMS: 1
Address: 0x20 (32)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	ADDRMASK0 [31:0]	**Address Mask 0 Low** Holds the 32 lower−order bits of the address filter mask that is split into ADDRMASK0L and ADDRMASK0H.	0x0	RW

Address Mask 0 High, ADDRMASK0H
MMS: 1
Address: 0x21 (33)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:16	−	Value always 0	0x0	RO
15:0	ADDRMASK0 [47:0]	**Address Mask 0 High** Higher order bits of the Filter Address Mask	0x0	RW

Address Mask 1 Low, ADDRMASK1L
MMS: 1
Address: 0x22 (34)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	ADDRMASK1 [31:0]	**Address Mask 1 Low** Holds the 32 lower−order bits of the address filter mask that is split into ADDRMASK1L and ADDRMASK1H.	0x0	RW

Address Mask 1 High, ADDRMASK1H
MMS: 1
Address: 0x23 (35)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:16	−	Value always 0	0x0	RO
15:0	ADDRMASK1 [47:0]	**Address Mask 1 High** Higher order bits of the Filter Address Mask	0x0	RW

Address Mask 2 Low, ADDRMASK2L
MMS: 1
Address: 0x24 (36)
Default: 0x0 (0)

Bit(s)	Name	DescriptionMMS: 1

Address Mask 3 Low, ADDRMASK3L
MMS: 1
Address: 0x26 (38)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	ADDRMASK3 [31:0]	**Address Mask 0 Low** Holds the 32 lower−order bits of the address filter mask that is split into ADDRMASK3L and ADDRMASK3H.	0x0	RW

Statistic, Frames Sent Ok, STFRAMESTXOK
MMS: 1
Address: 0x32 (50)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STFRAMESTXOK	Statistic, Frames Successfully Transmitted Holds the number of frames transmitted successfully since the last read of this register. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO ïSCR

Statistic, Broadcast Frames Sent Ok, STBCASTTXOK
MMS: 1
Address: 0x33 (51)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STBCASTTXOK	Statistic, Broadcast Frames Successfully Transmitted Holds the number of broadcast frames (destination address FF:FF:FF:FF:FF:FF) transmitted successfully since the last read of this register. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO ïSCR

Statistic, Multicast Frames Sent Ok, STMCASTTXOK
MMS: 1
Address: 0x34 (52)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STMCASTTXOK	Statistic, Multicast Frames Successfully Transmitted Holds the number of multicast frames (first bit of destination address is set to 1) transmitted successfully since the last read of this register. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO ïSCR

Statistic, 64 ïbyte Frames Sent Ok, STFRAMESTX64
MMS: 1
Address: 0x35 (53)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STFRAMESTX64	Statistic, 64 ïbyte frames sent ok Holds the number of 64 ïbyte frames transmitted successfully since the last read of this register. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO ïSCR

Statistic, 65−byte to 127−byte Frames Sent Ok, STFRAMESTX65
MMS: 1
Address: 0x36 (54)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STFRAMESTX65	**Statistic, 65−byte to 127−byte Frames Sent Ok** Holds the number of frames transmitted successfully since the last read of this register, with a size between 65 bytes and 127 bytes. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, 128−byte to 255−byte Frames Sent Ok, STFRAMESTX128
MMS: 1
Address: 0x37 (55)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STFRAMESTX128	**Statistic, 128−byte to 255−byte Frames Sent Ok** Holds the number of frames transmitted successfully since the last read of this register, with a size between 128 bytes and 255 bytes. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, 256−byte to 511−byte Frames Sent Ok, STFRAMESTX256
MMS: 1
Address: 0x38 (56)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STFRAMESTX256	**Statistic, 256−byte to 511−byte Frames Sent Ok** Holds the number of frames transmitted successfully since the last read of this register, with a size between 256 bytes and 511 bytes. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, 512−byte to 1023−byte Frames Sent Ok, STFRAMESTX512
MMS: 1
Address: 0x39 (57)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STFRAMESTX512	**Statistic, 512−byte to 1023−byte Frames Sent Ok** Holds the number of frames transmitted successfully since the last read of this register, with a size between 512 bytes and 1023 bytes. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, 1024−byte or More Frames Sent Ok, STFRAMESTX1024
MMS: 1
Address: 0x3A (58)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STFRAMESTX1024	**Statistic, 1024−byte or more Frames Sent Ok** Holds the number of frames transmitted successfully since the last read of this register, with a size of 1024 bytes or more. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, Aborted Frames Due to TX−buffer Underflow, STUNDERFLOW
MMS: 1
Address: 0x3B (59)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:10	−	Value always 0	0x0	RO
9:0	STUNDERFLOWs)			

Statistic, Frames Transmitted after Multiple Collisions, STMULITCOL
MMS: 1
Address: 0x3D (61)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:18	−	Value always 0	0x0	RO
17:0	STMULTICOL	**Statistic, Frames Transmitted after Multiple Collisions** Holds the number of frames transmitted after multiple collision events. When PLCA is enabled, the register should not count any events. Multiple collisions happening on a PLCA−enabled network may indicate a misconfiguration of the fundamental parameters (e.g. TO_TIMER), the presence of non−PLCA nodes on the same medium or a defect node on the network. The register does not overflow from its maximum value of 0x0003FFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, Frames Transmitted after Excessive Collisions, STEXCESSCOL
MMS: 1
Address: 0x3E (62)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:10	−	Value always 0	0x0	RO
9:0	STEXCESSCOL	**Statistic, Frames Transmitted after Excessive Collisions** Holds the number of outgoing frames that were aborted because of too many collisions. When PLCA is enabled, the register should not count any events. Excessive collision happening on a PLCA−enabled network may indicate misconfiguration of fundamental parameters (e.g. TO_TIMER), the presence of non−PLCA nodes on the network, or a malfunctioning node. The register does not overflow from its maximum value of 0x000003FF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, Frames Transmitted after Deferral, STDEFEEREDTX
MMS: 1
Address: 0x3F (63)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:18	−	Value always 0	0x0	RO
17:0	STDEFERREDTX	**Statistic, Frames Transmitted after Deferral** Holds the number of frames transmitted after being deferred. Refer to IEEE802.3 clause 5.2.2 for details. In PLCA−enabled networks, deferral is part of the arbitration mechanism; therefore, a non−zero value in this counter does not indicate a degradation of network performance. The register does not overflow from its maximum value of 0x0003FFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, Counter of CRS De−assertion During Frame Transmission, STCRSERR
MMS: 1
Address: 0x40 (64)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:10	−	Value always 0	0x0	RO
9:0	STCRSERR	**Statistic, CRS De−assertion During Frame Transmission** Counts events, where carrier indication is de−asserted or not asserted by the PHY during transmission of a frame. A non−zero value in the register may indicate a too−high level of noise on the line. The register does not overflow from its maximum value of 0x000003FF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, Received Bytes Counter Low, STOCTETSRXL
MMS: 1
Address: 0x41 (65)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STOCTETSRX [31:0]	**Statistic, Received Bytes Counter Low** This register holds the 32 low−order bits of the cumulative sum of all data bytes received since the last read. Together with the STOCTETSRXH, this register represents the number of received bytes. The bytes comprise the whole frame, from the first byte of the destination address up to (and including) the frame checksum. If the counter reaches its maximum value of 0xFFFFFFFFFFFF, it will wrap to zero. The counter is cleared when both STOCTETSRXL and STOCTETSRXH are being read. NOTE: Internal logic samples the high−order bits of the 48−bit counter into the STOCTETSRXH register, every time the STOCTETSRXL register is read. For reading the correct number of bytes transmitted, the STOCTETSRXL register must be read before reading the STOCTETSRXH register.	0x0	RO−SCR

Statistic, Received Bytes Counter High, STOCTETSRXH
MMS: 1
Address: 0x42 (66)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:16	−	Value always 0	0x0	RO
15:0	STOCTETSRX [47:32]	**Statistic, Received Bytes Counter High** This register holds the 16 high−order bits of the cumulative sum of all data bytes received since the last read.	0x0	RO−SCR

Statistic, Frames Received Ok, STFRAMESRXOK
MMS: 1
Address: 0x43 (67)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STFRAMESRXOK	**Statistic, Frames Received Ok** Holds the number of frames received successfully since the last read of this register. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, Broadcast Frames Received Ok, STBCASTRXOK
MMS: 1
Address: 0x44 (68)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STBCASTRXOK	**Statistic, Broadcast Frames Received Ok** Holds the number of broadcast frames (destination address FF:FF:FF:FF:FF:FF) received successfully since the last read of this register. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, 65−byte to 127−byte Frames Received Ok, STFRAMESTX65
MMS: 1
Address: 0x47 (71)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STFRAMESRX65	**Statistic, 65−byte to 127−byte Frames Received Ok** Holds the number of frames received successfully since the last read of this register, with a size between 65 bytes and 127 bytes. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, 128−byte to 255−byte Frames Received Ok, STFRAMESTX128
MMS: 1
Address: 0x48 (72)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STFRAMESRX128	**Statistic, 128−byte to 255−byte Frames Received Ok** Holds the number of frames received successfully since the last read of this register, with a size between 128 bytes and 255 bytes. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, 256−byte to 511−byte Frames Received Ok, STFRAMESTX256
MMS: 1
Address: 0x49 (73)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STFRAMESRX256	**Statistic, 256−byte to 511−byte Frames Received Ok** Holds the number of frames received successfully since the last read of this register, with a size between 256 bytes and 511 bytes. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, 512−byte to 1023−byte Frames Received Ok, STFRAMESTX512
MMS: 1
Address: 0x4A (74)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STFRAMESRX512	**Statistic, 512−byte to 1023−byte Frames Received Ok** Holds the number of frames received successfully since the last read of this register, with a size between 512 bytes and 1023 bytes. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.		

Statistic, 1024−byte or More Frames Received Ok, STFRAMESTX1024
MMS: 1
Address: 0x4B (75)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STFRAMESRX1024	**Statistic, 1024−byte or More Frames Received Ok** Holds the number of frames received successfully since the last read of this register, with a size of 1024bytes or more. The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, Dropped Too Short Frames, STRUNTERR
MMS: 1
Address: 0x4C (76)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:10	−	Value always 0	0x0	RO
9:0	STRUNTERR	**Statistic, Dropped Too Short Frames** Holds the number of received frames that were dropped due to their length being shorter than 64 bytes (runt frames). See Clause 4A.4.2 in the IEEE 802.3 specification. Runts are triggered by fragments resulting from collisions on CSMA/CD networks, but might also indicate poor SNR at the physical layer. The register does not overflow from its maximum value of 0x000003FF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, Dropped Too Long Frames STRXTOOLONG
MMS: 1
Address: 0x4D (77)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:10	−	Value always 0	0x0	RO
9:0	STRXTOOLONG	**Statistic, Dropped Too Long Frames** Holds the number of received frames that were dropped due to their length being longer than 1522 bytes. The register does not overflow from its maximum value of 0x000003FF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, Dropped FCS Error Frames STFCSERRS
MMS: 1
Address: 0x4E (78)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:10	−	Value always 0	0x0	RO
9:0	STFCSERRS	**Statistic, Dropped FCS Error Frames** CRC error counter. Holds the number of received frames that were dropped due to a frame check		

Statistic, Symbol Errors During Frame Reception, STSYMBOLERRS
MMS: 1
Address: 0x4F (79)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:10	−	Value always 0	0x0	RO
9:0	STSYMBOLERRS	**Statistic, Symbol Errors During Frame Reception** Holds the number of received frames that were dropped due to the PHY reporting a symbol decoding error. This may be caused by excessive differential noise on the line The register does not overflow from its maximum value of 0x000003FF. The register resets to 0 after reading.	0x0	RO−SCR

Statistic, Align Errors During Frame Reception, STALIGNERRS
MMS: 1
Address: 0x50 (80)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:10	−	Value always 0	0x0	RO
9:0	STALIGNERRS	**Statistic, Align Errors During Frame Reception** Holds the number of received frames that were dropped because their size was not byte−aligned. This may be caused by excessive differential noise on the line or collisions		

Statistic, RX Dropped Frame Count, STRXDROPPED
MMS: 1
Address: 0x52 (82)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
31:0	STRXDROPPED	**Statistic, RX Dropped Frame Count** Holds the number of received frames that were successfully received but dropped because of address filtering. Dropped frames include frames that did not pass the checks against ADDRFILTx/ADDRMASKx, broadcast frames filtered by the BCSF bit setting, and multicast frames filtered by the MCSF bit setting in the MAC control Register (MMS 1, 0x0000). The register does not overflow from its maximum value of 0xFFFFFFFF. The register resets to 0 after reading.	0x0	RO−SCR

MMS2 REGISTERS

Memory Map Selection 2 contains a direct mapping of Clause 45 MMD 3 PHY−PCS registers implemented in the NCV7410 device.

While register access through the SPI interface is always 32−bit, all MMS2 registers are 16−bit registers. The 2 most significant bytes of these registers always contain 0x0000 and cannot be altered by register writes

Devices in Package 1 Register

MMS: 2
Address: 0x5 (5)
Default: 0xB (11)

Bit(s)	Name	Description	Default	Access
15:4	−	Value always 0	0x0	RO
3	PCS	**Presence of PCS** 1 = PCS is present	0x1	RO
2	−	Value always 0	0x0	RO
1	PMA	**Presence of PMA** 1 = PMA is present	0x1	RO
0	CL22	**Presence of CL22 Registers** 1 = Indicates that the device contains Clause 22 standard registers.	0x1	RO

Devices in Package 2 Register

MMS: 2
Address: 0x6 (6)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
15:0	−	Value always 0	0x0	RO

10BASE−T1S PCS Control Register

MMS: 2
Address: 0x08F3 (2291)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
15	PCSRST	**PCS Reset** 1 = PCS reset 0 = Normal operation Setting this bit to one sets all 10BASE−T1S PCS registers to their default state. This may change the internal state of the PHY's PCS and the state of the physical link. Setting this bit causes the PCS and the PMA PHY layers to reset.	0x0	RW−SC
14	LOOP	**Loop−Back Mode** 1 = Loopback enabled 0 = Loopback disabled When enabled, data sent by the MAC is looped back, traversing PCS TX and PCS RX. This allows testing of the 4B/5B encoder/decoder, the PCS TX/RX state machines, and the scrambler.	0x0	RW
13:0	−	Value always 0	0x0	RO

10BASE−T1S PCS Status Register
MMS: 2
Address: 0x08F4 (2292)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
15:8	−	Value always 0	0x0	RO
7	JAB	**PCS has Detected Local or Remote Jabber** 1 = Fault condition detected 0 = No fault condition detected When reading a one on this bit, the PCS inside the NCV7410 has detected a jabber fault condition. This can either be a local or a remote fault condition. The fault is latched until read.	0x0	RO−LH
6:0	−	Value always 0	0x0	RO

10BASE−T1S PCS Diagnostics Register 1
MMS: 2
Address: 0x08F5 (2293)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
15:0	REMJAB	**Remote Jabber Counter** Counts the number of detected remote jabber events since this register was last read. For details see IEEE802.3 Clause 45, MMD3 address 2293. If the count reaches 0xFFFF no more errors are counted to prevent the counter from overflowing.	0x0	RO−SC

10BASE−T1S PCS Diagnostics Register 2
MMS: 2
Address: 0x08F6 (2294)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
15:0	CTX	**Physical Collisions Counter** Counts the number of physical collision events detected by the PHY, since this register was last read. If the count reaches 0xFFFF no more errors are counted to prevent the counter from overflowing. NOTE: Physical collisions are caused by the superposition of signals transmitted simultaneously by more than one station on the same medium. In contrast to physical collisions, logical collisions in PLCA mode are triggered by the PCLA RS arbitration algorithm.	0x0	RO−SC

MMS3 REGISTERS

Memory Map Selection 3 contains a direct mapping of Clause 45 MMD 3 PHY−PMA registers implemented in the NCV7410 device.

While register access through the SPI interface is always 32−bit, all MMS3 registers are 16−bit registers. The 2 most significant bytes of these registers always contain 0x0000 and cannot be altered by register writes

Devices in Package 1 Register

MMS: 3
Address: 0x5 (5)
Default: 0xB (11)

Bit(s)	Name	Description	Default	Access
15:4	−	Value always 0	0x0	RO
3	PCS	**Presence of PCS** 1 = PCS is present	0x1	RO
2	−	Value always 0	0x0	RO
1	PMA	**Presence of PMA** 1 = PMA is present	0x1	RO
0	CL22	**Presence of CL22 Registers** 1 = Indicates that the device contains Clause 22 standard registers	0x1	RO

Devices in Package 2 Register

MMS: 3
Address: 0x6 (6)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
15:0	−	Value always 0	0x0	RO

BASE−T1 Extended Ability Register

MMS: 3
Address: 0x12 (18)
Default: 0x8 (8)

Bit(s)	Name	Description	Default	Access
15:4	−	Value always 0	0x0	RO
3	10T1S	**10BASE−T1S Capability** 1 = NCV7410 supports 10BASE−T1S	0x1	RO
2:0	−	Value always 0	0x0	RO

10BASE−T1S PMA Control Register
MMS: 3
Address: 0x08F9 (2297)
Default: 0x400 (1024)

Bit(s)	Name	Description	Default	Access
15	PMARST	**PMA Reset** Alias of Clause 22 bit 0.15 and MII Control Register bit 15 Soft Reset Setting this bit to one triggers a soft reset. The bit self−clears when the reset finishes.	0x0	RW−SC
14	TXDIS	**Transmitter Disable** 1 = Disable transmit 0 = Enable transmit When enabled, the PHY'S transmitter is shut down and TX requests from the MAC (SPI) are ignored.	0x0	RW
13:11	−	Value always 0	0x0	RO
10	MULT	**Multidrop Mode** Always 1 NCV7410 is a Multidrop device	0x1	RO
9:1	−	Value always 0	0x0	RO
0	LOOP	**PLA Loopback Mode** Same as Clause 22 bit 0.14 and MIIM Control Register MMS1, Address 0xFF00, bit 14.	0x0	RW

10BASE−T1S PMA Status Register
MMS: 3
Address: 0x08FA (2298)
Default: 0x2600 (9728)

Bit(s)	Name	Description	Default	Access
15:14	−	Value always 0	0x0	RO
13	LOOPA	**Loopback Mode** Always returns 1, indicating the PHY supports loopback	0x1	RO
12	−	Value always 0	0x0	RO
11	LPWRA	**Low−power Mode Interface** Always reads 0, the PHY does not support Low Power Mode	0x0	RO
10	MULTA	**Multidrop Mode** Always reads 1, NCV7410 supports half duplex Multidrop operation	0x1	RO
9	RFLTA	**Receive Faults Detection** Always reads 1, the PHY supports receive fault detection	0x1	RO
8:2	−	Value always 0	0x0	RO
1	RJAB	**Remote Jabber Detected** 0 = Remote jabber was not detected since the last read−out 1 = Remote jabber was detected since the last read−out Copy of Clause 22 Register 1.4 and MIIM Status Register, MMS1, Address 0xFF01, bit 4. Auto clear to zero on read. See MIIM Status register for description.	0x0	RO−LH
0	−	Value always 0	0x0	RO

10BASE−T1S Test Mode Control Register
MMS: 3
Address: 0x08FB (2299)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
15:13	Test Mode	**Selection of a Test Mode** 000 = Normal operation 001 = Test Mode 1 (Transmitter output voltage) 010 = Test Mode 2 (Transmitter output droop) 011 = Test Mode 3 (Transmitter PSD mask) 100 = Test Mode 4 (Transmitter High Impedance) 101 = Reserved 110 = Reserved 111 = Reserved	0x0	RW
12:0	−	Value always 0	0x0	RO

MMS4 REGISTERS

Memory Map Selection 4 contains a direct mapping of Clause 45 MMD 31 PLCA and vendor−specific PHY registers implemented in the NCV7410 device.

While register access through the SPI interface is always 32−bit, all MMS4 registers are 16−bit registers. The 2 most significant bytes of these registers always contain 0x0000 and cannot be altered by register writes

Chip Revision Register

MMS: 4
Address: 0x8000 (32768)
Default: 0x10c6 (4294)

Bit(s)	Name	Description	Default	Access
15:12	MAJ	**Major Revision**		

PLCA Extensions Register
MMS: 4
Address: 0x8002 (32770)
Default: 0x800 (2048)

Bit(s)	Name	Description	Default	Access
15	PREN			

PMA Tune 0 Register
MMS: 4
Address: 0x8003 (32771)
Default: 0x2005 (8197)

This register allows fine−tuning of the NCV7410 line receiver.

WARNING: Changing the setting from their default should only be considered by experienced users at their own risk. Invalid settings may lead to unexpected link down and dropped or corrupted Ethernet frames.

Bit(s)	Name	Description	Default	Access
15:14	−	Value always 0	0x0	RO
13:8	BDT	**PLCA Beacon Detection Threshold** This field selects the threshold level for		

PLCA Register Map and Identification Register, PLCIDVER
MMS: 4
Address: 0xCA00 (51712)
Default: 0x0A10 (2576)

Bit(s)	Name	Description	Default	Access
15:8	MAPID	**The Memory Map Identifier** Indicates compatibility with the OA PLCA memory map definition	0x0A	RO
7:0	MAPVER	**The Memory Map Version** Indicated the version of the OA memory map definition, the memory map in the NCV7410 device adheres to	0x10	RO

PCLA Control 0 Register, PLCACTRL0
MMS: 4
Address: 0xCA01 (51713)
Default: 0x0 (0)

Bit(s)	NameName

PCLA Status Register, PLCASTATUS
MMS: 4
Address: 0xCA03 (51715)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
15	PST	**PLCA Status**		

MMS12 REGISTERS

Memory Map Selection 12 contains a direct mapping of Clause 45 MMD 30 vendor−specific registers implemented in the NCV7410 device.

While register access through the SPI interface is always 32−bit, all MMS12 registers are 16−bit registers. The 2 most significant bytes of these registers always contain 0x0000 and cannot be altered by register writes

MIIM Interrupt Control Register

MMS: 12
Address: 0x0010 (16)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
15:6	−	Value always 0	0x0	RO
5	MIPCE	**Physical Collision MIIM Interrupt Enable** 1 = PHYINT on Physical Collision enabled 0 = PHYINT on Physical Collision disabled If enabled, a PHYINT is issued every time a physical collision is detected.	0x0	RW
4	MIPRE	**PLCA Recovery MIIM Interrupt Enable** 1 = PHYINT on PLCA Recovery enabled 0 = PHYINT on PLCA Recovery disabled When enabled, a PHYINT is issued on every PLCA Recovery event. PCLA recovery is flagged when a false carrier event (i.e. impulse noise) occurs on the line. When a CRS event is not followed by the reception of a packet within in certain amount of time the PHY goes to either of two states, depending on its PLCA settings: When configured as PLCA coordinator, the PHY waits for the line to be quiet for a certain amount of time and then sends a new beacon. When configured as a follower, the PHY will wait for a Beacon before getting a new transmit opportunity.	0x0	RW
3	MIRJE	**Remote Jabber MIIM Interrupt Enable** 1 = PHYINT on Remote Jabber enabled 0 = PHYINT on Remote Jabber disabled When enabled, a PHYINT is issued every time the PHY detects a remote jabber condition. A remote jabber condition exists if a station transmits for longer than a maximum length Ethernet frame transmit duration (1518 bytes, not counting Preamble and inter−packet gap).	0x0	RW
2	MILJE	**Local Jabber MIIM Interrupt Enable** 1 = PHYINT on Local Jabber enabled 0 = PHYINT on Local Jabber disabled When enabled, a PHYINT is asserted when the PHY detects a local jabber condition.	0x0	RW
1	MIPSE	**PLCA Status MIIM Interrupt Enable** 1 = PHYINT on change of PLCA Status enabled 0 = PHYINT on change of PLCA Status disabled When enabled, the device issues a PHYINT every time the PLCA Status changes. To determine the actual PLCA status the host interrupt service routine would have the read the PCLA Status Register, PLCASTATUS at MMS 4, Address 51715 (0xCA03).	0x0	RW
0	MILSE	**Link Status MIIM Interrupt Enable** 1 = PHYINT on change of Link Status enabled 0 = PHYINT on change of Link Status disabled When enabled, a PHYINT is issued every time the Link status changes. The actual link status can be read from the Link Status bit (0.2) in the PHY Status Register MMS 0, Address 0xFF01,	0x0	RW

DIO Configuration Register

MMS: 12

Address: 0x0012 (18)

Default: 0x6060 (24672)

The DIO configuration register sets the function of the General Purpose I/O pins DIO1 and DIO0.

Bit(s)	Name	Description	Default	Access
15	SLR1	**DIO1 – Slew Rate** 1 = slow 0 = fast	0x0	RW
14	PEN1	**DIO1 – Pull−up/Pull−down Enable** 1= enabled 0 = disabled	0x1	RW
13	PUD1	**DIO1 – Pull−up/Pull−down Selector** 1 = Pull Down 0 = Pull Up Sets the type of the internal pull, when bit 14 is enabled	0x1	RW
12:9	FN1	**DIO1 – Function Selector** Select the function of the DIO1 pin. See Table 10 below.	0x0	RW
8	VAL1	**DIO1 – Output Value** Sets the output value of DIO1 when FN1[3:0] configure DIO1 for GPIO function It sets the polarity (1 = active high, 0 = active low) for all other modes	0x0	RW
7	SLR0	**DIO0 – Slew Rate** 1 = slow 0 = fast	0x0	RW
6	PEN0	**DIO0 – Pull−up/Pull−down Enable** 1= enabled 0 = disabled	0x1	RW
5	PUD0	**DIO0 – Pull−up/Pull−down Selector** 1 = Pull Down 0 = Pull Up Sets the type of the internal pull, when 6 is enabled	0x1	RW
4:.1	FN0	**DIO0 – Function Selector** Select the function of the DIO1 pin. See Table 10 below.	0x0	RW
0	VAL0	**DIO0 – Output Value** Sets the output value of DIO0 when FN0[3:0] configure DIO0 for GPIO function It sets the polarity (1 = active high, 0 = active low) for all other modes	0x0	RW

Table 10. DIOX FUNCTION SELECTOR DESCRIPTION

FNx[3:0]	Function	Description
0x0	Disable	DIOx is put in tristate (default)
0x1	GPIO	DIOx state corresponds to VALx
0x2	SFD−TX	Generates a pulse at SFD transmission. VALx sets the pulse polarity
0x3	SFD−RX	Generates a pulse when SFD is detected during the read. VALx sets the pulse polarity
0x4	LED − Link Control	Pin drives an LED when link is enabled and link status is up
0x5	LED − PLCA Status	Pin drives an LED when PLCA status is up
0x6		

0x6

Topology Discovery Control Register
MMS: 12
Address: 0x0016 (22)
Default: 0x0 (0)

Bit(s)	Name	Description	Default	Access
15	TD_ED	**Topology Discovery Enable**		

Topology Discovery Status Register
MMS: 12
Address: 0x0017 (23)
Default: 0x8000 (32768)

Bit(s)	Name	Description	Default	Access
15	DONE	**TopDisc Done** When this bit contains a one, the function requested to be performed by the combination of CLAM and MAN (calibration, measurement, or automatic sequence) has finished and the results can be read from the Topology Discovery Result register. Note that there is no valid data stored for the user after a manual calibration. When automatic mode or manual measurement is performed, the user should evaluate the content of the result register.	0x1	RO
14:3	−	Value always 0	0x0	RO
2	HNDE	**TopDisc Handshake Error** When done is set to one and the last topology discovery command was run in automatic mode, a one in this bit will indicate that a handshake error has occurred and the measurement is invalid.	0x0	RO
1	MEAE	**TopDisc Measure Error** 0 = no measurement error during the last executed measurement procedure 1 = error occurred during the last measurement procedure When DONE = 1, this bit indicates that a performed measurement (both, manual and automatic mode) ended with an error. This is an indication that the measurement result stored in the result register is invalid and should be discarded. Instead, the measurement needs to be re−run. This can also be an indication of a connection issue between the two Topology discovery partners (broken cable, short, wrong termination).	0x0	RO
0	CALE	**TopDisc Calibration Error** When DONE = 1, this bit indicates that there was an error during the calibration and the device could not find a calibration solution. This can point to a defective device or traffic on the cable, caused by a network station unaware of a Topology discovery procedure on the cable. The user shall arrange that no other station, than the two stations involved in the Topology discovery, occupies the medium. Calibration errors will be flagged regardless of the operating mode (manual or automatic Topology discovery).	0x0	RO

Topology Discovery Result Register
MMS: 12
Address: 0x0018 (24)
Default: 0x0 (0)

Bit(s)	Name	Description

Topology Discovery Precision Register
MMS: 12
Address: 0x0019 (25)
Default: 0x0FA0 (4000)

Bit(s)	Name	Description	Default	Access
15:0	RTMP	**Topology Discovery Precision Time** j1-.973eates tse7eT/ference coun654ET101.594-]9		

PHY Configuration 0 Register
MMS: 12
Address: 0x1001 (4097)
Default: 0x2ca1 (11425)

The PHY Configuration 0 register allows experienced users to customize the parameters of the Analog line driver among other custom parameters. The default values have been carefully selected and would not need modification under normal conditions.

Bit(s)	Name	Description	Default	Access
15:14	TX_GAIN	**Transmitter Output Amplitude** 0 = 1 Vpp 1 = 1.1 Vpp 2 = 0.9 Vpp 3 = 0.8 Vpp	0x0	RW
13:10	RX_CD	**Receiver Collision Detection Threshold** RX_CD threshold [mVpp] = 150 + (RX_CD x 50) (default = 700 mVpp) NOTE: Setting a small threshold level improves noise immunity but may increase the chance of mis−detecting a collision.	0xB	RW
9:6	RX_ED	**Received Energy Detection Threshold** RX_ED threshold [mVpp] = 150 + (RX_ED x 50) (default = 250 mVpp) NOTE: Threshold shall be set high enough to reject the noise and low enough to detect the worst−case signal amplitude on the line.	0x2	RW
5	DSLEW	**Digital Output Driver Slew Rate** Sets slew rate of all digital output pins 0 = Slow 1 = Fast	0x1	RW
4:3	CMC	**Common Mode Choke Resistance Compensation** This field should be set according to the resistance of the used CMC 00 = 0 – 0.5 Ω 01 = 0.5 – 2.25 Ω 10 = 2.25 – 3.75 Ω 11 = 3.75 – 5 Ω	0x0	RW
2	TXSLEW	**Transmitter Slew Rate** 0 = Slow 1 = Fast	0x0	RW
1	−	Value always 0	0	RO
0	CLKO_EN	**25 MHz Clock Output Enable** 0 = 25 MHz clock is not enabled to be output on CLK_O pin 1 = 25 MHz clock is enabled to be output on CLK_O pin	0x1	RW

MACID0
MMS: 12
Address: 0x1002 (4098)
Default: −

Bit(s)	Name	Description	Default	Access
15:0	MACID [15:0]	Lower 16 bits of the unique MAC address. Together with the upper 8 bits in the MACID1 register, and the OUI from IDVER (MMS0, address 0x0000, bits 31:10), it forms a unique MAC address for the NCV7410 device. Note that no Address Filter is pre−initialized with that MAC address. The user should read MACID0, MACID1, and OUI (from IDVER) to initialize the address filters. The host may also need to use the MAC address as the source address in Ethernet frames sent to the NCV7410.	−	RO

MACID1
MMS: 12
Address: 0x1003 (4099)
Default: −

Bit(s)	Name	Description	Default	Access
15:8	−	Value always 0	0x0	RO
7:0	MACID[23:16]	Upper 8 bits of the MAC address see the description in MACID0 for details.	−	RO

Chip Info Register
MMS: 12
Address: 0x1004 (4100)
Default: −

Bit(s)	Name	Description	Default	Access
15	−	Value always 0	0x0	RO
14:8	Wafer_Y	Y position on the Wafer where the part was picked from	N/A	RO
7	−	Value always 0	0x0	RO
6:0	Wafer_X	X position on the Wafer where the part was picked from	N/A	RO

NVM Health Register

MMS: 12

Address: 0x1005 (4101)

Default: 0x0

This register reports if there are errors in the trim and configuration data set by **onsemi** during manufacturing of the NCV7410.

There are three different zones for the trim & configuration data stored inside the device's nonvolatile configuration memory:

Zone	Description
Green	Manufacturing related data Errors in this zone do not cause any failure or misbehavior in the application.
Yellow	Functional Data: MAC and OUI Corrupted data in this area does not cause the part to malfunction, but a host relying on the information stored here might not initialize its drivers correctly. However, countermeasures taken in the host's software could be used to fall back to a state where operation is still possible.
Red	Trim data Data corruption in this area will render the part unusable. With trimming not being correct, it cannot be guaranteed that the part will operate within the limits required by IEEE802.3cg.

Note that the configuration & trim memory cannot be written by the user, so corrupted data cannot be recovered.

The trim & configuration memory is protected by an ECC scheme that allows the correction of single−bit errors and the detection of double−bit errors. With this, a single−bit error (SBERR) can be considered a warning, while a reported double−bit error needs to be interpreted as an error impairing the function of the part partially or entirely, depending on the zone in which it appears.

Bit(s)	Name	Description	Default	Access
15	Red Zone NVM Warning	When this bit reads as one, the ECC controller for the trim and configuration memory has detected a single−bit error in the red zone. As single−bit errors		

APPLICATIONS INFORMATION

Clock Source

The NCV7410 requires a precise and robust 25 MHz clock source for correct operation.

The clock can either be fed from an external 25 MHz clock source or be generated using a quartz crystal connected to the XTAL Oscillator circuit of the NCV7410.

Crystal Oscillator

The oscillator circuit is designed to drive a 25MHz parallel resonance AT cut quartz crystal. The external crystal shall be connected between the XI pin and the XO pin. XI is the input pin and XO is the output pin of the internal crystal oscillator circuit.

A typical crystal connection circuit is shown in Figure 5.

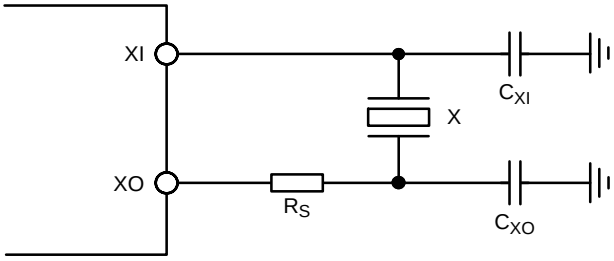


Figure 5. Crystal Connection Diagram

External Clock Source

In situations where a 25 MHz (±100 ppm) clock signal is already available in the system that utilizes the NCV7410 can be clocked using such a signal, removing the need of additional crystal and load capacitors. In this case, the external clock signal is connected to the XI pin of the NCV7410, while the XO pin shall be left floating.

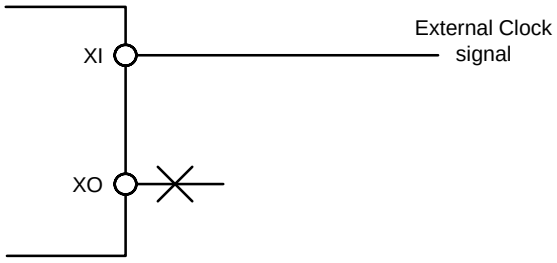


Figure 6. Connecting an External Clock Source

Clock Output

The NCV7410 also offers a dedicated output pin that can provide a stable 25 MHz clock to other components (like MCUs) on the same PCB. The CLK_O pin offers that function at 3.3 V or 2.5 V LVCMOS levels depending on the VDDIO.

DEVICE CONFIGURATION EXAMPLES

To configure the NCV7410, configuration registers (see memory map) can be set using the SPI command following

These filters can also be used to limit the multicast frames to dedicated multicast IDs or a larger group of IDs or unicast addresses.

Example A:

The NCV7410 should be set to forward all Broadcast frames and frames with the destination address 60:C0:BF:01:01:01

Solution:

- Set ADDRFLT0L to 0xBF010101
- Set ADDRFLT0H to 0x800060C0
  Note that bit 31 of ADDRFLTxH activates that filter
- Set ADDRMSK0L to 0xFFFFFFFF
- Set ADDRMSK0H to 0x0000FFFF
- Set bit ADRF and clear bit BCSF in the MAC Controll0 register to one.

Example B:

In addition to Example A, the MAC−PHY should also listen forward all multicast frames of the group 31:6E:17:XX:XX:XX

Solution:

ADDRFLT1L = 0x17000000
ADDRFLT1H = 0x8000316E
ADDRMASK1L = 0xFF000000
ADDRMASK1H = 0x0000FFFF

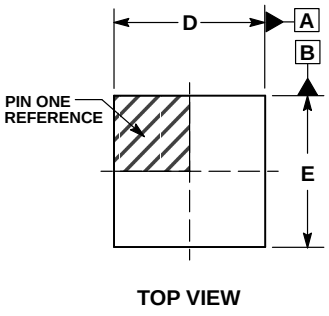
ORDERING INFORMATION

Device Order Number	Marking	Package Type	Shipping†
NCV7410MWR2G	V7410	QFNW32 (Pb−Free)	4000 / Tape & Reel

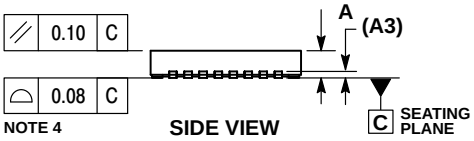
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

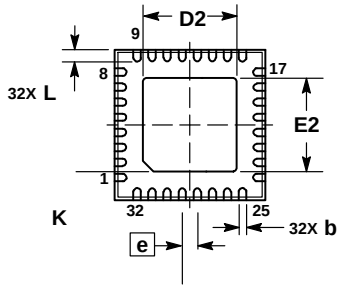
QFNW32 5x5, 0.5P
CASE 484AB
ISSUE D



TOP VIEW



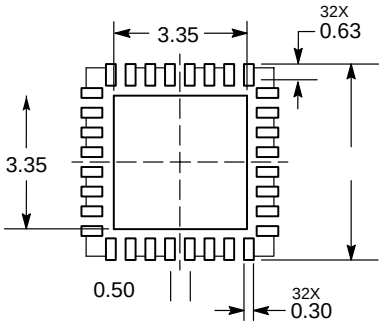
SIDE VIEW



BOTTOM VIEW

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.10 AND 0.20MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.