System Basis Chip with CAN FD, LDO Regulator and Wake-up Comparator

NCV7451

The system basis chip (SBC) NCV7451 integrates +5 V / 250 mA LDO regulator with a high speed CAN FD transceiver and local wake up comparator, directly controlled by dedicated pins.

Features
- 5 V ±2% / 250 mA LDO
  - Current Limitation with Fold back
  - Output Voltage Monitoring
- One High Speed CAN FD Transceiver
  - Compliant to ISO11898 2:2016
  - CAN FD Timing Specified up to 5 Mbps
  - Current Limitation, Reverse Current Protected
  - TxDC Timeout
- Local Wake up Comparator
  - Integrated Pull up / Pull down Current Source
- Very Low Current Quiescent Consumption
- Window Watchdog
- Direct Control
- Thermal Shutdown Protection
- AEC Q100 Qualified and PPAP Capable
- Wettable Flank Package for Enhanced Optical Inspection
- This is a Pb Free Device

Typical Applications
- Automotive
- Industrial Networks

DFNW14 4.5x3, 0.65P
CASE 507AC

MARKING DIAGRAM

NCV7451	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS

ORDERING INFORMATION

Device	Package	Shipping[†]
NCV7451MW0R2G	DFNW14 (Pb−Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
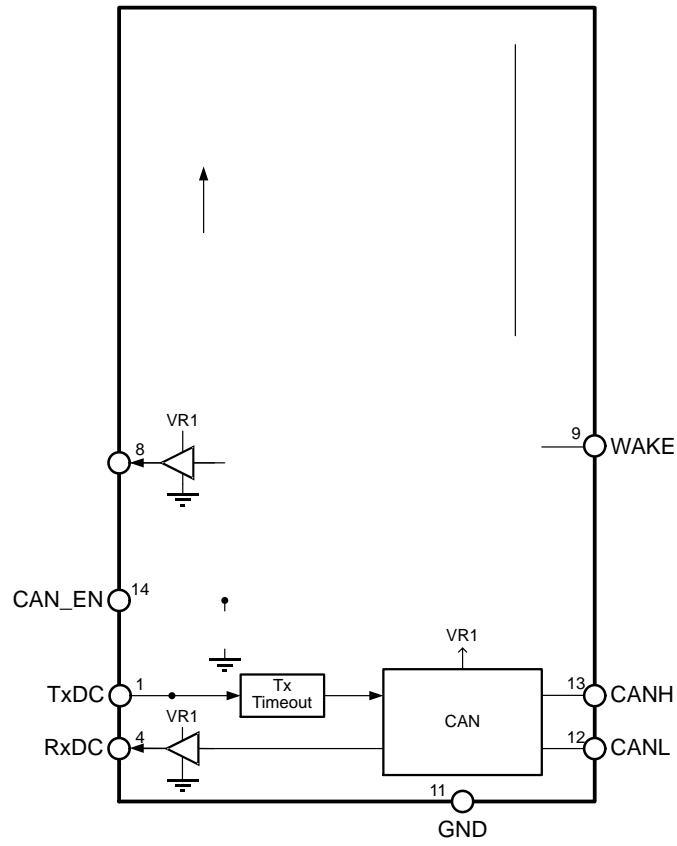
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Figure 2. Block Diagram

MAXIMUM RATINGS

Symbol	Rating		Min	Max	Unit
VS	DC Power Supply Voltage (Note 1)		− 0.3	+40	V
VR1	LDO Supply pin output voltage		− 0.3	6 or VS+0.3 (whichever is lower)	V
digIO	DC voltage on digital pins (CAN_EN, WD_EN, WDI, RSTN, RxDC, TxDC, WAKE_OUT)		− 0.3	VR1+0.3	V
WAKE	DC WAKE pin Input Voltage		− 40	+40	V
CANH, CANL	DC voltage on pin CANH and CANL		− 40	+40	V
Vdiff	Differential DC voltage between any two pins (incl. CANH and CANL)		− 40	+40	V
ESD$_{HBM}$	ESD capability, Device HBM, according to AEC−Q100−002 (EIA/JESD22−A114); (Note 2)	Pins VS, CANH, CANL, WAKE	− 8	+8	kV
		Other pins	− 4	+4	
ESD$_{MM}$	ESD capability; MM, according to AEC−Q100−003 (EIA/JESD22−A115); all pins		−200	+200	V
ESD$_{CDM}$	ESD capability; CDM, according to AEC−Q100−011 (EIA/JESD22−C101); all pins		− 750	+750	V
ESD$_{IEC}$	ESD capability; System HBM, according to IEC61000−4−2; pins VS, CANH, CANL, WAKE; (Note 3)		−6	+6	kV
SCHAF	Voltage transients, Test pulses According to ISO7637 − 2, Class D; pins VS, CANH, CANL, WAKE	Test pulse 1	− 100	–	V
		Test pulse 2a	–	+75	V
		Test pulse 3a	− 150	–	V
		Test pulse 3b	–	+100	V
Tj	Junction Temperature Range		− 40	+150	°C
Tstg	Storage Temperature Range		− 55	+150	°C

ED OPERATING RANGES

Rating	Min	Max	Unit
Functional supply voltage	5.0	28	V
Supply voltage for valid parameter specification	6.0	18	V
VR1 regulator output voltage	4.9	5.1	V
VR1 regulator output current (including CAN transceiver consumption)	0	250	mA
Digital inputs/outputs voltage	0	VR1	V
WAKE input voltage	0	VS	V
CAN bus pins voltage	−40	40	V
Junction Temperature	−40	150	°C
Ambient Temperature	−40	125	°C

n above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond Operating Ranges limits may affect device reliability.

CHARACTERISTICS

$-40°C \leq Tj \leq 150°C$; $4.75 V \leq VR1 \leq 5.25 V$; $R_{LT} = 60$, $C_{LT} = 100$ pF, C_{ST} not used, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Unit
	VS rising	3.4	–	4.1	V
VS POR threshold	VS falling	2.0	–	3.5	V
VS consumption, low−power	VS = 14 V, VR1 on (not loaded), WAKE floating, CAN bus recessive, CAN_EN = Low, WD_EN = Low, Tj $\leq$ 85°C	–	28	35	A
VS consumption, active	VS = 14 V, VR1 on (loaded by 100 mA, not included in Is_act), WAKE floating, CAN bus recessive, CAN_EN = High, WD_EN = High, TxDC = High	–	3.7	5.0	mA

EGULATOR

Parameter	Conditions	Min	Typ	Max	Unit
Regulator output voltage	0 mA $\leq$ I(VR1) $\leq$ 250 mA (including internal CAN consumption), 6 V $\leq$ VS $\leq$ 28 V	4.9	5.0	5.1	V
Regulator current limitation	Maximum VR1 overload current, VR1 > RES_VR1	250	–	650	mA
Regulator short current	Maximum VR1 short current, VR1 < RES_VR1	125	1/2 x Ilim_VR1	325	mA
Dropout Voltage	I(VR1) = 100 mA, VS = 5 V	–	0.2	0.4	V
	I(VR1) = 100 mA, VS = 4.5 V	–	0.2	0.5	
	I(VR1) = 50 mA, VS = 4.5 V	–	0.1	0.4	
Load Regulation	1 mA $\leq$ I(VR1) $\leq$ 100 mA	−50	–	50	mV
Line Regulation	I(VR1) $\leq$ 100 mA	−40			mV

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ELECTRICAL CHARACTERISTICS (continued)

6 V ≤ VS ≤ 18 V; −40°C ≤ Tj ≤ 150°C; 4.75 V ≤ VR1 ≤ 5.25 V; R_{LT} = 60 , C_{LT} = 100 pF, C_{ST} not used, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VR1 VOLTAGE REGULATOR						
Is_add_VR1						

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ELECTRICAL CHARACTERISTICS (continued)

6 V ≤ VS ≤ 18 V; −40°C ≤ Tj ≤ 150°C; 4.75 V ≤ VR1 ≤ 5.25 V; R_{LT} = 60, C_{LT} = 100 pF, C_{ST} not used, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit

CAN f522.312 698.8k(.68036 ref134.476346 0 TDNES001Pins 763H and 763L)TJ(5.25 V)35..0-TD.0sLT

ELECTRICAL CHARACTERISTICS (continued)

6 V $\leq$ VS $\leq$ 18 V; $-40°$C $\leq$ Tj $\leq$ 150°C; 4.75 V $\leq$ VR1 $\leq$ 5.25 V; R_{LT} = 60 , C_{LT} = 100 pF, C_{ST} not used, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit

undervoltage / overvoltage, the CAN transceiver is in its wake up detection state. Logical level on TxDC is ignored and pin RxDC is kept high until a CAN bus wake up is detected. The CAN bus wake up corresponds to a pattern consisting of dominant – recessive – dominant symbols of at least t_{wake_filt} each. The RxDC starts following the CAN bus afterwards. The pattern must be received within t_{wake_to} to be recognized as a valid wake up event, otherwise internal wake up logic is reset.
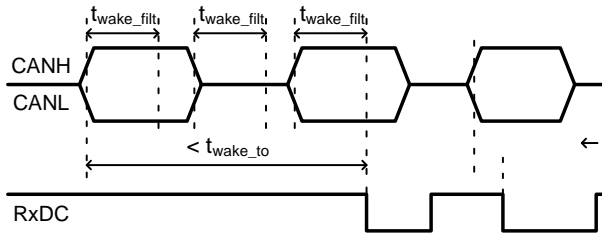
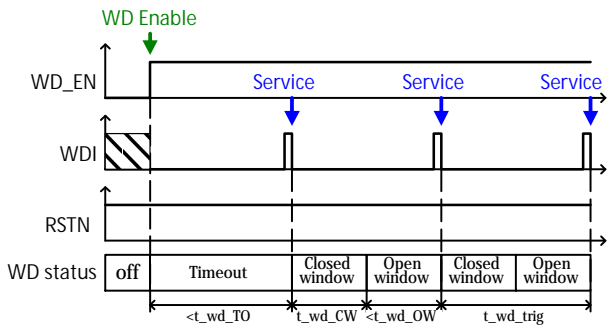

Figure 9. CAN Wake up Pattern

Figure 12. Correct Watchdog Services

In case the watchdog is not triggered before the timeout or open window elapses (Figure 13, Figure 14), or trigger is sent within the closed window (Figure 15), RSTN signal is generated and then watchdog restarted in the timeout mode again.
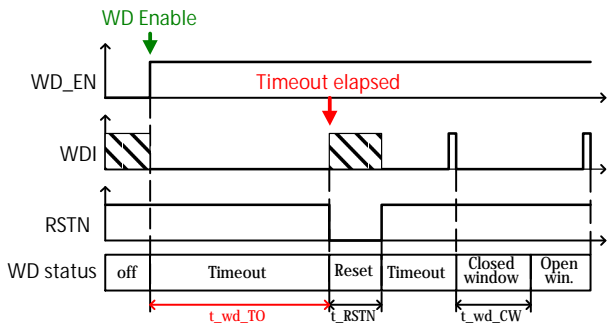
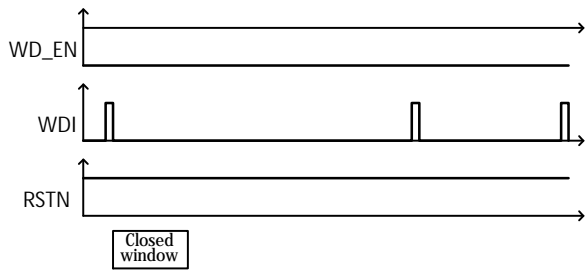

Figure 13. Missed Watchdog in Timeout Mode

Figure 14. Missed Watchdog in Window Mode

Operating Modes

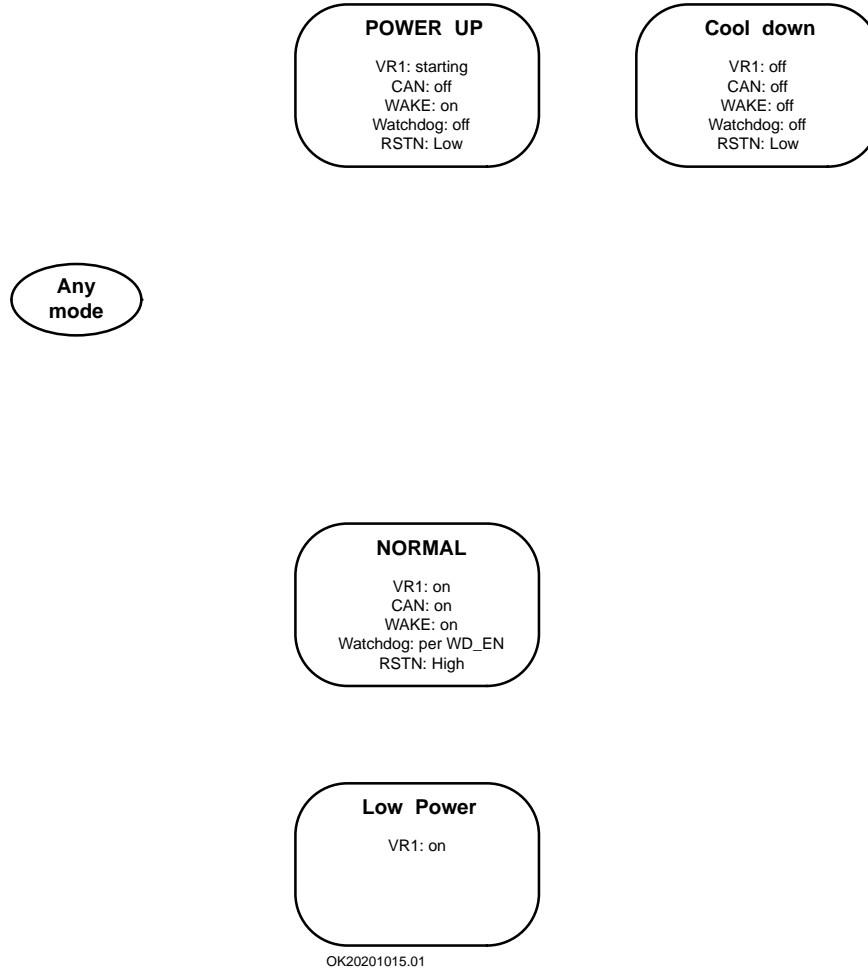The device operating modes are directly controlled by CAN_EN input pin and failure events (see Figure 17).

POWER UP

VR1: starting
CAN: off
WAKE: on
Watchdog: off
RSTN: Low

Cool down

VR1: off
CAN: off
WAKE: off
Watchdog: off
RSTN: Low

Any mode

NORMAL

VR1: on
CAN: on
WAKE: on
Watchdog: per WD_EN
RSTN: High

Low Power

VR1: on

OK20201015.01

Figure 17. Operating Modes Diagram

ISO11898 2:2016 PARAMETER CROSS REFERENCE TABLE

ISO11898 2:2016 PARAMETER CROSS REFERENCE TABLE (continued)

ISO 11898 2:2016 Specification		NCV7451 Datasheet
Parameter	**Notation**	**Symbol**
DATA SIGNAL TIMING REQUIREMENTS for use with bit rates above 2 Mbit/s and up to 5 Mbit/s		
Transmitted recessive bit width @ 5 Mbit/s	$t_{Bit(Bus)}$	$t_{Bit(Vi(diff))}$
Transmitted recessive bit width @ 5 Mbit/s	$t_{Bit(RXD)}$	$t_{Bit(RxDC)}$
Received recessive bit width @ 5 Mbit/s	t_{Rec}	t_{Rec}
MAXIMUM RATINGS OF V_{CAN_H}, V_{CAN_L} AND V_{DIFF}		
Maximum rating V_{Diff}	V_{Diff}	Vdiff
General maximum rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H} V_{CAN_L}	CANH CANL
Optional: Extended maximum rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H} V_{CAN_L}	NA
MAXIMUM LEAKAGE CURRENTS ON CAN_H AND CAN_L, UNPOWERED		
Leakage current on CAN_H, CAN_L	I_{CAN_H}, I_{CAN_L}	I_{LI}
BUS BIASING CONTROL TIMINGS		
CAN activity filter time, long	t_{Filter}	NA
CAN activity filter time, short	t_{Filter}	t_{wake_filt}
Optional: Wake−up timeout, short	t_{Wake}	NA
Optional: Wake−up timeout, long	t_{Wake}	t_{wake_to}
Timeout for bus inactivity (Required for selective wake−up implementation only)	$t_{Silence}$	NA
Bus Bias reaction time (Required for selective wake−up implementation only)	t_{Bias}	NA

PACKAGE DIMENSIONS

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