



Figure 1. Application Schematic Diagram

Table 1	RECOMMENDED	EXTERNAL	COMPONENTS
Table I.	RECOMMENDED	EATERINAL	COMPONENTS

Name	Description	Typical Value	Units	Rating	Tolerance	Comment
R1	Resonator Damping	Optimal value	kΩ		5 %	Value depends on used transducer & transformer
R2	Battery Filter Resistor	100	Ω	Note	5 %	Power rating according to required EMC robustness
R3	I/O Line Protection	470	Ω	Note	5 %	It may be omitted but system ESD robust- ness is reduced Power rating according to required EMC robustness
R4	I/O Line Pull Up	10	kΩ	100 mW	5 %	Optional. It is not used if I/O Line internal pull-up resistor is enabled (see Config RAM item IO_PUP_ENA)
R5	I/O Line High Frequency Protection	47	Ω	Note	5 %	Optional It improves high frequency EMC robust- ness Power rating according to required EMC robustness
RF1 RF2	Input EMC Filter Resistor (Note 1)	100	Ω	Note	5 %	Optional It improves high frequency EMC robustness Power rating according to required EMC robustness
C1	Receiver Input Coupling	680	pF	100 V	10 %	
C2	Receiver Input Coupling	680	pF	100 V	10 %	
C3	Serial and Parallel Resonances Matching	optimal value	pF	100 V	5 %	Value depends on used transducer & transformer
CF1	Input EMC Filter Capacitor (Note 1)	10	pF	50 V	10 %	Optional It improves high frequency EMC robustness
C6	Battery Filter Capacitor	100	nF	50 V	10 %	
C7	Tank Capacitor for Transmitting Current	22	μF	35 V	10 %	2x ceramic type capacitor

1. Some of RF1, RF2 and CF1 components may be omitted. Use them according to required EMC robustness.

Name	Description	Typical Value	Units	Rating	Tolerance	Comment
C8	VBAT HF Filter	100	nF	50 V	10 %	
C9	I/O Line Capacitor	330	pF	50 V	10 %	Standard I/O Line slope (60 μ s) IO_SLP_FAST = 0
C9	I/O Line Capacitor	100	pF	50 V	10 %	Fast I/O Line slope (20 μs) IO_SLP_FAST = 1
Tr1	Push-pull Transformer	Transducer specific	mH	100V	5%	
PZ1	Ultrasonic Transducer	MA40MF14-1B MA55AF15-07NA MA48AF15-07N	kHz	100V	the lower the better	muRata series
D1	Reverse Polarity Protection	BAS321	-	50 V	-	

Table 1. RECOMMENDED EXTERNAL COMPONENTS (continued)

1. Some of RF1, RF2 and CF1 components may be omitted. Use them according to required EMC robustness.

Table 2. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Туре	Description	
1	RXN (Note 2)	Input	Analog Receiver Negative Input	
2	RXP	Input	Input Analog Receiver Positive Input	
3	GNDA	Ground	Analog Ground	
4	n.c.	n.c.	Pin not connected	
5	GND	Ground	TX Ground, Digital Ground	
6	DRVA	Output	Driver Output A	
7	DRVC	Output	Driver Output C (Center of winding)	
8	DRVB	Output	Driver Output B	
9	VSUP	Power Supply	Main Power Supply	
10	IO	Input/Output	I/O Line Bidirectional Interfc 8031 14.343 ref207.723 382.961 77.613 .680	

Table 3. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Units
Supply Voltage Range VSUP (Note 4)	V _{SUP}	-0.3 to 40	V
I/O Line Voltage Range	V _{IO}	–5 to 40	

Table 6. ELECTRICAL CHARACTERISTICS

(VSUP = 6 V to 18 V, TA = -40° C to 85°C, external devices as in application circuit of Figure 1.)

Symbol

Description

Max

Min

- -

- -

- -

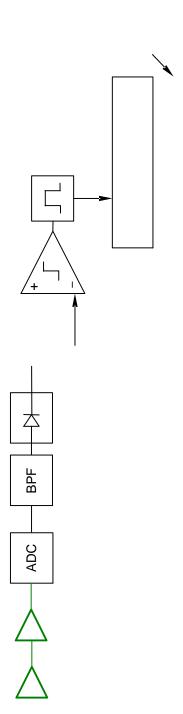


Figure 6. Block Diagram from Signal Processing Point of View

CFG_MEM (Configuration Memory)

Bit structure of configuration memory is described in Table 7. EEPROM Refresh is executed during reset and reset values of CFG_MEM cells are preloaded from EEPROM

Table 7. STRUCTURE OF CONFIGURATION MEMORY (continued)

Conf. Memory index	Name	Short Name	No of bits	Description	EEPROM (Note 11)	Default	R/W
7	Static RX Gain Code (sub-index 0)	RX_GAIN_CODE [6:0]	7	RX Gain Code 1			

Table 7. STRUCTURE OF CONFIGURATION MEMORY (continued)

Conf. Memory index	Name	Short Name	No of bits	Description	EEPROM (Note 11)	Default	R/W	
8	Dynamic Gain Control Start (sub-index 15)	DYN_GAIN_START [3:0]	4	DYN_GAIN_START 204.8				

Table 7. STRUCTURE OF CONFIGURATION MEMORY (continued)
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Conf. Memory index	Name	Short Name	No of bits	Description	EEPROM (Note 11)	Default	R/W
10	I/O Line 99.2 μs Echo Duration Enabled (sub-index 20)	IO_ECHO_PULSE_ ENA	1	0: Disabled 1: Enabled, valid only when ADV_IO_ENA = 0. When enabled, echo is always reported by 99.2 μ s pulse on I/O Line. Measurement is stopped If I/O Line is pulled low for at least 350 μ s during active measure- ment. Once active measurement is stopped, I/O Line has to be re- leased to idle state (high) for at least T _{DEB} time to re-enable the detection of next I/O Line com- mand. In case of T _{SNDx} , I/O Line is driven low for 99.2 μ s at the de- tected end of reverberations, then I/O Line is again driven low for 99.2 μ s each time when valid echo is detected (this is identical with T _{RECx}). Min. time is 99.2 μ s between two echoes in this mode. If dis- tance between echoes is less than 99.2 μ s just single echo is reported. Comment: This mode enables fully programmable measure- ment duration (by stopping of on-going measurement) while it is still transparently propagating detected echo (ToF) on I/O Line.		0	R/W

Table 7. STRUCTURE OF CONFIGURATION MEMORY (continued)

Conf. Memory index

Description

EEPROM (Note 11)

Conf. Memory index	Name	Short Name	No of bits	Description	EEPROM (Note 11)	Default	R/W
	Measurement Results – Long This index is only	MEAS_RES_LNG_ SENSOR_STATUS [7:0] (sub-index 0)	8	Refer to Encoding of Sensor Status Section		n.a	R only
14b Accessible only when WIDTH_PEAK_ENA = 1	functional when ADV_IO_ENA = 1. Otherwise, there is no response for this index.	MEAS_RES_LNG_ TOF1 [9:0] (sub-index 1)	10	ToF1 – time of 1 st echo 1–LSB ~ 51.2 μs See index 13. ToFx = 0 in case when any echo is not detected		0	R only
Ac WID		MEAS_RES_LNG_ PEAK1 [5:0] (sub-index 2)	6	Maximal magnitude of 1 st echo. The same encoding as echo magnitude in MEAS_DATA. In case of no echo, it is 0.		0	R only
		MEAS_RES_LNG_ WIDTH1 [5:0] (sub-index 3)	6	Width of 1 st echo. 1–LSB ~ 12.8 μs In case of no echo, it is 0.		0	R only
15	Command Byte (Write) IC Revision ID (Read)	CMD[7:0] / IC_ID_xx[7:0]	8	See Data communication sec- tion. <u>WRITE:</u> CMD [7:0] command byte <u>READ:</u> IC_ID_xx [7:4]: Full mask version Allowed range from 1 to15. IC_ID_xx [3:0]: Metal tune version Allowed range from 1 to15. Comment: 1 st silicon version is IC_ID_xx = 0x11 hex		IC_ID_xx [7:0]	R/W

Table 7. STRUCTURE OF CONFIGURATION MEMORY (continued)

10. n.a. = not applicable 11. Configuration memory start-up v9TJ09es:/TT2 1 Tf8 0 3.1sione69TJ09es:/TT2 1 Tf8 0 3.1sione69TJ09 ref6803 149.c(detected)TjET309.713 575.943 .j2.2

ENCODING OF SENSOR_STATUS [7:0] REGISTER

SENSOR_STATUS [0] = Acoustic Noise Flag

Flag is set if an acoustic noise is above the noise threshold (NOISE_THR) in noise monitoring time window.

Flag is automatically cleared by any measurement.

SENSOR_STATUS [1] = VSUP Under-voltage or Over-voltage during TX

Flag is set if VSUP voltage is below under-voltage threshold or crosses the over-voltage threshold during TX. If the VSUP voltage is higher than over-voltage threshold before TX, then the flag is not set.

In any case when over-voltage was detected during TX, transmission is automatically stopped, but measurement normally continues.

Flag is automatically cleared by direct measurement only.

SENSOR_STATUS [2] = TX Period Update Required

Flag is set if MEASURED_REVERB_PER is outside the range set by REVERB_PER_VAR_LIMIT and CARRIER_PER. Flag is updated by direct measurement only. Flag is automatically cleared by direct measurement only.

Flag is set after POR.

SENSOR_STATUS [3] = TX Period Update Direction

Flag indicates if MEASURED_REVERB_PER is greater than CARRIER_PER.

Flag is updated by direct measurement only. Flag is automatically cleared by direct measurement only.

SENSOR_STATUS [4] = Unexpected Decay Time (decay time too short)

Flag is set if transducer decay time (reverberation) is shorter than REVERB_MON_DUR time.

Flag is updated by direct measurement only. Flag is automatically cleared by direct measurement only.

SENSOR_STATUS [5] = End of Reverberation Time-out

Flag is set if transducer decay time is longer than end-of-reverberation time-out (TX end + END_OF_REVERB_TOUT * $51.2 \,\mu$ s). Flag is updated by direct measurement only. Flag is automatically cleared by direct measurement only.

SENSOR_STATUS [6] = THS_ERROR Flag

a3tomatically cleared by direct murementThTm-.0001 T23 Tw[(S7NSOR_ST)66.6(A)73.4(TUS [6] = THS7of ReEPROMime754(Two-Bit3

CONFIGURATION MEMORY DETAILED DATA STRUCTURES

Table 8. INDEX 0 DATA STRUCTURE (Data are transferred LSBit first.)

Data Frame Byte	Data Frame Bit	Threshold Table Bit
0	0	TEMPERATURE_CODE [0]
	7	TEMPERATURE_CODE [7]

Table 9. INDEX 1 DATA STRUCTURE (Data are transferred LSBit first.)

Data Frame Byte	Data Frame Bit	Threshold Table Bit
0	0	SENSOR_STATUS [0]
	7	SENSOR_STATUS [7]
1	8	MEASURED_REVERB_PER [0]
	15	MEASURED_REVERB_PER [7]
2	16	MEASURED_REVERB_PER [8]
	17	MEASURED_REVERB_PER [9]
	18	MEASURED_REVERB_PER [10]

Table 10. INDEX 2A DATA STRUCTURE (Data are transferred LSBit first.)

Data Frame Byte	Data Frame Bit	Threshold Table Bit
0	0	CARRIER_PER [0]
	7	CARRIER_PER [7]
1	8 CARRIER_PER [8]	
	9	CARRIER_PER [9]
	10	CARRIER_PER [10]

Table 11. INDEX 2B DATA STRUCTURE (Data are transferred LSBit first.)

Data Frame Byte	Data Frame Bit	Threshold Table Bit
0	0	DTX_PER [0]
	7	DTX_PER [7]
1	8	DRX_PER [0]
	15	DRX_PER [7]

Table 12. INDEX 7 DATA STRUCTURE (Data are transferred LSBit first.)

Data Frame Byte	Data Frame Bit	Threshold Table Bit
0	0	RX_GAIN_CODE [0]
	6	RX_GAIN_CODE [6]
	7	DYN_GAIN_ENA

Table 13. INDEX 10 DATA STRUCTURE (Data are transferred LSBit first.) (continued)

Data Frame Byte	Data Frame Bit	Threshold Table Bit
6	48	END_OF_REVERB_TOUT [0]
	53	END_OF_REVERB_TOUT [5]
	54	ADV_IO_IND_SFE
	55	IO_TRANS_DIAG_ENA
7	56	END_OF_REVERB_THR
	57	IO_ECHO_PULSE_ENA
	58	PARASITIC_PEAK_MAG [0]
	59	PARASITIC_PEAK_MAG [1]
	60	TX_RX_PER_ENA
	61	WIDTH_PEAK_ENA

Table 14. INDEX 12 DATA STRUCTURE (Data are transferred LSBit first.)

Data Frame Byte	Data Frame Bit	Threshold Table Bit
0	0	MEAS_DATA0 [0]
	5	MEAS_DATA0 [5]
	6	MEAS_DATA1 [0]
	171	MEAS_DATA1 [1]
1	8	MEAS_DATA1 [2]
	11	MEAS_DATA1 [5]
	12	MEAS_DATA2 [0]
	15	f

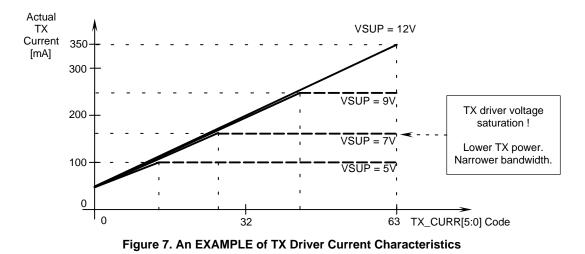


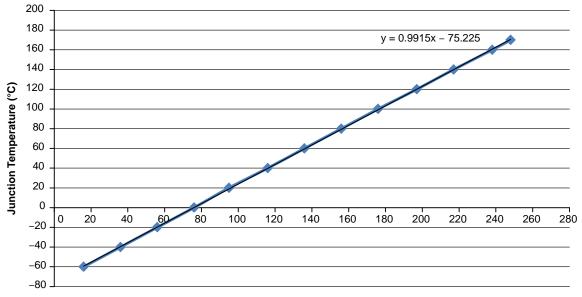
Table 17. INDEX 14B DATA STRUCTURE (Data are transferred LSBit first.)

Data Frame Byte	Data Frame Bit	Threshold Table Bit
0	0	SENSOR_STATUS [0]
	7	SENSOR_STATUS [7]
1	8	MEAS_RES_LNG_TOF1 [0]
	15	MEAS_RES_LNG_TOF1 [7]
2	16	MEAS_RES_LNG_TOF1 [8]
	17	MEAS_RES_LNG_TOF1 [9]
	18	MEAS_RES_LNG_PEAK1 [0]
	23	MEAS_RES_LNG_PEAK1 [5]
3	24	MEAS_RES_LNG_WIDTH1 [0]
	29	MEAS_RES_LNG_WIDTH1 [5]

TEMPERATURE MEASUREMENT

It is possible to monitor junction temperature by reading configuration memory index 0.

Junction Temperature	TEMP[7:0] – Config. Mem. ldx 0
-60	16
-40	36
-20	56
0	76
20	95
40	116
60	136
80	156
100	176
120	197
140	217
160	238
170	248



Temperature Code (-)

Figure 8. Junction Temperature Transfer Function

THRESHOLDS

DSP Filter Threshold (signal magnitude threshold) is controlled by values in 1 of 2 threshold Look-Up Tables (THR1 or THR2). The last threshold interval ends at 60ms (measured from the beginning of TX Ultrasonic transmission). Each threshold table consists of 12 data pairs. Each pair contains threshold level (6 bit) and delta time code (4 bit), which defines a time for linear interpolation to the particular threshold level. Threshold levels are interpreted using linear scale.

Table 19. THRESHOLD TABLE SELECTION

Command Pulse (Measurement Type)	Threshold Table Used
T _{SND1} or T _{REC1}	THR1
T _{SND2} or T _{REC2}	THR2

Table 20. THRESHOLD LEVELS THRx_LVLy[5:0] (Note 13)

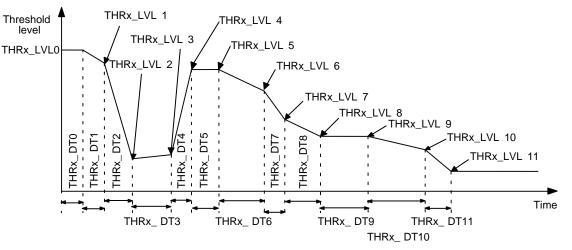
Value	Interpretation
0	Lowest threshold level
63 (0x3F)	Highest threshold level (equivalent of full ADC range signal)

Table 21. THRESHOLD DELTA TIME THRx_DTy[3:0] (Note 13)

THRx_DTy Code	Delta Time [µs]	THRx_DTy Code	Delta Time [μs]
0	100	8	1600
1	200	9	2000
2	300	10	2400
3	400	11	3200
4	600	12	4000
5	800	13	5200
6	1000	14	6400
7	1200	15	8000

13.x stands for index 1 or 2

y stands for index from 0 to 11





Threshold levels are piecewise approximated inside the thresholds intervals.

THR1_LVL11[5:0] resp. THR2_LVL11[5:0] threshold is applied until end of measurement if last delta time expires

Table 22. THRESHOLD TABLE DATA IN CONFIGURATION MEMORY (INDEX 5 AND 6)

(Data are transferred LSBit first)

Data Frame Byte	Data Frame Bit	Threshold Table Bit
0	0	THRx_LVL0 [0]
	5	THRx_LVL0 [5]
	6	THRx_LVL3 [0]
	7	THRx_LVL3 [1]
1	8	THRx_LVL1 [0]
	13	THRx_LVL1 [5]
	14	THRx_LVL3 [2]
	15	THRx_LVL3 [3]
2	16	THRx_LVL2 [0]
	21	THRx_LVL2 [5]
	22	THRx_LVL3 [4]
	23	THRx_LVL3 [5]
6	48	THRx_LVL8 [0]
	53	THRx_LVL8 [5]
	54	THRx_LVL11 [0]
	55	THRx_LVL11 [1]
7	56	THRx_LVL9 [0]
	61	THRx_LVL9 [5]
	62	THRx_LVL11 [2]
	63	THRx_LVL11 [3]
8	64	THRx_LVL10 [0]
	69	THRx_LVL10 [5]
	70	THRx_LVL11 [4]
	71	THRx_LVL11 [5]
9	72	THRx_DT0 [0]
	75	THRx_DT0 [3]
	76	THRx_DT1 [0]
	79	THRx_DT1 [3]
14	112	THRx_DT10 [0]
	115	THRx_DT10 [3]
	116	THRx_DT11 [0]
	119	THRx_DT11 [3]

DYNAMIC GAIN

Table 24. DYNAMIC GAIN FILTER COEFFICIENT DYN_GAIN_BW[1:0] CODE LUT (LOOK-UP TABLE):

DYN_GAIN_BW[1:0]	Filter Bandwidth	Coefficient "s"
0		

SUPER READ, SUPER WRITE

Super read data transfer is very useful at ultrasonic system startup. It enables to read all configuration memory items in one transaction which are initialized from EEPROM memory at power-on reset.

Then, the communication master (ECU) can use super write data transfer to initialize most of configuration memory items.

Table 26. INDEX 11 READ DATA STRUCTURE	E (Data are transferred LSBit first.)
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Data Frame Byte	Data Frame Bit	Threshold Table Bit
0	0	CARRIER_PER [0]
	7	CARRIER_PER [7]
1	8	CARRIER_PER [8]
	9	CARRIER_PER [9]
	10	CARRIER_PER [10]
	11	RX_GAIN_CODE [0]
	15	RX_GAIN_CODE [4]
2	16	RX_GAIN_CODE [5]
	17	RX_GAIN_CODE [6]
	18	DYN_GAIN_ENA
	19	REVERB_MON_DUR [0]
	23	REVERB_MON_DUR [4]
	24	REVERB_MON_DUR [5]
	25	REVERB_MON_DUR [6]
	26	REVERB_MON_DUR [7]
	f	

COMMAND BYTE

The chip is commanded to requested action by writing the particular *Command Code* to the command byte item in configuration memory at index 15. The Command Byte cannot be read back, it is write only access. Commands are protected by 8-bits coding, Hamming distance, checksum and number of message bits. Unwanted execution is practically impossible.

Table 27. COMAND BYTE

Command Code	Action
hex: 29 bin: 0010 1001	Unlock EEPROM – unlocks EEPROM for next I/O Line command. EEPROM has to be unlocked first to successfully execute Program EEPROM and Refresh Configuration RAM. EEPROM is automatically locked after the finishing of any following command.
hex: D6 bin: 1101 0110	Program EEPROM – store data in configuration memory marked "Yes" in EEPROM column in Table 1 into EEPROM
hex: 73 bin: 0111 0011	Refresh Configuration RAM from EEPROM (items stored in EEPROM only)
hex: Ax bin: 1010 xxxx	Write TP_ENA bits - TP_ENA[3:0] <= CommandByte[3:0]
hex: E7 bin: 1110 0111	Unlock reading from Conf. RAM index <512> – enables reading from Conf. RAM indexes <5 12>, otherwise there will be no response to I/O Line read command for Conf. RAM indexes <5 12>
hex: 18 bin: 0001 1000	Lock reading from Conf. RAM index <512> – disables reading from Conf. RAM indexes <5 12>
hex: 92 bin: 1001 0010	Activate low power mode – The chip enters low consumption mode and it only accepts IO Line com- mand bytes "De-activate low power mode" and "SW reset". Normal operation is not possible.
hex: 5 bin: 0000 0101	De-activate low power mode – Normal mode is re-entered from low power mode and normal opera- tion is restored. See Electrical Characteristic section for required wake time (t _{wake}) to re-enter normal mode.
hex: 5A bin: 0101 1010	SW reset – Software activation of power-on reset (POR). This command effect is equal to POR.
others	no reaction

17. Reading from Conf. RAM indexes <5 12> is enabled after POR.

Store Data to EEPROM:

1st command *Unlock EEPROM* 2nd command *Program EEPROM* Refresh Data from EEPROM: 1st command Unlock EEPROM 2nd command Refresh Configuration RAM

CHIP ID

The chip ID can be read from index 15. It is read only access.

Table 28. INDEX 15 DATA READ STRUCTURE (Data are transferred LSBit first.)

Data Frame Byte	Data Frame Bit	Threshold Table Bit
0	0	IC_ID_MT [0]
	3	IC_ID_MT [3]
	4	IC_ID_FM [0]
	7	IC_ID_FM [3]

18. IC_ID_FM: Full mask silicon version. Completely modified silicon version.

19.IC_ID_MT: Metal tune silicon subversion. Small bugs can be fixed by different active components interconnection. Metal layers are modified but active silicon components remain the same.

20. The first silicon version is: IC_ID_FM = 1, IC_ID_MT = 1

21. The second silicon version is: $IC_ID_FM = 2$, $IC_ID_MT = 1$

CUSTOMER TEST OUTPUTS, TP_ENA

Custom diagnostic test (debugging) output/input (TST1...4) signals are selected by TP_ENA bits. TP_ENA bits are set via appropriate Command byte. DSP internal

"analog" signals are PDM modulated. External low-pass filters are required. See table below for valid test signal combinations.

Table 29. CUSTOMER TEST OUTPUTS, TP_ENA

TP_ENA[3:0]	TST0	TST1	TST2	TST3		
0000 (Default)	Hi–Ζ / 4 kΩ	Hi–Ζ / 4 kΩ	Hi–Ζ / 4 kΩ	Hi–Ζ / 4 kΩ		
0001	Hi–Ζ / 4 kΩ	Hi–Ζ / 4 kΩ	THRESHOLD[9:0] PDM2	ECHO_MAG[9:0] PDM1		
0010	Hi–Ζ / 4 kΩ	Hi–Ζ / 4 kΩ	ECHO_ENVELOPE PDM2	ECHO_MAG[9:0] PDM1		
0011	Hi–Ζ / 4 kΩ	Hi–Ζ / 4 kΩ	Not Defined	Not Defined		
0100	Hi–Ζ / 4 kΩ	Hi–Z / 4 k Ω	ECHO_DET	ECHO_MAG[9:0] PDM1		
0101	Hi–Ζ / 4 kΩ	Hi–Ζ / 4 kΩ	Not Defined	Not Defined		
0110	Hi–Ζ / 4 kΩ	Hi–Z / 4 kΩ Hi–Z / 4 kΩ GAIN[7:0] PDM2				
0111	Hi–Ζ / 4 kΩ	Hi–Ζ / 4 kΩ	IO_RXD	IO_DRV (input)		
1000	Single Ended Analog RX Output	Permanent Digital Output Set to "1"	Hi–Z / 4k	Hi–Z / 4k		
1001	Single Ended Analog RX Output	Permanent Digital Output Set to "1"	THRESHOLD[9:0] PDM2	ECHO_MAG[9:0] PDM1		
1010	Single Ended Analog RX Output	alog Permanent Digital ECHO_ENVELOF Output Set to "1" PDM2		ECHO_MAG[9:0] PDM1		
1011	11 Single Ended Analog Per RX Output Ou		Not Defined	Not Defined		
1100	1100 Single Ended Analog Per RX Output Ou		ECHO_DET	ECHO_MAG[9:0] PDM1		
1101	Single Ended Analog Permanent Digital Not Defined RX Output Output Set to "1"		Not Defined	Not Defined		
1110	Single Ended Analog RX Output	Permanent Digital Output Set to "1"	GAIN[7:0] PDM2	ECHO_MAG[9:0] PDM1		
1111	Single Ended Analog RX Output	Permanent Digital Output Set to "1"	IO_RXD	IO_DRV (Input)		

22. Hi–Z / 4 k Ω = IO is not driven but pull down active

23. VGA_Gain = (analog(PDM2) / 20 mV) * (30 / 63) dB 24. Initial/POR value shall be 0 decimal ("0000" binary) – test outputs are disabled 25. GAIN[7:0] is effectively using half of the full-scale of PDM output

26. Threshold[9:0] is effectively using half of the full-scale of PDM output

Recommended External Low-pass Filter

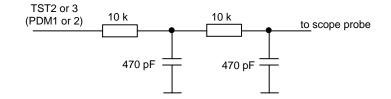


Figure 11. Recommended PDM External Low-pass Filter

EEPROM PROGRAMMING SEQUENCE

EEPROM programming operation is performed in 12 successive steps:

- 1. Power-on the device.
- 2. Read Configuration RAM index 1 to clear SENSOR_STATUS (SENSOR_STATUS[7] = HW ERROR).
- 3. Write data into Configuration RAM (EEPROM shadow registers).
- 4. Verify EEPRPOM shadow registers content by reading back Configuration RAM index 11 (super read) and index 9. If mismatch detected, go-to step 2.
- 5. Unlock EEPROM Write Command Code 0x29hex into Configuration RAM index 15.
- 6. Program EEPROM Write Command Code 0xD6hex into Configuration RAM index 15.

- 7. Wait 25 ms. It is needed to complete programming of the EEPROM memory.
- 8. Unlock EEPROM Write Command Code 0x29hex into Configuration RAM index 15.
- 9. Refresh Configuration RAM Write Command Code 0x73hex into Configuration RAM index 15.
- Read Configuration RAM index 1 to get SENSOR_STATUS. SENSOR_STATUS[7] (EEPROM ERROR or HW_ERROR) should be 0. If SENSOR_STATUS[7] is 1, EEPROM failure occurred, then, go-to step 3.
- Verify EEPRPOM shadow registers content by reading back Configuration RAM index 11 (super read) and index 9. If mismatch detected, go-to step 3.
- 12. Power-off the device.

EEPROM ERROR CORRECTION BLOCK

The error correction block utilizes SECDED coding for one bit error correction and 2 bits error detection. As data are split in words 16 bits long each, 5 extra bits are required for encoding ECC (Hamming code) and one extra bit for parity check (two bits error detection). The encoding bits are spread into the bit matrix accordingly to the Tab.2.

Bit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
<u>, Da</u> ta Gel III	P0 1 X (1)	P1	_DQ ∎11 X ©	-E2-	<u>.</u> 원. X성	<u>-</u> <u>1</u> 2	₽3 ₩	<u>₽</u> 3 ∎11	- <u>D</u> † X≼¢1	- JN5 - =		DZ.	_D& ¥⊊ÿL		₽19 ×≪	E4	D11 X公	<u>D</u> 12 - 1		D14	015 X≨©L
21	ĺ	X 92	X			X 🕂 :	Xe			XX	X 🛛 :			X 🛛 :	XX			X 🙁 🗄	X 🕅 :		
12				XX	X %.	XX	X %					XX	XX	X %	XX					X %.	XX
23 1								XX	XX	XX	XX	XX	XX	XX	XX						
PM 11					ļ					į						X 4.	X	Xe	XX	XX	Xe

Figure 12. 16-bits Word SECDED Encoding

Error correction is based on the calculation of the parity bits. The parity bits are spread in such a way, that if the parity fails, the position of the error bit is defined directly by the position of the failing bits.

Example 1:

If the failure appears on bit 9 (D4), the parity of P0 and P3 will be wrong (column for bit 9, X's are for P0 and P3). Putting one on the wrong positions of the parity when writing parity word would be:

P4, P3, P2, P1, P0 = 01001 binary = 9 decimal.

Example 2:

Error is on parity bit P4 - the word is 10000 = bit 16 decimal (that is directly the parity bit P4).

If two bits error is detected, invalid data of the impacted address in the shadow registers will not be updated.

IO_LINE_CTRL (COMMAND PULSE, MEASUREMENT CONTROL, DATA COMMUNICATION)

I/O Line is a master-slave point-to-point communication link. If more than one chip is connected to master (ECU) unit, it creates star topology. Every I/O Line communication starts with particular command pulse. Its length and meaning is in table below:

Table 30. IO_LINE COMMAND PULSE

Command Pulse	Min. Pulse Length [μs]*	Typ. Pulse Length [μs]	Max. Pulse Length [μs]*	Addressing	Description
T _{SND1}	328	400	472	-	TX+RX (direct measurement with THR1 table)
T _{REC2}	503	580	657	-	RX only (indirect measurement with THR2 table)
T _{REC1}	697	780	863	-	RX only (indirect measurement with THR1 table)
T _{SND2}	920	1010	1100	-	TX+RX (direct measurement with THR2 table)
T _{DATA}	1172	1270	1368	R/nW, xxxx	Data communication

I/O Line command pulse, which is generated by ECref358.639 586.82.3.345 194.23 .6.943.has-.be alwayT2 1 range from minimaled by n table -.00ximaled by n table



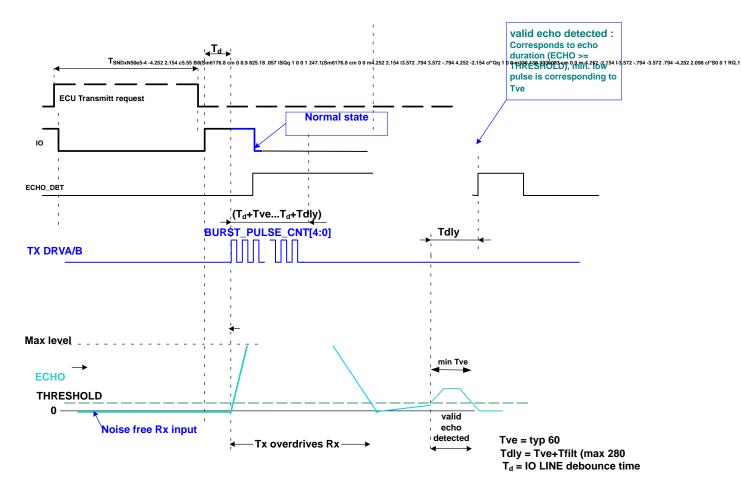


Figure 15. Send Command Sequence with Threshold Table 1 (T_{SND1}) and Threshold Table 2 (T_{SND2}) Noise Free and Defect Free Case

T_{SND1}/T_{SND2} Command (Direct Measurement); ADV_IO_ENA = 1

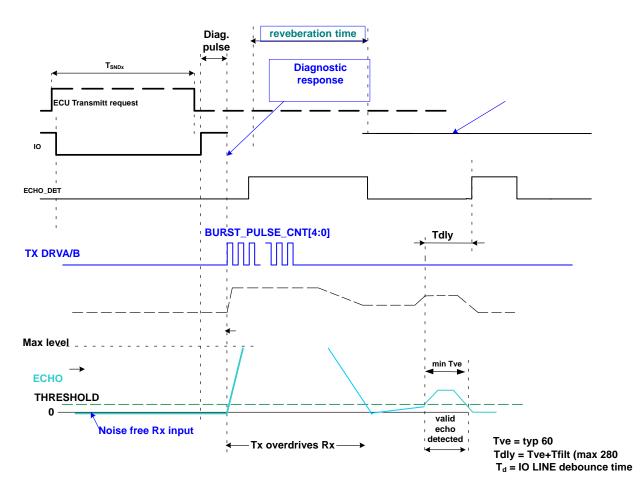
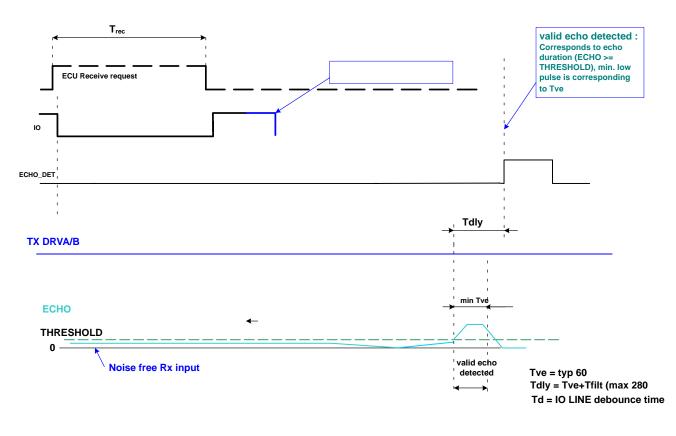


Figure 16. Send Command Sequence with Threshold Table 1 (T_{SND1}) and Threshold Table 2 (T_{SND2}) Noise Free and Defect Free Case

T_{REC1}/T_{REC2} Command (Indirect Measurement); ADV_IO_ENA = 0





T_{REC1}/T_{REC2} Command (Indirect Measurement); ADV_IO_ENA = 1

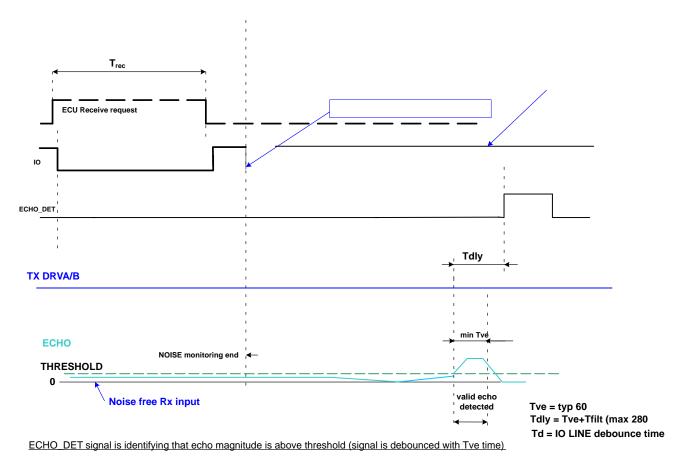
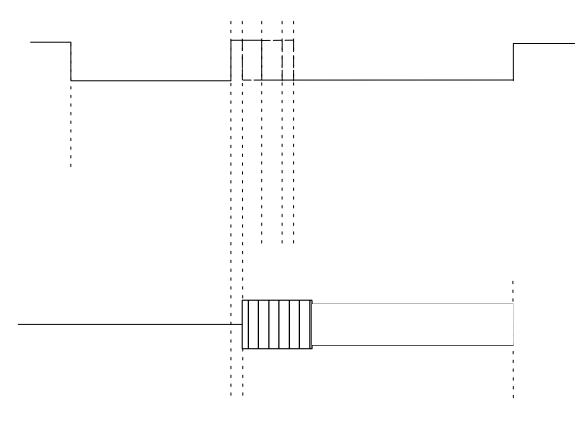


Figure 18. Receive Command Sequence Noise Free and Defect Free Case



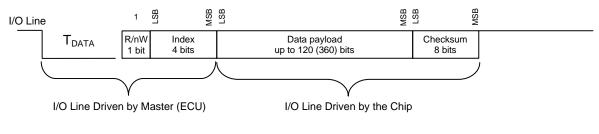
Note: All NCV75215 generated timing has accuracy of 3%.

Figure 19. I/O Line Noise Reporting and Sensor Defect Reporting (Diagnostic Pulse) for T_{SNDx} and T_{RECx} Commands

DATA COMMUNICATION

Every I/O Line data communication starts by T_{DATA} command pulse. The chip supports index data read and write transfers.

Read index data:



Write index data:

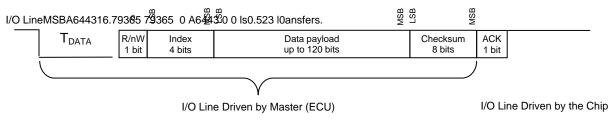
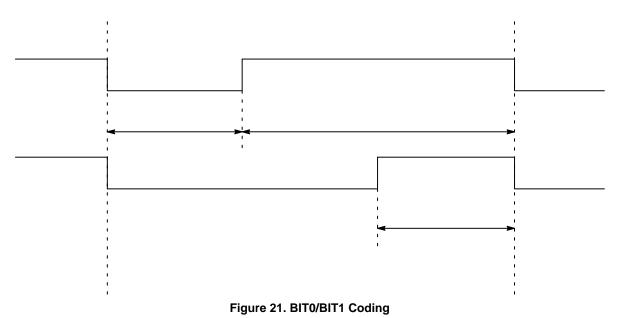


Figure 20. Read and Write Index Data





CHECKSUM

Validity of data transferred over I/O Line is ensured by Enhanced 8-bit Checksum. The checksum calculation is explained in example below.

Example: R/nW = 1 (read operation) Index = 2 = 0010 bin

ACKNOWLEDGE BIT

Meaning of Acknowledge bit is explained in Figure 22.

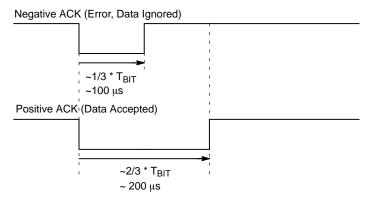


Figure 22. I/O Data Communication – Meaning of Acknowledge Bit

The chip transmits acknowledge bit after reception of the last checksum bit. Acknowledge bit is transmitted after data write transfer only.



SCALE 2:1

TSSOP-16 WB CASE 948F ISSUE B

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