SPI Controlled H-bridge and Dual-Half Bridge Pre-Driver

NCV7535

TSSOP20
CASE 948AD

The NCV7535 is a monolithic SPI controlled H−bridge pre−driver providing control of a DC−motor. Due to the SPI interface, it includes enhanced feature set useful in automotive systems. This allows a highly integrated solution.

Features

- Main Supply Functional Operating Range from 5 V to 28 V
- Main Supply Parametrical Operating Range 6 V to 18 V
- Active and Standby Operating Modes
- Compatible to Low−ohmic Standard Level N−channel MOSFETs
- Enhanced Charge Pump for Internal High−side Supply
- Specific Pin for N−channel MOSFET Reverse Battery Protection
- Programmable Slew−rate, Dead−time and Over−current Level
- PWM Operation up to 25 kHz
- Active or Passive Freewheeling
- High−side or Low−side Freewheeling
- Configurable into Single H−bridge or Dual Half−bridges Mode
- 24−Bit SPI Interface
- Protection Against Short−circuit, Over−voltage, Under−voltage and Over−temperature
- TSSOP20 Package
- AEC−Q100 Qualified and PPAP Capable
- This is a Pb−free Device

Typical Applications

- Replacing Systems with Relays by MOSFETs
- Motor Drivers

MARKING DIAGRAM

A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS

ORDERING INFORMATION

Device	Package	Shipping†
NCV7535DBR2G	TSSOP20 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Pin Type	Description
1	CP	Analog output	Charge pump output for high−side gate drive supply
2	CPM	Analog output	Minus terminal for pump capacitor
3	CPP	Analog output	Plus terminal for pump capacitor
4	VCC	Supply input	Logic supply of the device
5	CSN		

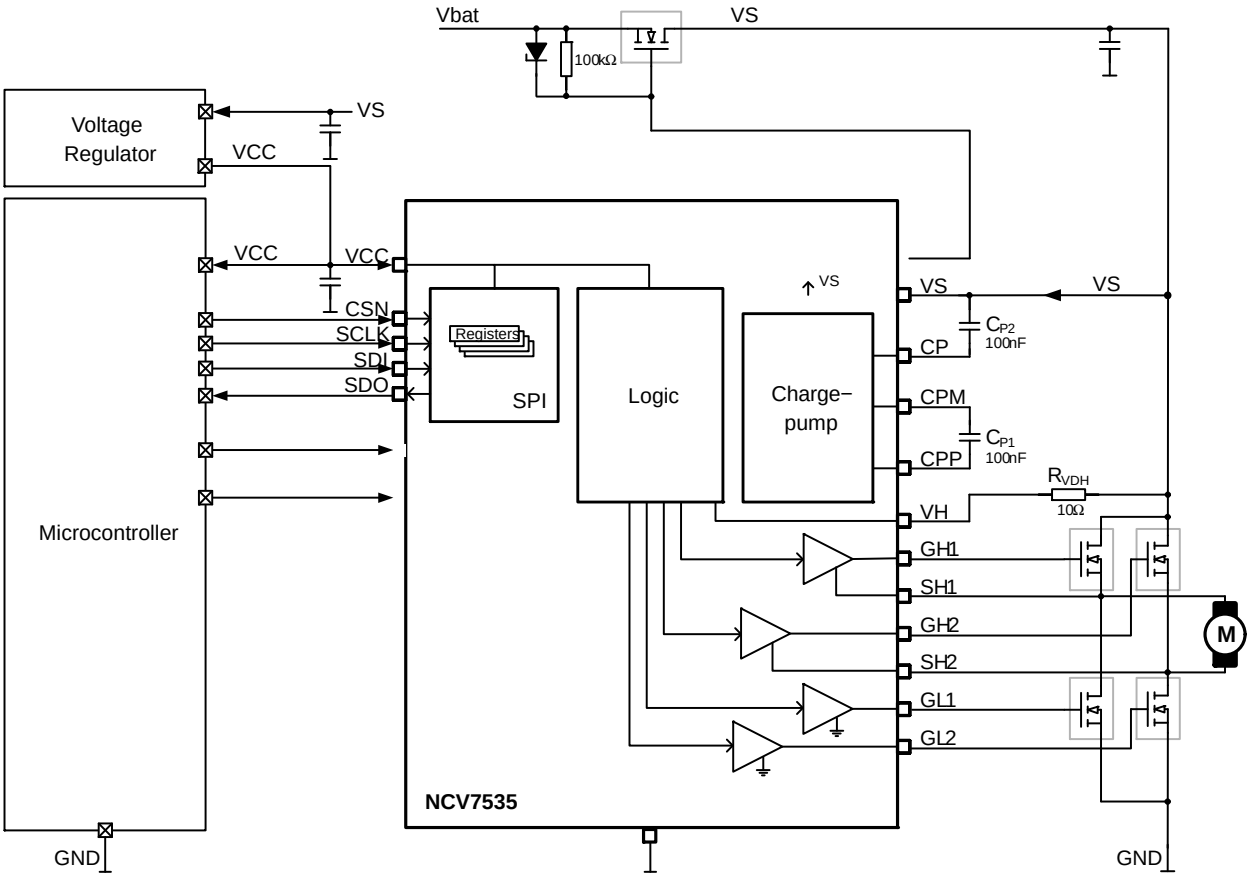

Figure 1. Block Diagram and Typical Application Diagram

Table 5. ELECTRICAL CHARACTERISTICS

6 V ≤ VS ≤ 18 V, 4.5 V ≤ VCC ≤ 5.25 V, −40°C ≤ T_J ≤ 150°C; unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OVERVOLTAGE AND UNDERVOLTAGE DETECTION						
Vov_vs(off)	VS Over−Voltage detection	VS increasing	22.5	24	25.5	V
Vov_vs(on)		VS decreasing	20.5	22	23.5	
Vov_vs(hys)	VS Over−Voltage hysteresis	Vov_vs(off) – Vov_vs(on)		2		V
Vuv_vcc(off)	VCC Under−Voltage detection	VCC increasing		3.0	3.2	V
Vuv_vcc(on)		VCC decreasing	2.6	2.8		
Vuv_vcc(hys)	VCC Under−Voltage hysteresis	Vuv_vcc(off) – Vuv_vcc(on)		0.2		V
td_uvov	VS Under−Voltage / Over−Voltage filter time	Time to set the power supply fail bit UOV_OC in the Global Status Byte	48	76	125	μs
CHARGE−PUMP						
fCP	Charge pump frequency		300	425	550	kHz
Vcp1	Charge pump output voltage1	VS > 10.5 V, Icp = −10 mA (see Note 5), Cp1 = Cp2 = 100 nF	VS+8		VS+15.1	V
Vcp2	Charge pump output voltage2	VS > 6 V, Icp = −5 mA, Cp1 = Cp2 = 100 nF	VS+4.5			V
R_CPR	Switch impedance between CPR and CP	tested at 0.5 mA	250	300	420	Ω
I_CPR	Current capability of Reverse Polarity Gate Control				1	mA
GATE OUTPUTS						
dVGx_fast	Slew Rate of gate driver	VS=13.5 V, SPI bit CONFIG.SRF=1, Gate charge ≤ 60 nC		30		V/μs
dVGx_slow	Slew Rate of gate driver	VS=13.5 V, SPI bit CONFIG.SRF=0, Gate charge ≤ 60 nC		5		V/μs
Ipull_SHx_act	SH1/2 pull−up current in Active mode, H−Bridge off	SHx = 1.2 V	−240	−140	−60	μA
fPWM	PWM frequency				25	kHz
tprop	Propagation delay of PWM rising or falling edge to gate activation	Measured at 50% PWM input signal to 10% rising or 90% falling edge of the gates Measured with dVGxfast & 5 nF load	200	500	800	ns
tjitter	Jitter versus PWM rising or falling edge to gate activations	Measured at 50% PWM input signal to 10% rising or 90% falling edge of the gates Measured with dVGxfast & 5 nF load	−150	0	150	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. The device must see a VS voltage above VS Under−voltage (Vuv_vs) and below VS Over−voltage (Vov_vs) detection levels to drive the H−bridge normally.
4. The Load must not have path to VS
5. ICP is internal load due to H−bridge switching (no external load)
6. Internal propagation delay and re−synchronization time are not included
7. Over−current is not detected during the transitions

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DIGITAL INPUTS EN, CSN, SCLK, SDI; TIMING						
tcsn_hi_stdby	Minimum CSN high time, switching from Standby mode			5	10	μs
tcsn_hi_min	Minimum CSN high time, Active mode			2	4	μs
ten_neg	Minimum EN negative pulse which is seen as 0 (after synchronization)		325			ns
tcsn_hi_en_hi	Minimum time between CSN high and EN high edge		100			ns
ten_hi_csn_lo	Minimum time between EN high and CSN low edge		100			ns
OPERATING MODES TIMING						
tsact	Time delay from Standby (CSN rising edge MODE=1 and EN=1) into Active mode (NRDY=0)			240	340	μs
tacts	Time to place device from Active to Standby after rising edge CSN and MODE=0 or EN=0				13.5	μs
tsrt_stby	Time to place device back to Standby from Startup phase if after 1st SPI communication MODE=0 or EN=0				8	μs
THERMAL PROTECTION						
Tjsd_on	Thermal shutdown threshold, Tj increasing	Junction temperature	160	175	195	°C
Tjsd_off	Thermal shutdown threshold, Tj decreasing	Junction temperature	155			°C
Tjsd_hys	Thermal shutdown hysteresis			5		°C
td_tx	Filter time for thermal shutdown	TSD Global Status bit	10		125	μs

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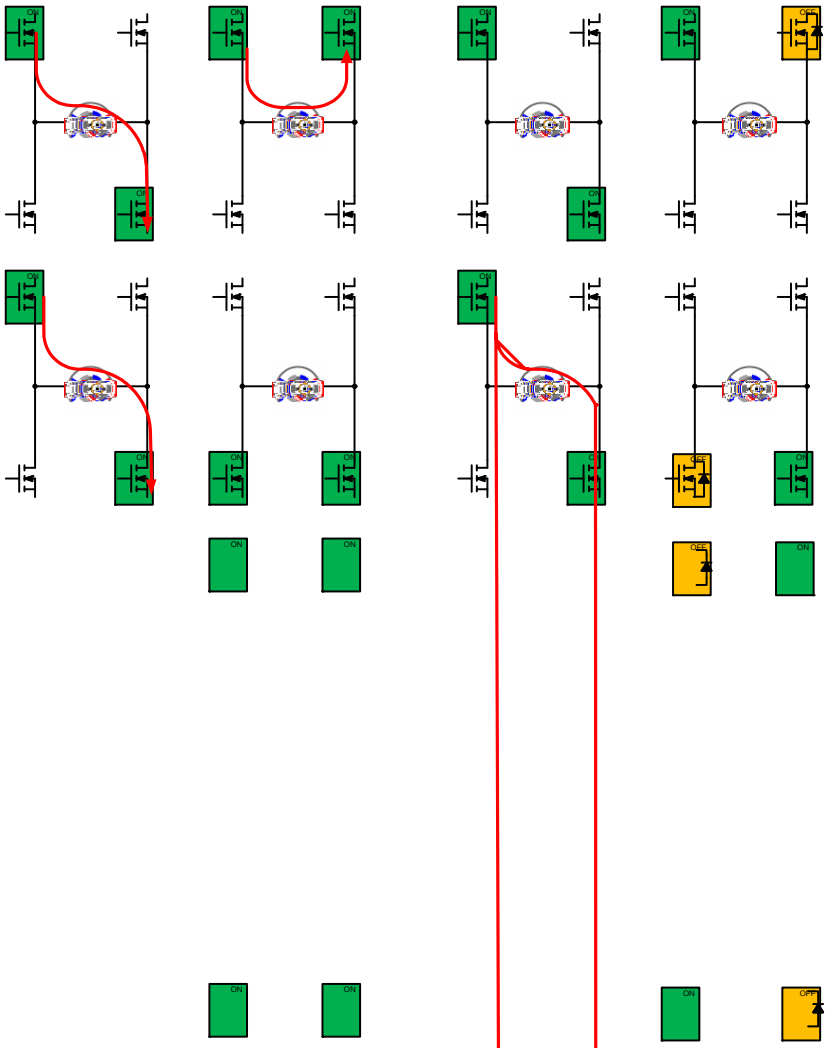


Figure 6. Bridge Configurations

Over Voltage and Under Voltage Shutdown

If the supply voltage VS rises above the switch off voltage Vov_vs(off) or falls below Vuv_vs(off), all output transistors are switched OFF.

Over Temperature Shutdown

The device provides an over−temperature protection. If the junction temperature rises above Tjsd_on threshold, the thermal shutdown bit TSD is set and all the output transistors are switched OFF. The shutdown delay for the over−temperature is td_tx. The output channels can be re−enabled after the device is cooled down and the TSD flag has been reset by the microcontroller by setting CONTROL_0.MODE = 0.

Over Current Shutdown

Over Current is detected by the device when the drain−source voltage (Vds) of the external N−MOSFETs saturates. Above the Over−Current threshold (programmable via SPI register bits CONFIG.OCTH[2:0]), the over current is detected. During the bridge transitions, the error detection is masked (Vds can be higher than the OCTH during the slopes).

If the device is in full−bridge mode (CONFIG.HALF_HB = 0), the full bridge is disabled in case of over−current.

Otherwise, if the device is in half−bridge mode (CONFIG.HALF_HB = 1), only the half−bridge in affected by the over−current is disabled.

SPI Control

General Description

The 4−wire SPI interface establishes a full duplex synchronous serial communication link between the NCV7535 and the application's microcontroller. The NCV7535 always operates in slave mode whereas the controller provides the master function. A SPI access is performed by applying an active−low slave select signal at CSN. SDI is the data input, SDO the data output. The SPI master provides the clock to the NCV7535 via the SCLK input. The digital input data is sampled at the rising edge at SCLK. The data output SDO is in high impedance state (tri−state) when CSN is high. To readout the global error flag without sending a complete SPI frame, SDO indicates the corresponding value as soon as CSN is set to active. With the first rising edge at SCLK after the high−to−low transition of CSN, the content of the selected register is transferred into the output shift register.

The NCV7535 provides one control registers (CONTROL_0), one status register (STATUS_0) and one general configuration register (CONFIG). Each of these register contains 16−bit data, together with the 8−bit frame header (access type, register address), the SPI frame length is therefore 24 bits. In addition to the read/write accessible

Chip Select Not (CSN)

CSN is the SPI input pin which controls the data transfer of the device. When CSN is high, no data transfer is possible and the output pin SDO is set to high impedance. If CSN goes low, the serial data transfer is allowed and can be started. The communication ends when CSN goes high again.

Serial Clock (SCLK)

If CSN is set to low, the communication starts with the rising edge of the SCLK input pin. At each rising edge of SCLK, the data at the input pin Serial IN (SDI) is latched. The data is shifted out thru the data output pin SDO after the falling edges of SCLK. The clock SCLK must be active only within the frame time, means when CSN is low. The correct transmission is monitored by counting the number of clock pulses during the communication frame. If the number of SCLK pulses does not correspond to the frame width indicated in the SPI−frame−ID (Chip ID Register, address 3Eh) the frame will be ignored and the communication failure bit “TF” in the global status byte will be set. Due to this safety functionality, daisy chaining the SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected ICs is recommended.

Serial Data In (SDI)

During the rising edges of SCLK (CSN is low), the data is transferred into the device thru the input pin SDI in a serial way. The device features a stuck−at−one detection, thus upon detection of a command = FFFFFFh, the device will be forced into the Standby mode. All output drivers are switched off.

Serial Data Out (SDO)

The SDO data output driver is activated by a logical low level at the CSN input and will go from high impedance to a low or high level depending on the global status bit, FLT (Global Error Flag). The first rising edge of the SCLK input after a high to low transition of the CSN pin will transfer the content of the selected register into the data out shift register. Each subsequent falling edge of the SCLK will shift the next bit thru SDO out of the device.

Command Byte / Global Status Byte

Each communication frame starts with a command byte (Table 6). It consists of an operation code (OP[1:0]) which specifies the type of operation (Read, Write, Read & Clear, Readout Device Information) and a six bit address (A[5:0]). If less than six address bits are required, the remaining bits are unused but are reserved. Both Write and Read mode allow access to the internal registers of the device. A “Read & Clear”−access is used to read a status register and subsequently clear its content. The “Read Device Information” allows to read out device related information such as ID−Header, Product Code, Silicon Version and Category and the SPI−frame ID. While receiving the command byte, the global status byte is transmitted to the microcontroller. It contains global fault information for the device.

ID Register

Chip ID Information is stored in five special 8−bit ID. The content can be read out at the beginning of the communication.

Table 6. COMMAND BYTE (IN) / GLOBAL STATUS BYTE (OUT)

Bit	Command Byte (IN) / Global Status Byte (OUT)							
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NCV7535 IN	OP1	OP0	A5	A4	A3	A2	A1	A0
NCV7535 OUT	FLT	TF	RESB	TSD	−	UOV_OC	−	NRDY
Reset Value	1	0	0	0	0	0	0	1

Table 8. COMMAND BYTE, REGISTER ADDRESS

A[5:0]	Access	Description	Content
00h	R/W	Control Register CONTROL_0	Device mode control, external H−Bridge outputs control
10h	R/RC	Status Register STATUS_0	Pre−driver diagnosis
3Fh	R/W	Configuration Register CONFIG	Mask bits for global fault bits, PWM mapping

Table 9. GLOBAL STATUS BYTE CONTENT

FLT	Global Fault Bit	
0	No fault Condition	Failures of the Global Status Byte, bits [6:0] are always linked to the Global Fault Bit FLT. This bit is generated by an OR combination of all failure bits of the device (RESB bit inverted). It is reflected via the SDO pin while CSN is held low and NO clock signal is present (before first positive edge of SCLK). The flag will remain valid as long as CSN is held low. This operation does not cause the Transmission error Flag in the Global Status Byte to be set.
1	Fault Condition	
TF	**SPI Transmission Error**	
0	No Error	If the number of clock pulses within the previous frame was unequal 0 (FLT polling) or 24. The frame was ignored and this flag was set.
1		

SPI REGISTERS CONTENT

CONTROL_0 Register

Address: 00h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access type	−	−	−	−	−	−	RW	RW	RW	RW	−	RW	RW	RW	RW	RW
Bit name	−	−	−	−	−	−	HS1	LS1	HS2	LS2	−	FWH	FWA	OVR	UVR	MODE
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

HS/LS Outputs Control	HSx	LSx

CONFIG Register

Address: 3Fh

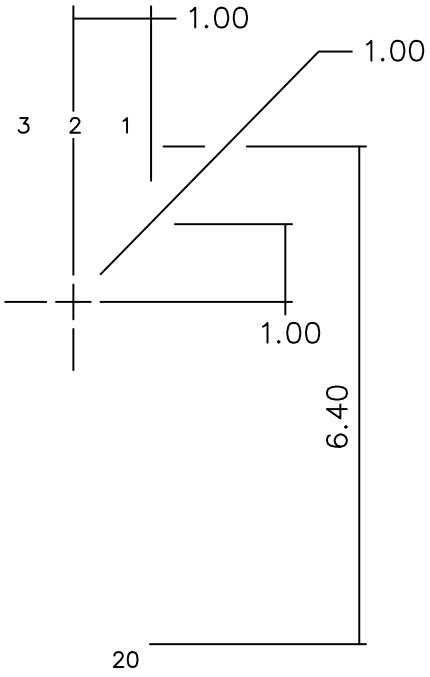
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	−	−	−

Over−

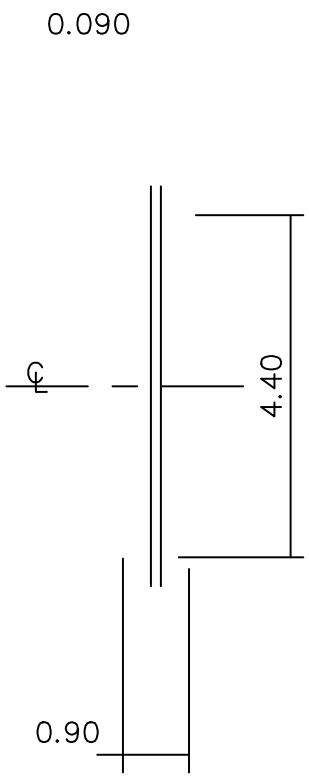
PACKAGE DIMENSIONS

TSSOP 20
CASE 948AD−01
ISSUE O

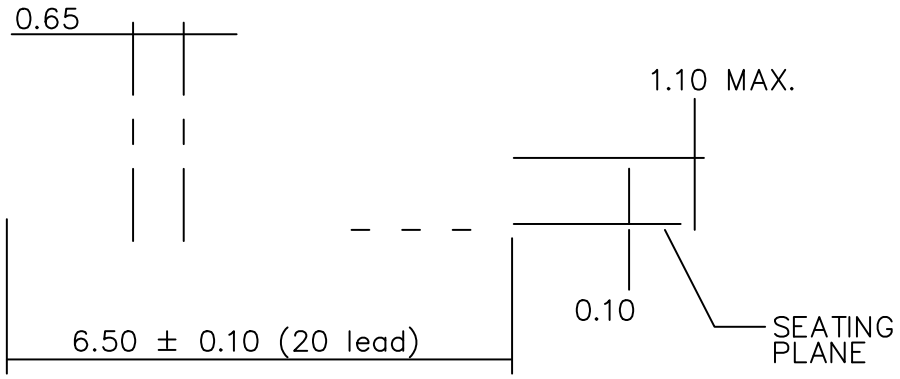
DATE 17 JUL 2008



TOP VIEW



END VIEW



SIDE VIEW