NCV7544

FLEXMOS™ Quad Half-Bridge MOSFET Pre-driver

The NCV7544 programmable four channel half−bridge MOSFET pre−driver is one of a family of FLEXMOS automotive grade products for driving logic−level NMOS FETs. The product is controllable by a combination of serial SPI and CMOS−compatible parallel inputs. An internal power−on reset provides controlled power up. A reset input allows external re−initialization and a failsafe input allows the device to be safely disabled in the event of system upset.

Each channel independently monitors its external MOSFETs' drain−source voltages for fault conditions. Overload detection thresholds are SPI−selectable and the product allows different detection thresholds for each channel.

The FLEXMOS family of products offers application scalability through choice of external MOSFETs.

Features

- Supports Functional Safety Compliance
- 4 Half−bridge Pre−drivers for External Logic−level NMOS FETs
- Integrated Charge Pump for:
  - High−side Gate Drive
  - Switched Reverse Battery Protection
- 5 V CMOS Compatible I/O:
  - 16−bit SPI Interface for Control and Diagnosis
  - Reset and Failsafe Inputs
  - 2 PWM Control Inputs
- Programmable:
  - Slew Rate Control
  - Overload Protection Thresholds
- Low Quiescent Current
- Wettable Flanks Pb−free Packaging
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

Benefits

- Scalable to Load by Choice of External MOSFET

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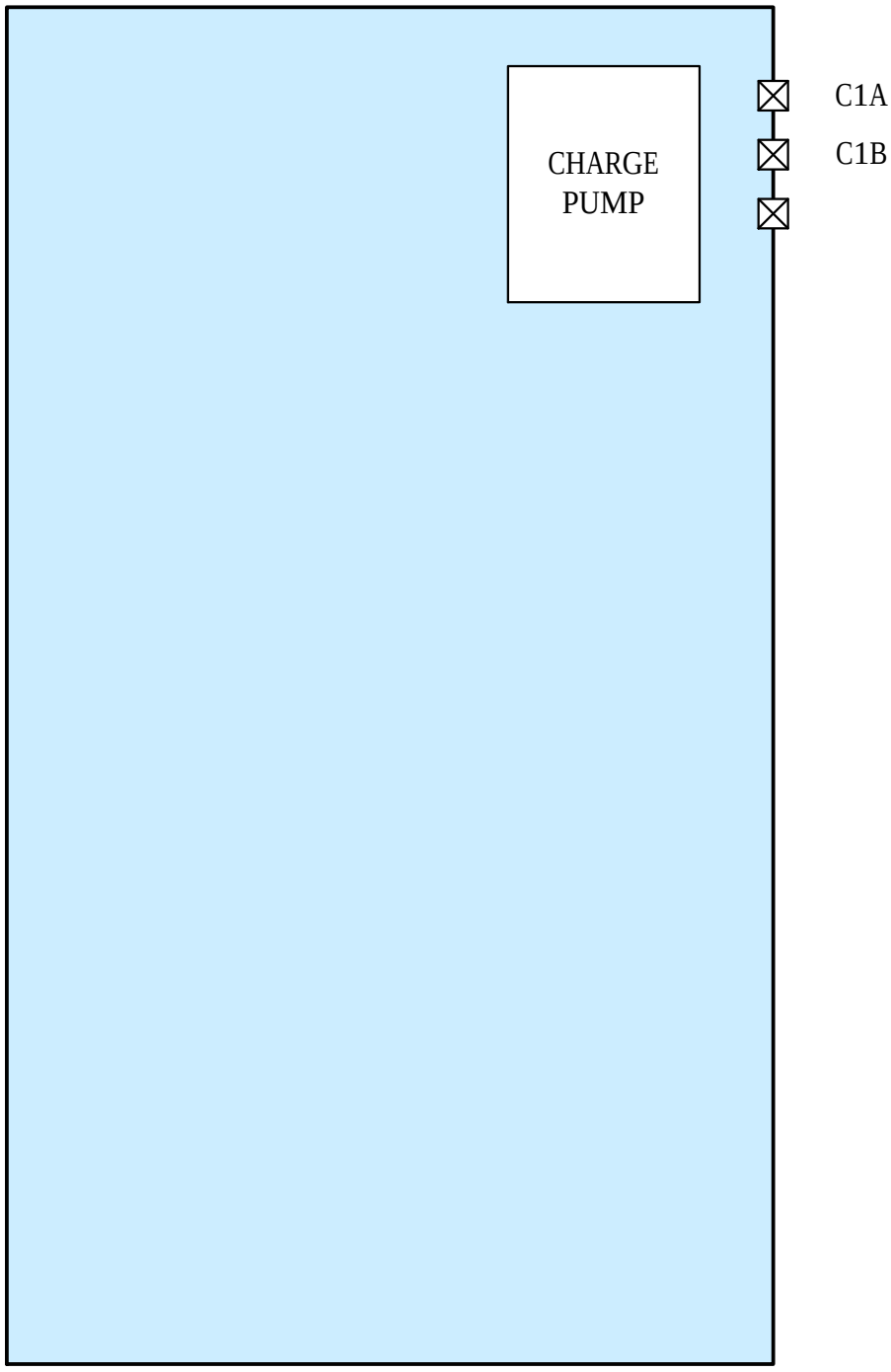
QFN32 5x5, 0.5P (PUNCHED)
CASE 485CZ

MARKING DIAGRAM

NCV7544	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
▪	= Pb−Free Package

Device	Package



{2018.06.25}

Figure 1. Block Diagram

PARAMETRIC TABLES

ELECTRICAL CHARACTERISTICS

(4.5 V ≤ VCC ≤ 5.5 V, 7.0 V ≤ VS ≤ 18 V, RSTB = VCC, CR1.D[10] = 1, −40°C ≤ T_J ≤ 150°C, unless otherwise specified.) (Note 5)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
VS Supply						
Standby Current	I_{VS_SBY}	VS = 12.0V, 0 □ VCC □ 5.5 V, RSTB = 0, T_A = 25°C	–	–	5.0	μA
Operating Current	I_{VS_OP0}	VCC = 5.0 V , RSTB = 1, T_A = 25 °C Default Settings at POR, SPI Inactive CR1.D[10]=0	–	0.9	5.0	mA
	I_{VS_OP1}	CR1.D[10]=1	–	13.4	25.0	mA
Under−voltage Lockout	VS_{UVLO}	VS decreasing, SR0.D[5] □ 1	4.5	5.0	5.5	V
Under−voltage Hysteresis	VS_{UVHY}	SR0.D[5] □ 0 (after read status if VS > $VS_{UVLO+UVHY}$)	100	200	–	mV
Under−voltage Filter Time	t_{UVDGL}	VS decreasing	4.0	5.0	6.0	μs
Over−voltage Shutdown	VS_{OVSDR}	VS increasing, SR0.D[4] □ 1	19.0	20.0	21.0	V
	VS_{OVSDF}	VS decreasing, SR0.D[4] □ 0	18.0	19.0	20.0	V
Over−voltage Hysteresis	VS_{OVHY}	SR0.D[4] □ 0 (after read status if VS < $VS_{OV\ –\ OVHY}$)	–	0.9	–	V
Over−voltage Filter Time	t_{OVDGL}	VS increasing	4.0	5.0		

ELECTRICAL CHARACTERISTICS

(4.5 V ≤ VCC ≤ 5.5 V, 7.0 V ≤ VS ≤ 18 V, RSTB = VCC, CR1.D[10] = 1, −40°C ≤ T_J ≤ 150°C, unless otherwise specified.) (Note 5)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Charge Pump Over−voltage Detection	CP_{OV}	VS increasing	28.0	30.25	32.5	V
Charge Pump Over−voltage Hysteresis	CP_{OV_HYS}		0.5	1.0	2.0	V
CP Switch Resistance	R_{CPTOT}	*Guaranteed by Simulation* 8x CP switches in parallel, T_A = 25°C	–	1.5	–	Ω
Switched CP Output Resistance	R_{CPSW_ON}	CR1.D[9] = 1, I(CPSW) = 5 mA	–	–	100	Ω
Switched CP Output Leakage	CP_{SW_LKG}	CR1.D[9] = 0	−1.0		1.0	uA
Digital I/O						
V_{IN_X} High	V_{INHX}	CSB, SCLK, SI, RSTB, FSI[1], PWMx	3.5	–	–	

ELECTRICAL CHARACTERISTICS

(4.5 V ≤ VCC ≤ 5.5 V, 7.0 V ≤ VS ≤ 18 V, RSTB = VCC, CR1.D[10] = 1, −40°C ≤ T_J ≤ 150°C, unless otherwise specified.) (Note 5)

Characteristic	Max	Unit

ELECTRICAL CHARACTERISTICS
(4.5 V ≤ VCC ≤ 5.5 V, 7.0 V ≤ VS ≤ 18 V, RSTB = VCC, CR1.D[10] = 1, −40°C ≤ T_J

ELECTRICAL CHARACTERISTICS

5 V ≤ VS ≤ 18 V, RSTB = VCC, CR1.D[10] = 1, −40°C ≤ T_J ≤ 150°C, unless otherwise spe

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
VDS Detection Time Rising or Falling Slope	t_{DLYX}	T_DLYX[3:0] = 0x00	(Note 7)	0.35	(Note 7)	
		T_DLYX[3:0] = 0x01		0.55		
		T_DLYX[3:0] = 0x02		0.75		
		T_DLYX[3:0] = 0x03		0.95		
		T_DLYX[3:0] = 0x04		1.15		
		T_DLYX[3:0] = 0x05		1.35		
		T_DLYX[3:0] = 0x06		1.55		
		T_DLYX[3:0] = 0x07		1.75		
		T_DLYX[3:0] = 0x08		1.95		
		T_DLYX[3:0] = 0x09		2.15		
		T_DLYX[3:0] = 0x0A		2.35		
		T_DLYX[3:0] = 0x0E		3.15		
		T_DLYX[3:0] = 0x0F		3.35		
Dynamic VDS Monitor Filter Time	t_{DGL_DYN}		231	330	429	ns
Dynamic VDS Monitor Propagation Delay	t_{VDSD_PD}		–	59	100	ns
HBx Monitor Threshold	VHB					

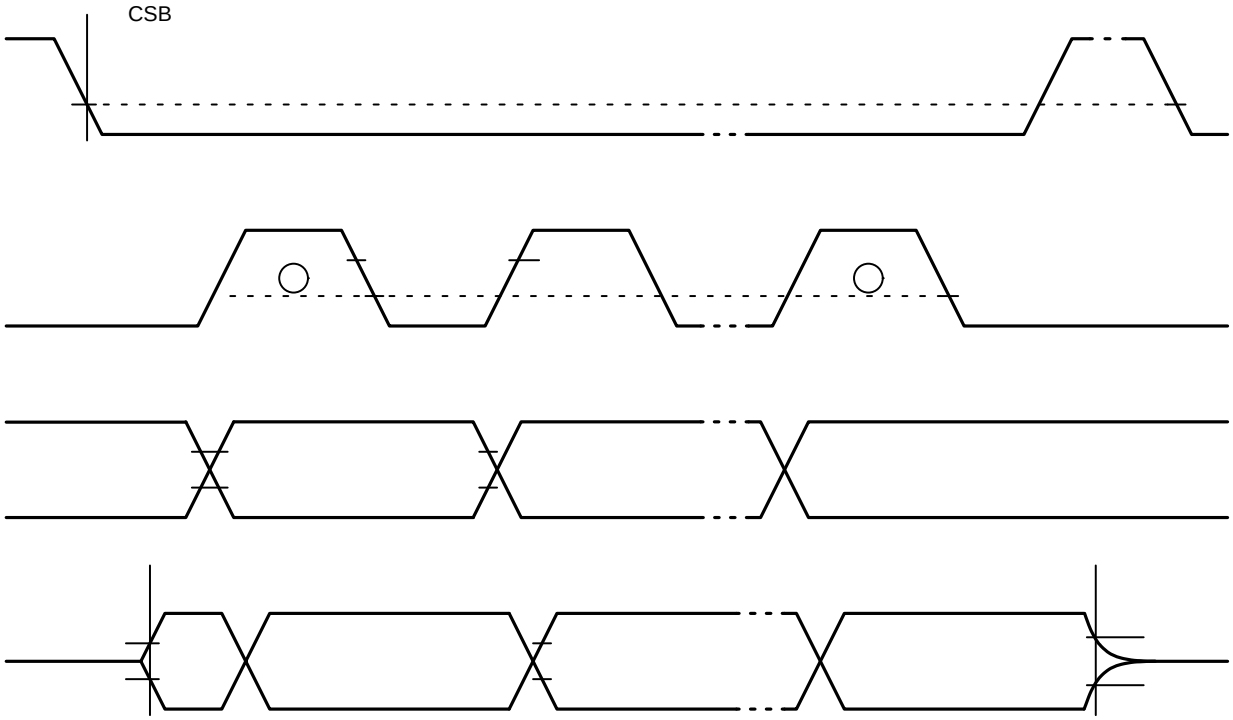


Figure 4. SPI Timing

DETAILED OPERATING DESCRIPTION

Power Supply

The power supply block provides:

- all internal supply and reference voltages;
- all internal bias and reference currents;
- VCC power−on reset (POR) and VS under/over−voltage lockout signals.

The analog and power portions of the device (reference voltages/currents,

- VS_{OVSDF} < VS < VS(CP_{OV}

SPI Interface

A full−duplex synchronous serial data transfer interface (SPI) is used to control the device and provide diagnosis during normal operation. Daisy chain capability of the interface is implemented in order to minimize circuit expenditure and communication efforts. The SPI protocol utilizes 16−bit data words (B15 = MSB). The idle state of SCLK is low and the SI data must be stable before the falling edge of SCLK (“legacy mode 1”: CPOL=0, CPHA=1).

The interface consists of 4 I/O lines with 5V CMOS logic levels and termination resistors (see Figure 7, Figure 2):

- the active−low CSB enables the SPI interface;
- the SCLK pin clocks the internal shift registers of the device;
- the SI pin receives data of the input shift registers MSB first;
- the SO pin sends data of the output shift registers MSB first.

The device offers the following SPI communication error checks in order to protect the application from unintended motor activation:

- protocol length error (modulo 16);
- no edges on SCLK during a CSB period;
- an undefined SPI command (not used bits must be set to logic 0);
- watchdog (WD) toggle (the internal watchdog bit (CRx.WD) must be toggled with each SPI message);
- WD timeout (the WD bit must be toggled before the internal watchdog timeout is reached).

An SI pin stuck−at condition during a CSB period is detected by a WD toggle error. A VCC under−voltage condition is directly blocking the complete SPI functionality via the VCC_{PORF} signal.

The length of the watchdog timeout is SPI programmable (see § *SPI Control Set* and § *Electrical Characteristics: Watchdog Timer*) in order to facilitate module boot loader programming. The timeout setting is controlled by the CR1.WD_CFG bit:

- when CR1.WD_CFG=0 (default setting) the WD timeout is t_{WD} = 25 ms;
- when CR1.WD_CFG=1 the WD timeout is t_{WD} = 500 ms.

The first WD bit value sent after VCC POR or wake−up must be WD = 0 in the first frame, then WD = 1 in the next.

A correct communication is reported when bit SR0.SPIF = 0 and the device is in **NORMAL MODE** (NM) when bit SRx.NM = 1. The device enters **FAILSAFE MODE** immediately in the event of an SPI communication error (see § *Operating Modes*).

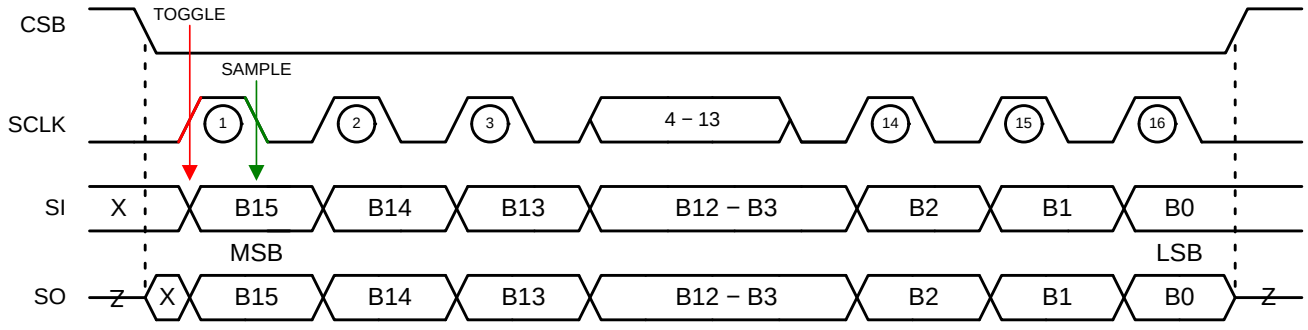
Serial Data and SPI Register Structures

The input and output message formats of the implemented SPI protocol are as shown in the following tables. In the descriptions in the following sections, it is implied that the frame length is correct and that the WD bit has been properly toggled when sending and receiving SPI messages. Please also note that the SPI hardware protocol is a “frame−behind” response type, i.e. the requested data is delivered in the next frame.

SPI Control Set

The first 4 bits (D15 ... D12) serve as address bits, while 12 bits (D11 ... D0) are used as data bits. The D11 bit is the WD toggle bit: A SPI fail is detected if the bit is not toggled within the WD timeout. The D10 bit may be used as an extended address in some messages.

All Control Register (CRx) bits are initialized to logic 0 after a reset. The predefined value is off / inactive unless otherwise noted. The SPI control set (input data map) and input data structure prototype are shown in the following tables.



Note: SPI Legacy Mode 1; X=Don’t Care, Z=Tri−State

Figure 7. SPI Communication Frame Format

Table 2. SPI INPUT DATA FORMAT

Command Input Message Format															
MSB															LSB
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
A3	A2	A1	A0	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
4−bit REGISTER ADDRESS				WATCH DOG	11−bit INPUT DATA										

Table 3. INPUT DATA STRUCTURE PROTOTYPE

Input Data Prototype												
CRx	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			?	?	?	?	?	?	?	?	?	?

Table 6. CR0 INSTRUCTION DEFINITIONS

Mnemonic	Value	Comment
SRA_MODE	0	The Status Register Address selected via CR0.SRA [2:0] will be used for a single read command. The address always points to SR0 after the read (default state).
	1	The Status Register Address selected via SRA [2:0] will be used for the next and all further read commands until a new address is selected.
SRA[2:0]	000	SR0 data is returned in the next frame (default state).
	001	SR1 data is returned in the next frame.
	010	SR2 data is returned in the next frame.
	011	SR3 data is returned in the next frame.
	100	SR4 data is returned in the next frame.
	101	SR5 data is returned in the next frame.
	110	SR6 data is returned in the next frame.
	111	SR7 data is returned in the next frame.
HB_ENx	0	HBx output disabled (default state).
	1	HBx output enabled.

Table 7. CR1: HBx MODE CONTROL REGISTER

CR1	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	WD	DRV_EN	CP_SW	WD_CFG	X	X	X	X	HB_MODE4 … HB_MODE1			

Table 8. CR1 INSTRUCTION DEFINITIONS

Mnemonic	Value	Comment
DRV_EN	0	Charge pump and gate drive currents are disabled (default state).
	1	Charge pump and gate drive currents are enabled.
CP_SW	0	Charge pump switched output is OFF: CPSW = Hi−Z (default state).
	1	Charge pump switched output is ON: CPSW = V(CP−VS).
WD_CFG	0	Watch dog timeout = 25 ms (default state).
	1	Watch dog timeout = 500 ms.
HB_MODEx	0	Low−side pre−driver active (default state).
	1	High−side pre−driver active.

Table 9. CR2: HBx PWM CONTROL REGISTER

CR2	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	WD	0	0	0	0	X	X	X	HB_PWM4 … HB_PWM1			

Table 10. CR2 INSTRUCTION DEFINITIONS

Mnemonic	Value	Comment
HB_PWMx	0	Output is in 100% ON mode (default).
	1	Output is in PWM mode.

Table 11. CR3: HBx PWM MODE CONTROL REGISTER

CR3	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	WD	X	X	X	X	PWM40	X	PWM30	X	PWM20	X	PWM10

Table 21. CR14: HBx PWM DE−GLITCH

CR14	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	WD	0	0	0	0	X	X	X	DGL4	DGL3	DGL2	DGL1

Table 22. CR14 INSTRUCTION DEFINITIONS

Mnemonic	Value	Comment
DGLx	0	Type 1 de−glitch: $t_{PWM\_DGL} = t_{BLANKx} + t_{PRCx} + t_{DLYx}$ (default).
	1	Type 2 de−glitch: $t_{PWM\_DGL} = t_{PRCx} + t_{DLYx}$

Table 23. CR15: TEST MODE REGISTER

CR15	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	WD	Factory Use Only										

SPI Diagnosis Set

The first 3 bits D[15:13] serve as address bits, while the 13 bits D[12:0] are used as data bits. Output data for “not used” register adresses is D[11:0] = 0. The address of the Status Register (SRx) accessed for status information to be retrieved via a subsequent SPI frame is selected by the control register bits CR0.SRA_MODE and CR0.SRA[2:0] (see Table 5, Table 6).

Two different reading modes are provided depending on the SRA_MODE bit:

- when CR0.SRA_MODE = 0, the SRx address selected via bits CR0.SRA[1:0] will be used for a single status read command and the SR address returns to SR0 (device status register, default state) after reading;
- when CR0.SRA_MODE = 1, the SRx address selected via bits CR0.SRA[1:0] will be used for the next and all further status read commands until a new address or mode is selected.

The default reading mode and address after VCC POR or wake−up is CR0.SRA_MODE = 0, CR0.SRA[1:0] = 00. All status diagnosis bits are initialized to logic 0 after a reset event and in normal operation except:

- the **NORMAL MODE** (NM) bit indicates **NORMAL MODE** when SRx.NM = 1;
- the Register Clear Flag (RCF) bit is set (SR0.RCF = 1) after a mode change to **NORMAL MODE** (see § *Operating Modes*).

The RCF bit indicates that all input and output registers were initialized; the bit is cleared after SR0 is read.

All status diagnosis bits are latched with the exception of the SR5.D[3:0] bits (see § *Output Status Monitoring*). To de−latch a diagnosis:

- the referring failure has to be removed;
- the referring failure bit has to be read by SPI diagnosis.

Refer to § *Protection and Diagnosis* to restart the outputs after a fault condition. The SPI diagnosis set (output data D0ta

Table 26. SPI OUTPUT REGISTER DEFINITIONS

Defined Status Output Registers (SRx)					
		D15	D14	D13	D12
Register Name	**Alias**	**A2**	**A1**	**A0**	**NM**
Device Status	SR0	0	0	0	NM
HB 1…4 Status Monitor	SR1	0	0	1	
Not Used	SR2	0	1	0	
HB 1…4 VDS Monitor	SR3	0	1	1	
HB 1…4 Calibration Result	SR4	1	0	0	
HB 1…4 Output Status	SR5	1	0	1	
Not Used	SR6	1	1	0	
Device ID/Test Mode	SR7	1	1	1	

Table 27. SR0: DEVICE STATUS REGISTER

[redacted]	NM	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SR0	NM	TM	RCF	FSM	SPIF	CPL	CPF	UVF	OVF	0			

Table 30. SR1 RESPONSE DEFINITIONS

Mnemonic	Value	Comment
SWHx	0	GHx output is “low” (default).
	1	GHx output is “high”.
SWLx	0	GLx output is “low” (default).
	1	

Table 35. SR5: HBx OUTPUT STATUS REGISTER

SR5	NM	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	NM	0	0	0	0	0	0	0	0	HB_OUT4 … HB_OUT1			

Table 36. SR5 RESPONSE DEFINITIONS

Mnemonic	Value	Comment
HB_OUTx	0	Output < VHB_{THR} (default).
	1	Output > $VHB_{THR.}$

Table 37. SR7: TEST MODE STATUS REGISTER − SR0.TM = 1: TEST MODE FORMAT

SR7	NM	D11	D10

Table 40. DEVICE REVISION LEVEL ENCODING

Silicon Revision		Mask Revision	
DEV_ID[5:3]	LEVEL	DEV_ID[2:0]	LEVEL
000	A	000	0
001	B	001	1
010	C	010	2
011	D	011	3
100	E	100	4
101	F	101	5
110	G	110	6
111	H	111	7

- when input PWMx=1, the driver defined by its HB_MODEx bit is turned ON (i.e. VGS ≈ V_{PDHX} or V_{PDLX}) and its complementary gate driver is turned OFF (i.e. VGS ≈ 0 V).

When multiple PWMx inputs are needed to be active, the scheduled PWM signals should be offset in time to avoid degradation of the VDS overload detection due to crosstalk (see § *Overload Protection*). The minimum offset should be based on the t_{PWM_DGL} times appropriate for the respective channels (see § *Switching Behavior of Half−bridge Drivers*, Figure 10 and Figure 11).

NOTE: The PWM source selection logic does not prevent more than one half−bridge output to be controlled by the same PWMx input.

Switching Behavior of Half−bridge Drivers

The external high−side NMOS switches are controlled with gate pre−charge and slew phases, while the external low−side switches are controlled via simple drive stages supplying a nominal 4x multiple of the selected high−side driver slew current (see Figure 9 and § *Electrical Characteristics: Pre−driver Slope Control)*. The timing for the gate drivers is provided by the digital logic, where the key parameters can be programmed via SPI in order to adapt different MOSFET types and application switching speeds.

Each individual half−bridge can be programmed via three configuration registers, e.g. CR5A and CR5B for HB1, and CR14 (see § *SPI Control Set*, Table 15 − Table 17 and Table 21, summarized in Table 43):

Table 43. HALF−BRIDGE CONFIGURATION REGISTERS

CR5A – CR8A	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	WD	0	BLANKx[1:0]		I_PCFx[2:0]			I_PCRx[2:0]			T_PCx[1:0]	

CR5B – CR8B	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	WD	1	VDSx[2:0]			T_DLY[3:0]				SR_CTRL[2:0]		

CR14	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	WD	0	0	0	0	XX						

In order to not overload the charge pump circuit in case of loss of VS or in case of a disconnected security switch, the steady state output current of the high−side gate drivers is limited to I_{GHX_SS} after $t_{TIMEOUT}$ (see I(GHx) in Figure 12 and § *Electrical Characteristics: Half−Bridge Pre−Driver Outputs*).

NOTE: Driver turn−ON/OFF via SPI (i.e. CR1.HB_MODEx bits) includes both the pre−charge and slew phases, but adapted de−glitch strategy is not applied.

When operating in PWM mode, type 1 de−glitch is selected when CR14.DGLx = 0 (see Figure 10) and the adapted time is given by:

$$t_{PWM\_DGL} \approx t_{BLANKX} + t_{PRCX} + t_{DLYX} \quad \text{(eq. 1)}$$

Type 2 de−glitch is selected when CR14.DGLx = 1 (see Figure 11) and the adapted time is given by:

$$t_{PWM\_DGL} \approx t_{PRCX} + t_{DLYX} \quad \text{(eq. 2)}$$

NOTE: To avoid synchronization issues, the de−glitch type must be selected before beginning PWM of a load.

Once a switching parameter set for EMC optimization and stable VDS overload detection has been chosen, the allowable duty ratio (D) is bounded by the selected adaptive de−glitch type and PWM frequency such that:

$$f_{PWM} \cdot t_{PWM_{DGL}} \cdot D \cdot 1 - f_{PWM} \cdot t_{PWM_{DGL}} \quad \text{(eq. 3)}$$

When operating in PWM mode, the timing of the gate drivers is according to Figure 12.

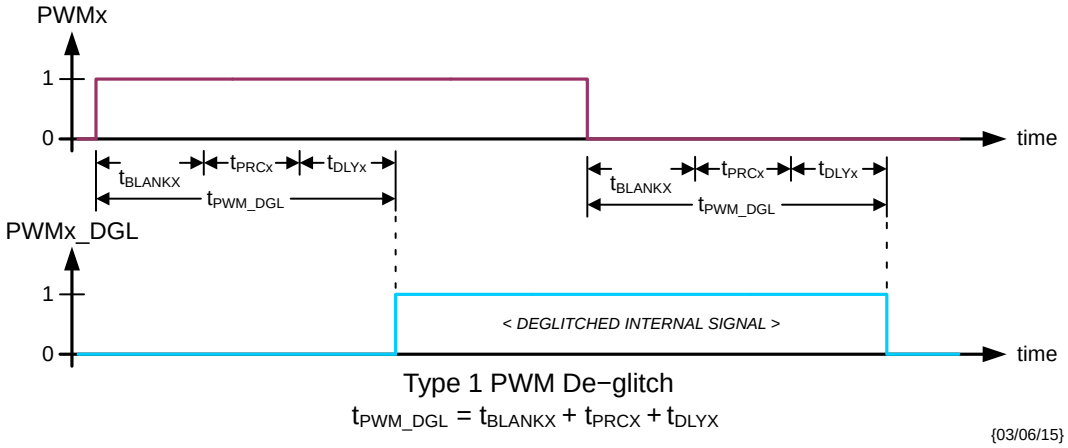


Figure 10. Type 1 PWMx Input De−glitch − CR14.DGLx = 0

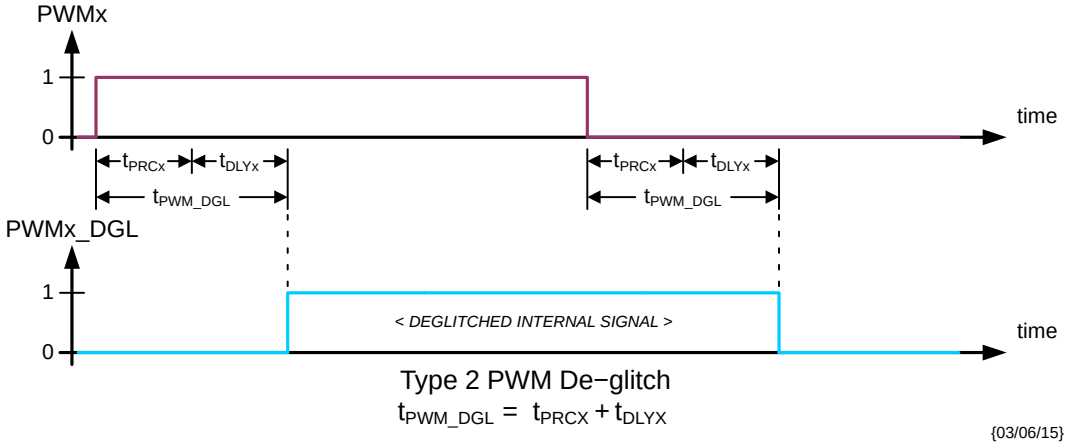


Figure 11. Type 2 PWMx Input De−glitch − CR14.DGLx = 1

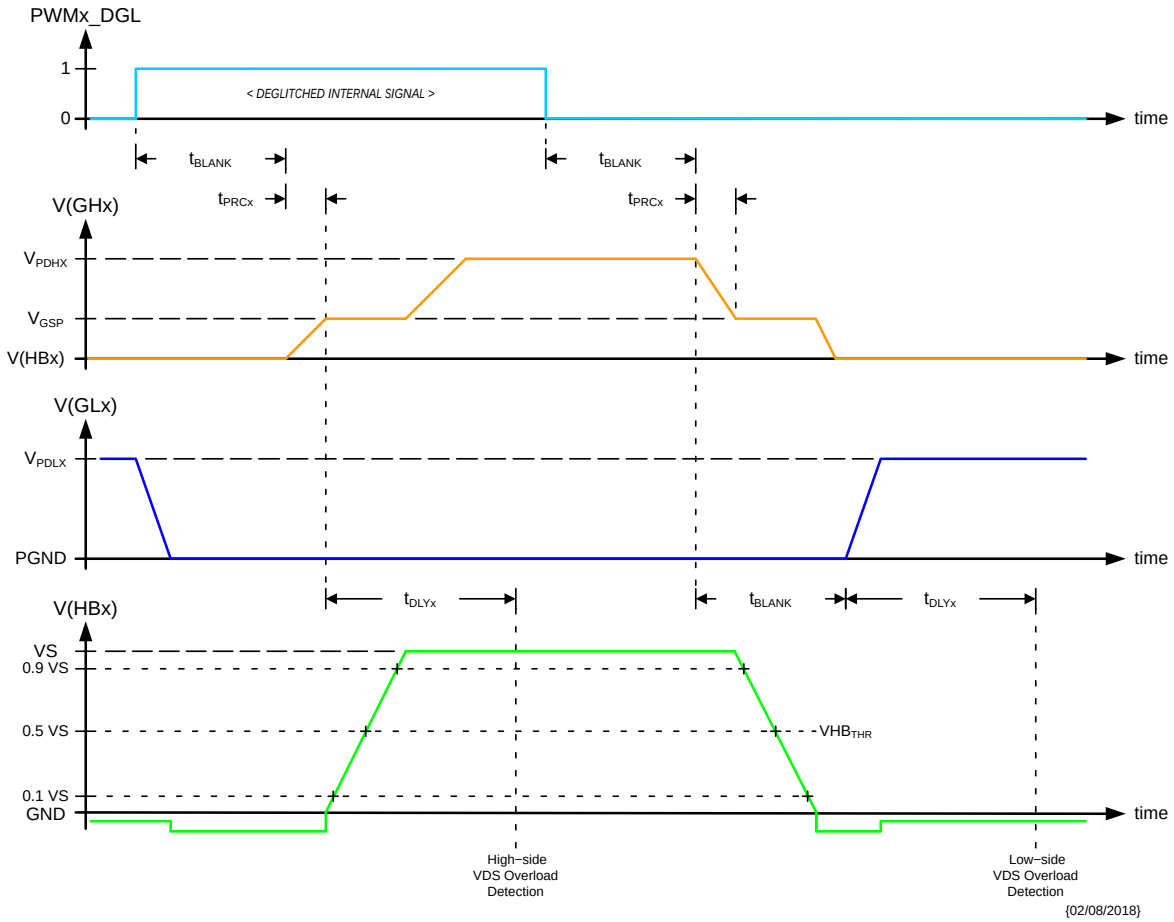


Figure 12. HBx Output Switching in Half−Bridge Configuration

In the pre−charge phase ($V_{GHX} < V_{GSP}$) the GHx output delivers the selected rise (I_{PRCX_R}) or fall (I_{PRCX_F}) current for the selected time (t_{PRCx}), and in the slew phase ($V_{GSP} \leq V_{GHX} \leq V_{PDHX}$) the GHx output delivers the selected current (I_{SRX}) for up to the gate drive timeout time ($t_{TIMEOUT}$). After $t_{TIMEOUT}$, the GHx output delivers the timeout current (I_{GHx_SS}). The GLx output always delivers a multiple (I_{LSX}) of the selected slew current (see Figure 9 and § *Electrical Characteristics: Half− Bridge Pre−Driver Outputs, Pre−driver Slope Control*).

Slope Control Calibration Unit

A slope control calibration unit is implemented in order to allow adjustments to a selected MOSFET's initial switching parameter set and to verify proper setting of the high−side gate drivers (GHx). The calibration assists optimizing EMC performance and alignment of the GHx switching slopes with the VDS overload detection delay time and threshold to assure stable behavior of the protection strategy (see § *Overload Protection*).

A calibration detection unit, consisting of 4 multiplexed high−speed comparators, samples the voltage at the desired HBx input at a selected calibration sample time (see t_{CAL_PCx}, t_{CAL_DLYx} in § *Electrical Characteristics: Slope Control Calibration Unit*). A complete calibration cycle consists of sampling both the rising and falling switching slopes, and the encoded calibration result is stored in the device's calibration register (SR4).

Calibration is enabled when the calibration register (CR4) is written (summary Table 44 − see also Table 13):

- the desired HBx input is selected by the CR4.CAL_SEL[2:0] bits where the resulting binary code refers directly to the selected half−bridge (e.g. 100 = HB4);
- the detection pre−charge and delay sample times (t_{CAL_PCx} and t_{CAL_DLYx}) for calibration of the desired input are selected individually by the CR4.CAL_PC[3:0] bits and by the CR4.CAL_DLY[3:0] bits for both the rising and falling slopes.

The calibration unit is turned off when CR4.CAL_SEL[2:0] = 000 (POR default) is selected (see also Table 14).

Detection is started with the next edge of a routed PWMx input signal (see § *Control of Half−bridge Drivers*) on the selected channel and detection is finished when both rising and falling edges are completed (see Figure 13). The detection results are stored in the calibration result register SR4 (summary Table 44 − see also Table 33):

The CAL_READY bit indicates that when:

- SR4.CAL_READY = 0, calibration has not been executed OR the calibration result has been read;
- SR4.CAL_READY = 1, successful detection was performed for both slopes AND a valid comparator output state is delivered.

As long as the CAL_READY bit is not set (≠ 1), the calibration of a particular slope for the selected channel may be repeated. Calibration may be terminated by sending CR4.CAL_SEL[2:0] = 000.

The calibration result is encoded in the SR4. CAL_PC_R[1:0] bits and the SR4.CAL_DLY_R[1:0] bits for the rising slope and in the SR4. CAL_PC_F[1:0] bits and the SR4.CAL_DLY_F[1:0] bits for the falling slope according to Table 45.

Table 44. HBx CALIBRATION CONTROL AND RESULT REGISTERS

CR4	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	WD	CAL_DLY[3:0]				CAL_PC[3:0]				CAL_SEL[2:0]		

SR4	NM	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	NM	0	0	0	CAL_READY	CAL_DLY_R[1:0]		CAL_PC_R[1:0]		CAL_DLY F[1:0]		CAL_PC _F[1:0]	

Table 45. CALIBRATION RESULT RELATIVE TO HBx SAMPLE TIME

Mnemonic	Value	Relative HBx Level Detected at Selected Sample Times	Comment
Start of Rising Slope			
CAL_PC_R[1:0]	00	VHBx < 5%	Pre−charge too low.
	01	5% < VHBx < 15%	Pre−charge within target.
	10	15% < VHBx < 85%	Pre−charge too high.
	11	VHBx > 85%	Pre−charge far too high.
End of Rising Slope			
CAL_DLY_R[1:0]	00	VHBx < 15%	Transition far too slow.
	01	15% < VHBx < 85%	Transition slightly too slow.
	10	85% < VHBx < 95 %	Gate drive setting correct.
	11	VHBx >95%	Transition too fast.
Start of Falling Slope			
CAL_PC _F[1:0]	00	VHBx > 95%	Pre−charge too low.
	01	95% > VHBx > 85%	Pre−charge within target.
	10	85% > VHBx > 15%	Pre−charge too high.
	11	VHBx < 15%	Pre−charge far too high.
End of Falling Slope			
CAL_DLY_F[1:0]	00	VHBx > 85%	Transition far too slow.
	01	85% > VHBx > 15%	Transition slightly too slow.
	10	15% > VHBx > 5%	Gate drive setting correct.
	11	VHBx < 5%	Transition too fast.

The temporal position (see Figure 13) of the target transition detection point (e.g. 10%, 90%) with respect to t_{CAL_PCx} or t_{CAL_DLYx} (or in normal operation, t_{DLYX}) of the channel selected for calibration is dependent upon:

- the PWMx_DGL resulting from the channel's operating configuration (see § *Switching Behavior of Half−bridge*

OVERLOAD PROTECTION

Static Overload Protection

A static VDS monitoring technique is used to protect the external MOS power switches in case of overload resulting from short circuit conditions applied after activation of the power switches (“short circuit 2” condition).

The thresholds of the VDS monitoring comparators (CMP1 and CMP4 in Figure 14) are SPI programmable (see § *Electrical Characteristics: Half−Bridge Diagnostics*) for each individual half−bridge via the VDSx[2:0] bits in the HBx configuration “B” registers (see Table 17, Table 18).

When a switch is in the ON−state ($t > t_{DLYx}$ after end of the pre−charge phase) and its drain−source voltage exceeds the programmed VDS threshold:

- the corresponding half−bridge’s GHx and GLx drivers are latched off immediately after a de−glitch time (see t_{DGL_STAT} in § *Electrical Characteristics: Half−Bridge Diagnostics*);
- the SR0.HB_QSB Quick Status Bits and the appropriate VDS_Hx or VDS_Lx bit is latched in the corresponding VDS monitor status register (see Table 31 and Table 32)

Please refer to § *Output Fault (Local) Protection* to restart the half−bridge drivers after a shutdown event.

NOTE: Additional protection via use of current sensing in the low−side path of the power MOSFETs (see Figure 2) may be necessary in order to avoid destruction due to soft short condition.

Dynamic Overload Protection

A dynamic switching slope monitoring technique is used to protect the external MOS power switches in case of overload resulting from short circuit conditions applied before or during activation of the power switches (“short circuit 1” condition).

The output voltage at the switching nodes (HBx) is monitored during each of the GHx and the GLx turn−on phases by a high speed comparator (< 100 ns propagation delay, CMP2 and CMP3 in Figure 14). A single detection delay time (t_{DLYX}) is used during switching of each of the high−side and the low−side external MOS. The detection delay at each input is selected individually by the T_DLY[3:0] bits in the HBx configuration “B” registers (see § *SPI Control Set*). The detection delay t_{DLYX} is chosen based on the value of t_{CAL_R} for the rising slope of the high−side MOS as determined from the calibration result (see CAL_DLYR[3:0] in § *Slope Control Calibration Unit*).

The appropriate latch is set (after the adapted t_{PWM_DGL} − see Figure 10 and Figure 11) at the start of the switch activation (see V(HBx) in Figure 12). In the case of the high−side MOS, the delay time t_{DLYX} is started at the end of the pre−charge time (t_{PRCX}). In the case of the low−side MOS, the delay time t_{DLYX} is started concurrent with the

HBx Diagnostic & Overload Protection

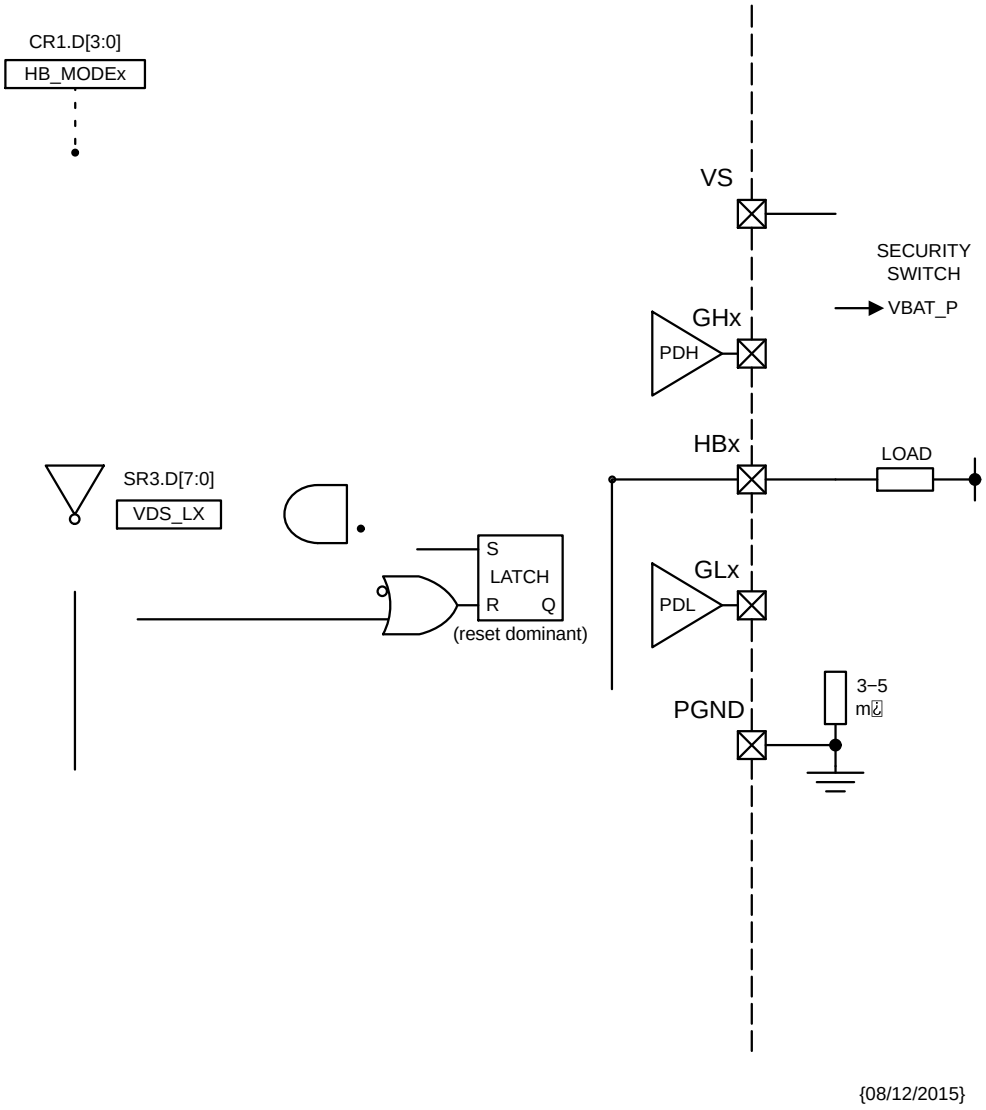


Figure 14. HBx Diagnostic and Overload Protection

The diagnostic consists of (see Figure 14 and Figure 15):

- a high−side and a low−side test current source at each odd−numbered HBx feedback input;
- a comparator (CMP5) at each HBx feedback input.

Provided the device is in **NORMAL MODE** (see § *Operating Modes*) and no global failure (see § *Device Fault (Global) Protection*) has been detected, the test current sources can be

- when the battery supply voltage VS is below the minimum supply voltage for a regulated charge pump voltage OR V(CP,VS) drops below the minimum output voltage CP_{LOW} this status is reported by the

FUNCTIONAL SAFETY SUPPORT STRATEGY

The device uses a closed−loop verification strategy in order to avoid mistreatment of the outputs and to support functional safety. The verification strategy is implemented based on the features in the following sections.

SPI Communication Monitoring

The SPI is protected against communication errors by use of the WD toggle bit and protocol check features (see § *SPI Interface*). In case of SPI communication error the device enters **FAILSAFE MODE** immediately (see § *Operating Modes*). A correct communication is reported in the NM bit (see § *SPI Diagnosis Set*).

Gate Driver Status Monitoring

The correct activation of the half−bridge drivers can be monitored by the microcontroller by means of SPI communication (see § *SPI Diagnosis Set*). The switching status of the output drivers is indicated by the SWLx and SWHx bits in the half− bridge status monitor register SR1. The bit value corresponds to the logic status of the driver. In PWM mode, both SWHx = 1 and SWLx = 1.

In case of a discrepancy between control data and status information from the device, the microcontroller has to drive the device into **FAILSAFE MODE** in order to avoid mistreatment of the motor drives, then transition the device to **NORMAL MODE** for reprogramming.

Output Status Monitoring

The status of the MOS switches and the motor connection lines can be monitored during **NORMAL MODE** by the microcontroller by means of the SPI communication (see Figure 14 and § *SPI Diagnosis Set*):

The output voltage levels of the half−bridge switches are monitored by the transparent VS/2 comparators. The comparator states are not latched and the current node states are indicated by the HB_OUTx bits in the SR5 half−bridge output status register. The controller can use the motor status information for correlation of the operating mode, OFF state diagnosis, or for controlled brake activation.

External Fail Mode Activation

The **FAILSAFE MODE** can be also activated by an external signal (e.g. watchdog circuitry) via the FSM input. In case of a malfunction of the microcontroller, an external watchdog can cause the device to enter **FAILSAFE MODE** (see § *Operating Modes*).

Failure of External Voltage Regulator

In case of breakdown of the external voltage regulator, the device and the application's VCC node may be protected against overload by use of an optional external voltage limiter circuit which must limit the voltage to VCC_{MAX} (see Figure 2 and § *MAXIMUM RATINGS*).

The SPI port's SO pin is protected against reverse biasing by use of a back−to−back switch. The reverse voltage for this condition is limited to V_SO_{MAX} (see § *MAXIMUM RATINGS*).