NCV7547

FLEXMOS™ 7x Half-bridge MOSFET Pre-driver

The NCV7547 programmable seven channel half−bridge MOSFET pre−driver is one of a family of FLEXMOS automotive grade products for driving logic−level NMOS FETs. The product is controllable by a combination of serial SPI and CMOS−compatible parallel inputs. An internal power−on reset provides controlled power up. A reset input allows external re−initialization and a failsafe input allows the device to be safely disabled in the event of system upset.

Each channel independently monitors its external MOSFETs' drain−source voltages for fault conditions. Overload detection thresholds are SPI−selectable and the product allows different detection thresholds for each channel.

The FLEXMOS family of products offers application scalability through choice of external MOSFETs.

Features

- Supports Functional Safety Compliance
- 7 Half−bridge Pre−drivers for External Logic−level NMOS FETs
  - One Channel with Separated High−side & Low−side Pre−drivers Configurable as a Half−bridge or as Independent Pre−drivers
- Integrated Charge Pump for:
  - High−side Gate Drive
  - Switched Reverse Battery Protection
- 5 V CMOS Compatible I/O:
  - 16−bit SPI Interface for Control and Diagnosis
  - Reset and Failsafe Inputs
  - 4 PWM Control Inputs
- Programmable:
  - Slew Rate Control
  - Overload Protection Thresholds
- Low Quiescent Current
- Wettable Flanks Pb−free Packaging
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

Benefits

- Scalable to Load by Choice of External MOSFET

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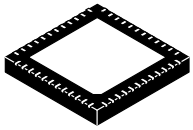
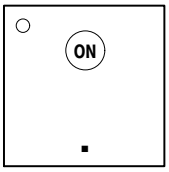


QFNW48
7x7, 0.5P
CASE 484AJ

MARKING DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping

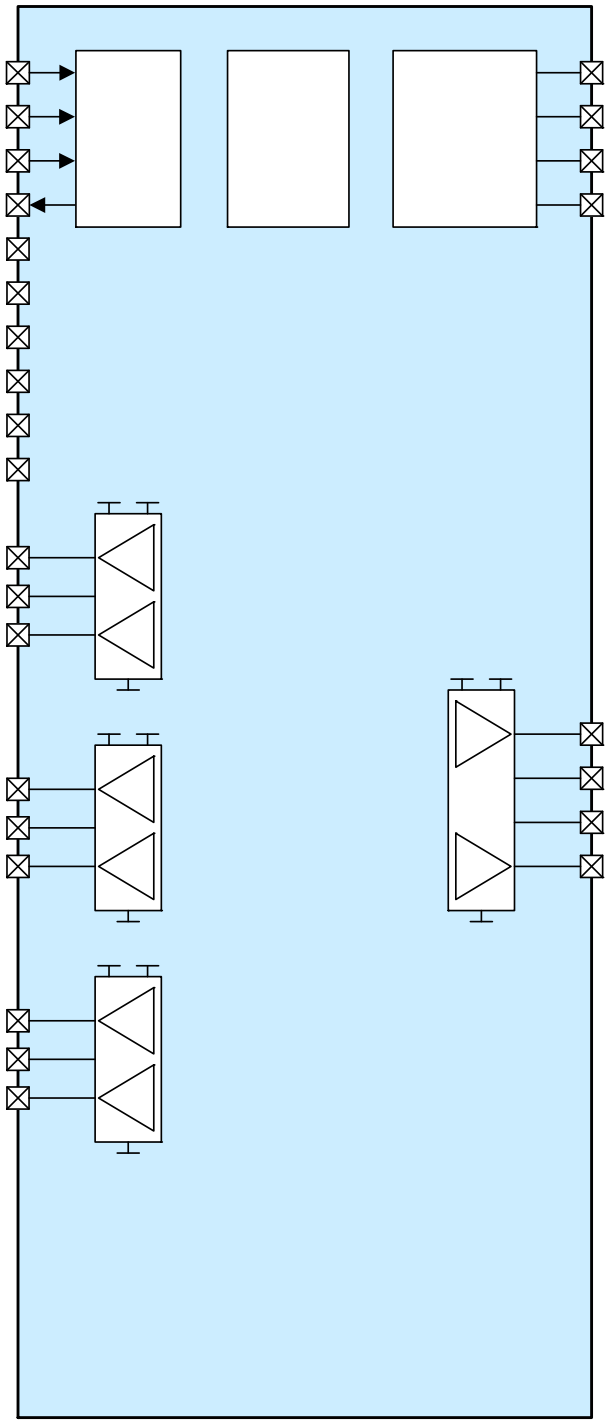


Figure 1. Block Diagram

Figure 2. Application Diagram

PACKAGE PIN DESCRIPTION

Pin	Label	Function	Description
48 PIN QFN EXPOSED PAD PACKAGE			
			– – –
			– – –

PACKAGE PIN DESCRIPTION

Pin	Label	Function	Description
48 PIN QFN EXPOSED PAD PACKAGE			
		– – – – –	

MAXIMUM RATINGS

Rating	Symbol	Value	Unit

ELECTRICAL CHARACTERISTICS

≤ ≤ ≤ ≤ – ° ≤ ≤ °

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
CHARGE PUMP						
		→				
						µ
		→				
–						
–						
		°				Ω
						Ω
			–			
DIGITAL I/O						
–						Ω
–						Ω
			–			µ
			–			µ
						µ
–		→ →				µ
		→				µ
–			–			µ

SERIAL PERIPHERAL INTERFACE (See Figure 4)

VCC = 5.0V, FSCLK = 2.5 MHz, CLOAD = 80 pF, all timing is at 30% and 70% VCC unless otherwise specified.						

ELECTRICAL CHARACTERISTICS

≤ ≤ ≤ ≤ – ° ≤ ≤ °

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
SERIAL PERIPHERAL INTERFACE (See Figure 4)						
		=				

ELECTRICAL CHARACTERISTICS

≤ ≤ ≤ ≤ – ° ≤ ≤ °

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
PRE–DRIVER SLOPE CONTROL						
– –						
–						
–						
SLOPE CONTROL CALIBRATION UNIT						

[redacted]

ELECTRICAL CHARACTERISTICS

≤ ≤ ≤ ≤ – ° ≤ ≤ °

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
SLOPE CONTROL CALIBRATION UNIT						
–						
						µ
HALF–BRIDGE DIAGNOSTICS						
– –						
						µ

± ± ±

ELECTRICAL CHARACTERISTICS

≤ ≤ ≤ ≤ – ° ≤ ≤ °

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
HALF–BRIDGE DIAGNOSTICS						
						µ
		– –	–		–	Ω

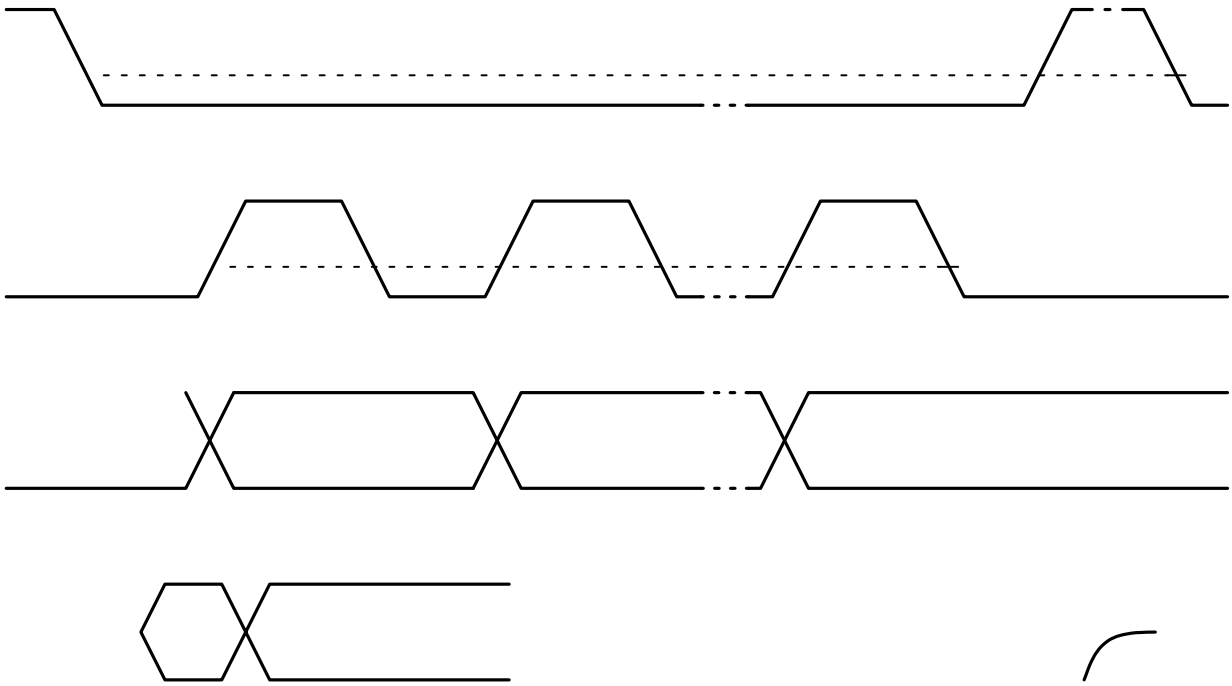


Figure 4. SPI Timing

DETAILED OPERATING DESCRIPTION

Power Supply

The power supply block provides:

- all internal supply and reference voltages;
- all internal bias and reference currents;
- VCC power−on reset (POR) and VS under/over−voltage lockout signals.

The analog and power portions of the device (reference voltages/currents, charge pump, low−side gate drivers, etc.) are supplied from the VS terminal. Each of the low−side gate driver outputs (GLx) is supplied from VS via an individual buffer (source follower) with voltage limit functionality. The high−side gate driver outputs (GHx) are supplied from a regulated charge pump.

The logic core and the SPI communication interface are supplied from the VCC terminal in order to achieve a high frequency operation by use of external bypass capacitors. In case of breakdown of the external voltage regulator, the device can be protected by use of an external voltage limiter, which must limit the maximum voltage at the VCC terminal to VCC_{MAX} (see § *MAXIMUM RATINGS*).

The outputs are disabled during device initialization at power−up via an interlock between VS and VCC and such that no control is available until after VCC > VCC_{PORR} (see § *Electrical Characteristics: VCC Supply*). Reverse battery protection for VS and the VCC regulator is provided externally by the application (see Figure 2).

- VS_{OVSDF} < VS < VS(CP_{OV})
  the charge pump including the CPSW output is functional, but the GHx outputs are shut down;
- VS > VS(CP_{OV})
  the charge pump is disabled and the charge pump buffer capacitor is discharged to VS in order to protect the device from destruction.

In the case of VS overvoltage, the charge pump automatically resumes normal operation when the VS voltage returns to below $CP_{OV} - CP_{OV\_HYS}$. In the case of VS < VS_{PWM} or V(CP, VS) < CP_{LOW} it should be considered for the microcontroller to adopt a PWM duty ratio management schema in order to minimize charge pump loading while ensuring smooth motor operation.

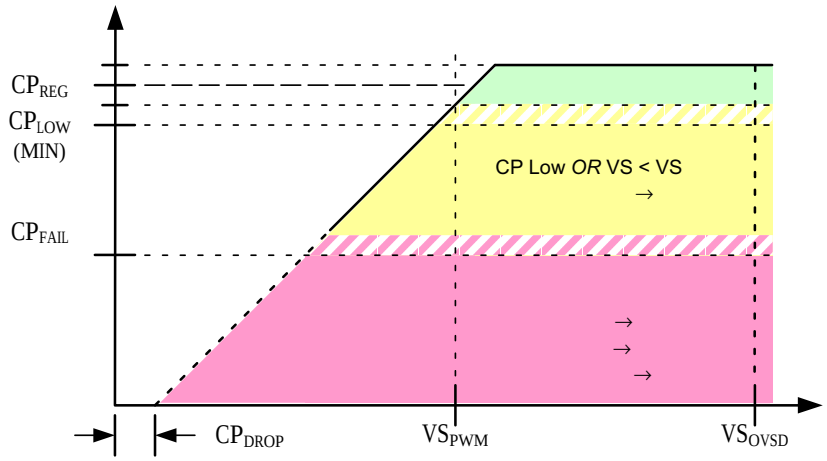


Figure 5. Charge Pump Characteristics

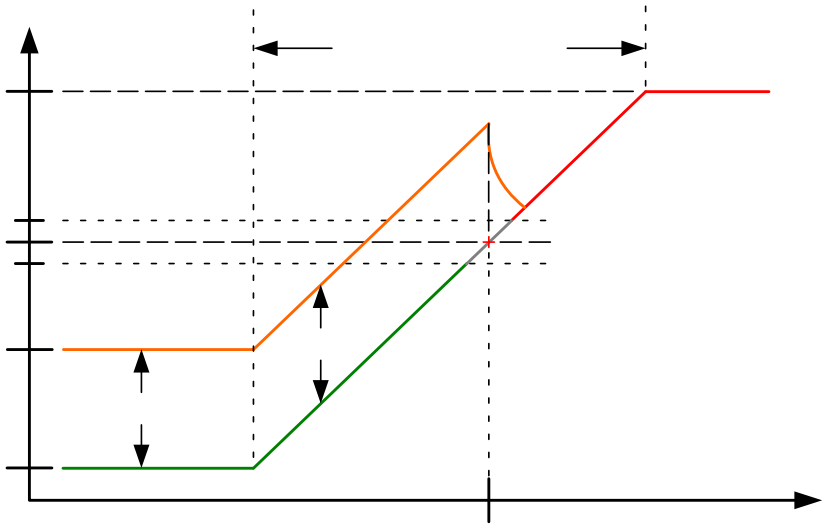


Figure 6. Charge Pump Overvoltage Behavior

SPI Interface

A full−duplex synchronous serial data transfer interface (SPI) is used to control the device and provide diagnosis during normal operation. Daisy chain capability of the interface is implemented in order to minimize circuit expenditure and communication efforts. The SPI protocol utilizes 16−bit data words (B15 = MSB). The idle state of SCLK is

Table 2. SPI INPUT DATA FORMAT

Command Input Message Format															
–					–										

Table 3. INPUT DATA STRUCTURE PROTOTYPE

Input Data Prototype												

Table 4. SPI INPUT REGISTER DEFINITIONS

Defined Command Input Registers (CRx)							
Register Name	Alias	A3	A2	A1	A0		D10

Table 6. CR0 INSTRUCTION DEFINITIONS

Mnemonic	Value

Table 12. CR3 INSTRUCTION DEFINITIONS

Mnemonic	Value	Comment

Table 13. CR4: HBx CALIBRATION CONTROL REGISTER

Table 14. CR4 INSTRUCTION DEFINITIONS

Mnemonic	Value	Comment
		µ
		µ
		µ
		µ
		µ

Table 14. CR4 INSTRUCTION DEFINITIONS

Mnemonic	Value	Comment

Table 15. CR5A – CR11A: HBx CONFIGURATION A REGISTER

Table 18. CR5B – CR11B INSTRUCTION DEFINITIONS

Mnemonic	Value	Comment
		µ
		µ
		µ
		µ
		µ
		µ
		µ
		µ
		µ
		µ
		µ
		µ
		µ
		µ
		µ

Table 19. CR12: HBx DIAGNOSIS CONTROL REGISTER

Table 20. CR12 INSTRUCTION DEFINITIONS

Mnemonic	Value	Comment
		–
		–
		–
		–

Table 21. CR14: HBx PWM DE−GLITCH

Table 22. CR14 INSTRUCTION DEFINITIONS

Mnemonic	Value	Comment
		−
		−

Table 23. CR15: TEST MODE REGISTER

SPI Diagnosis Set

The first 3 bits D[15:13] serve as address bits, while the 13 bits D[12:0] are used as data bits. Output data for “not used” register adresses is D[11:0] = 0. The address of the Status Register (SRx) accessed for status information to be retrieved via a subsequent SPI frame is selected by the control register bits CR0.SRA_MODE and CR0.SRA[2:0] (see Table 5, Table 6).

Two different reading modes are provided depending on the SRA_MODE bit:

- when CR0.SRA_MODE = 0, the SRx address selected via bits CR0.SRA[2:0] will be used for a single status read command and the SR address returns to SR0 (device status register, default state) after reading;
- when CR0.SRA_MODE = 1, the SRx address selected via bits CR0.SRA[2:0] will be used for the next and all further status read commands until a new address or mode is selected.

The default reading mode and address after VCC POR or wake−up is CR0.SRA_MODE = 0, CR0.SRA[2:0] = 00.

All status diagnosis bits are initialized to logic 0 after a reset event and in normal operation except:

- the **NORMAL MODE** (NM) bit indicates **NORMAL MODE** when SRx.NM = 1;
- the Register Clear Flag (RCF) bit is set (SR0.RCF = 1) after a mode change to **NORMAL MODE** (see § *Operating Modes*).

The RCF bit indicates that all input and output registers were initialized; the bit is cleared after SR0 is read.

All status diagnosis bits are latched with the exception of the SR5.D[3:0] bits (see § *Output Status Monitoring*). To de−latch a diagnosis:

- the referring failure has to be removed;
- the referring failure bit has to be read by SPI diagnosis.

Refer to § *Protection and Diagnosis* to restart the outputs after a fault condition. The SPI diagnosis set (output data map) and output data structure prototype are shown in the following tables.

Table 24. SPI OUTPUT DATA FORMAT

Status Output Message Format															
−				−											

Table 25. OUTPUT DATA STRUCTURE PROTOTYPE

Output Data Prototype													

Table 26. SPI OUTPUT REGISTER DEFINITIONS

Defined Status Output Registers (SRx)					
Register Name	**Alias**	**A2**	**A1**	**A0**	**NM**
…6					
…6					
…					

Table 27. SR0: DEVICE STATUS REGISTER

Table 28. SR0 RESPONSE DEFINITIONS

Mnemonic	Value	Comment
		−OR−
		– –
		– –

Table 29. SR1: HBx STATUS MONITOR REGISTER

Table 30. SR1 RESPONSE DEFINITIONS

Mnemonic	Value	Comment

Table 31. SR2: HB 7 STATUS & VDS MONITOR REGISTER

Table 32. SR2 RESPONSE DEFINITIONS

Mnemonic	Value	Comment
		–
		–
		–
		–

Table 33. SR3: HBx VDS MONITOR REGISTER

Table 34. SR3 RESPONSE DEFINITIONS

Mnemonic

Table 36. SR4 RESPONSE DEFINITIONS

When not in test mode (SR0.TM = 0), a status request via CR0.D[10:7] returns SR7.D[11:0] = DEV_ID[11:0] as defined in Table 41. The default content of SR7 after VCC POR or wake−up is SR7.D[11:0] = 0.

The DEV_ID[5:0] revision value may be changed based on whether the entire die (silicon) or intermediate layer (mask) is affected. The revisions can be e.g. classified accordingly:

- silicon revision: defined area changed (isolation pocket or other boundary, bond pad etc. changed/moved) or digital core changed (isolation pocket changed or unchanged);
- mask revision: interconnect changed (metal and/or polysilicon/contact/via).

The mask revision value is set to DEV_ID[2:0] = 000 whenever the die revision is incremented. Table 42 shows how the value encoding scheme is used to indicate the device revision level.

Table 42. DEVICE REVISION LEVEL ENCODING

Silicon Revision		Mask Revision	

Half−bridge Gate Drivers

The half−bridge drivers are used to control the gates of external logic−level NMOS power switches. Drivers HB1 … HB6 are dedicated to e.g. motor control – the switches are normally connected in half−bridge configuration. HB7 is dedicated to e.g. heater control – the switches are normally connected independently in a split configuration but may be optionally connected in a half−bridge configuration (see Figure 2). The device is initialized at power−up into a reduced power state (CR1.DRV_EN = 0, see Table 7, Table 8):

- the charge pump is disabled;
- all gate drive currents are disabled.
- HBx diagnostic test currents are available (see § *Monitoring of Half−bridge Drivers in OFF−state*).

The device is placed into a full power state when CR1.DRV_EN = 1. The half−bridges are held in high−impedance state (external NMOS are off) via gate pull−down structures which are activated during power−up, while in reduced power state, or when in sleep mode.

Control of Half−bridge Drivers

The operation of the drivers is controlled by SPI configuration individually for each driver. All half−bridges can be operated in 100% “ON” mode as well as in PWM mode.

The control schema for HB1 … HB7 in half−bridge configuration and for HB7 in split configuration is shown in Table 44 (see also § *SPI Control Set*).

The CR0.HB_ENx bits are used to enable the operation of the selected half−bridges and to re−start the drivers after a fault condition:

- when CR0.HB_ENx=0, the GHx and GLx outputs are disabled (i.e. VGS ≈ 0 V);
- when CR0.HB_ENx=1, the GHx and GLx outputs are enabled.

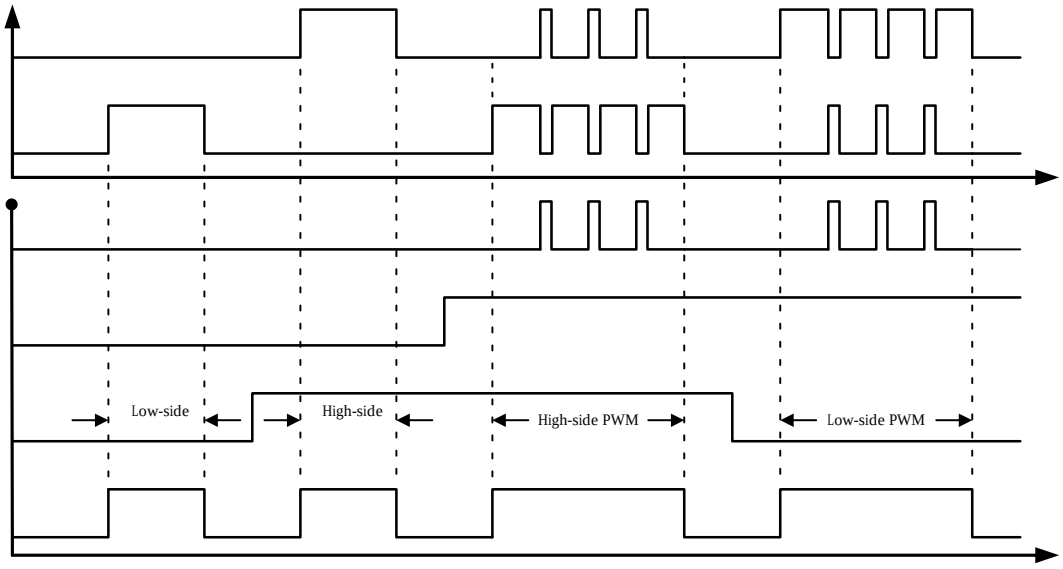
The CR1.HB_CFG7 bit is used to enable the split configuration of half−bridge HB7:

- when CR1.HB_CFG7=0, HB7 is in operating in half−bridge configuration;
- when CR1.HB_CFG7=1, HB7 is in operating in split configuration.

NOTE: When operating HB7 in split configuration, both the high−side and low−side switches are in ON−state simultaneously. Therefore the CR1.HB_CFG7 bit should only be set to ‘1’ when the application hardware is configured correctly. In case of erratic hardware configuration, VDS overload monitoring protects the external power switches.

The CR1.HB_MODEx bits are used to control the polarity of the selected half−bridge:

- when CR1.HB_MODEx=0, the low−side driver (PDL) is in an ON state (i.e. GLx = VGS ≈ V_{PDLX}, see § *Electrical Characteristics: Half−Bridge Pre−Driver Outputs*);
- when CR1.HB_MODEx=1, the high−side driver (PDH) is in an ON state (i.e. GHx = VGS ≈ V_{PDHX}, see § *Electrical Characteristics: Half−Bridge Pre−Driver Outputs*).



Note 1. GLx and GHx are for the same HBx output control (e.g. HB1: GL1, GH1).
Note 2. GLx and GHx time offset from PWMx via adaptive PWM input de-glitch not shown.

Figure 8. Gate Drive Operation in PWM Mode

For each individual half−bridge:

- cross−conduction blanking time is selected via the BLANKx[1:0] bits;
- pre−charge current is selected via the I_PCRx[2:0] bits for the rising slope and via the I_PCFx[2:0] bits for the falling slope;
- pre−charge time for both slopes is selected via the T_PCx[1:0] bits;
- slew current for both slopes is selected via the SR_CTRLx[2:0] bits – this parameter controls the external NMOS switches' rise/fall times to adopt proper EMC performance and minimize switching losses;
- VDS overload detection delay is selected via the T_DLYx[3:0] bits – this parameter controls when the VDS overload detection is performed (see § *Overload Protection*);
- VDS overload detection threshold is selected via the VDSx[2:0] bits – this parameter controls the VDS monitoring comparator threshold (see Table 17, Table 18);
- adaptive PWM input de−glitch construction when in half−bridge configuration is selected by DGLx[6:0] bits (see Figure 10, Figure 11, Table 21 and Table 22).

Please refer to § *Electrical Characteristics* for defined blanking (t_{BLANKX}), pre−charge (t_{PRCX}, I_{PRCX_R}, I_{PRCX_F}), slew (I_{SRX}), delay (t_{DLYX}) and VDS threshold (VDS_{THRX}) parametric values.

NOTE: A proper initial switching parameter set (e.g. VDS_{THRX}, t_{PRCX}, I_{PRCX_R}, $I_{SRX,}$ I_{PRCX_F}) for a chosen MOSFET has to be evaluated for a desired switching speed (see also § *Overload Protection*).

When operated in PWM mode, the PWMx input signals are each provided with a symmetrical de−glitch within a half− bridge's control logic. The de−glitch time (t_{PWM_DGL}) is adapted to the SPI settings t_{BLANKX}, t_{PRCX}, t_{DLYX} and DGLx as selected for each channel (see § *Electrical Characteristics: Half−Bridge Pre−Driver Outputs & Pre−driver Slope Control*).

The adapted t_{PWM_DGL} avoids mistreatment of the half−bridge drivers by ensuring that a complete turn−on or turn−off sequence is executed (erratic pulse widths are thereby avoided) and assures correct operation of the VDS overload protection (see § *Overload Protection).*

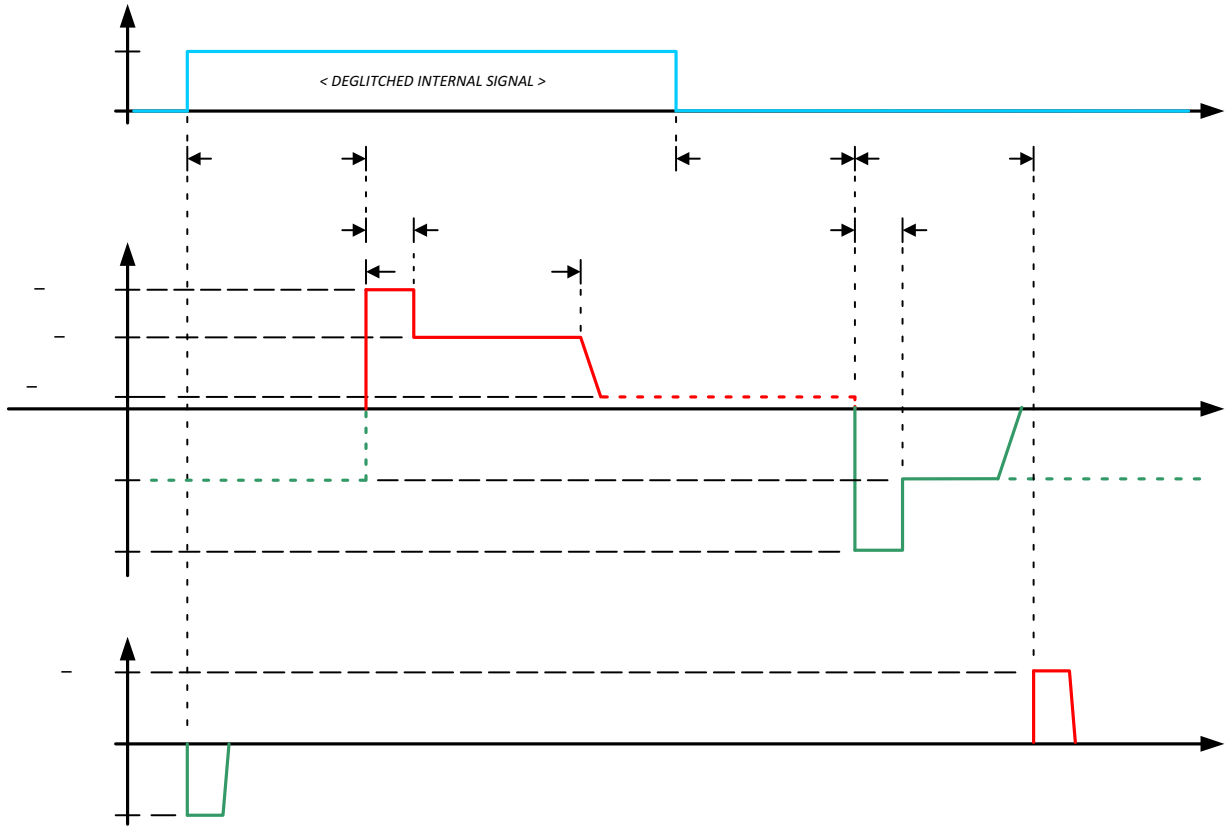


Figure 9. Gate Drive Current Evolution

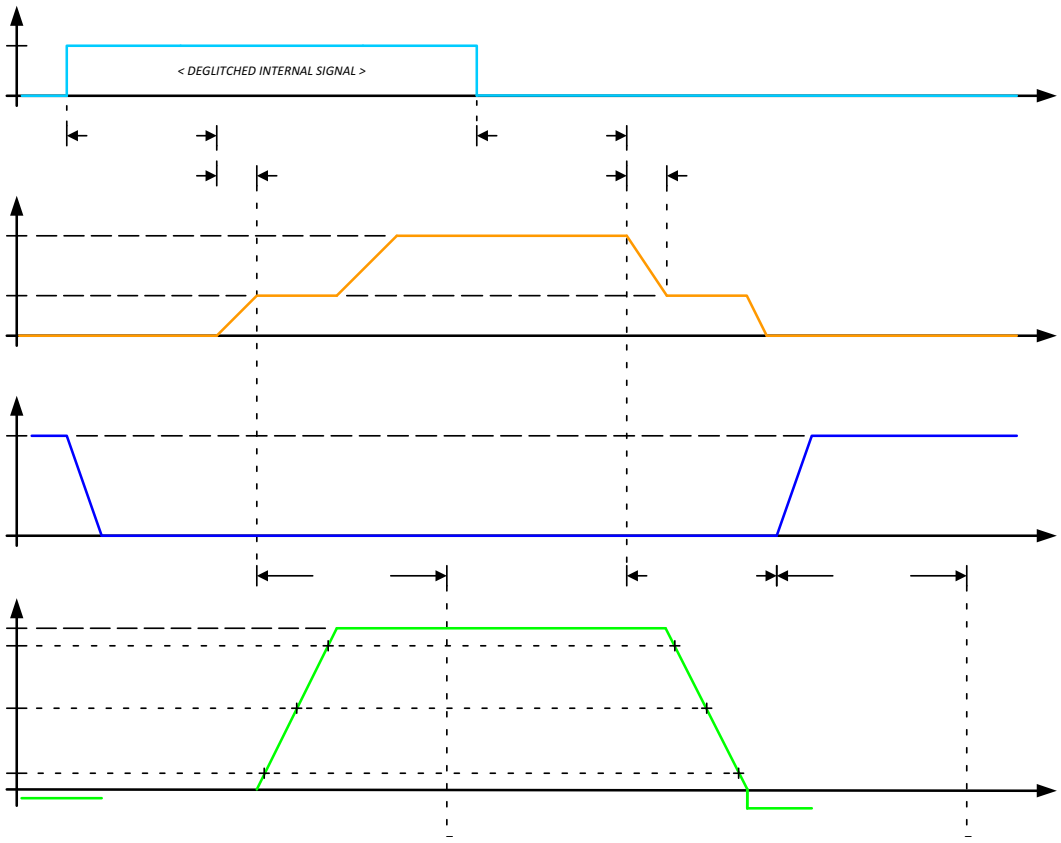


Figure 12. HBx Output Switching in Half−Bridge Configuration

Figure 13. HB7 Output Switching in Split Configuration

Calibration is enabled when the

The temporal position (see Figure 13) of the target transition detection point (e.g. 10%, 90%) with respect to t_{CAL_PCx} or t_{CAL_DLYx} (or in normal operation, t_{DLYX}) of the channel selected for calibration is dependent upon:

- the PWMx_DGL resulting from the channel's operating configuration (see § *Switching Behavior of Half−bridge Drivers*, Figure 10 and Figure 11);
- the t_{BLANKX} cross−conduction blank time setting as applicable;
- the t_{PRCX}, I_{PRCX_R} and I_{PRCX_F} pre−charge phase time and current settings;
- the I_{SRX} slew phase current setting.

Calibration may be performed at the application level during module end−of−line (EOL) test where the (adjusted) settings may be stored in a microcontroller's EEPROM. In order to maintain stable function and proper EMC performance with temperature drift and output load variations, the calibration can be verified/updated on a sample basis during normal application operation.

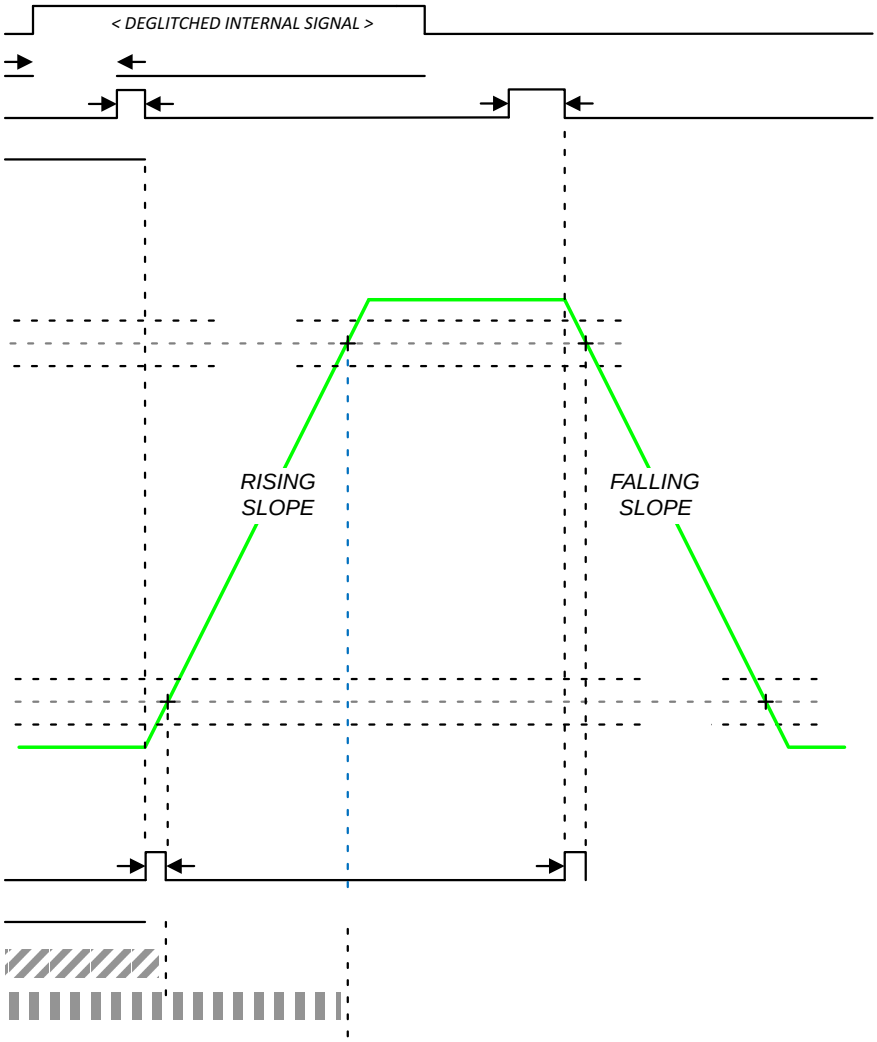


Figure 14. HBx Slope Control Calibration

The diagnostic consists of (see Figure 14 and Figure 15):

- a high−side and a low−side test current source at each odd−numbered HBx feedback input;
- a comparator (CMP5) at each HBx feedback input.

Provided the device is in **NORMAL MODE** (see § *Operating Modes*) and no global failure (see § *Device Fault (Global) Protection*) has been detected, the test current sources can be activated individually by the TST_HSx and TST_LSx bits in the HB diagnosis register (CR12.D[5:0] − see Table 19, Table 20). Active pull−down current sources are disabled in

- when the battery supply voltage VS is below the minimum supply voltage for a regulated charge pump voltage OR V(CP,VS) drops below the minimum output voltage CP_{LOW} this status is reported by the SR0.CPL bit in the device status register immediately after a de−glitch time t_{CPL_DGL} (see Table 27, Table 28). During this condition it should be considered for the microcontroller to adopt a PWM duty ratio management schema in order to minimize charge pump loading while ensuring smooth motor operation.
- when the charge pump output voltage V(CP, VS) drops below the charge pump fail threshold CP_{FAIL}, the half bridge high−side and low−side gate drivers are latched off immediately after a de−glitch time t_{CPF_DGL} and the status is reported by the SR0.CPF bit in the device status register (see Table 27, Table 28).
- when the battery supply voltage VS is in the nominal operation range $VS_{PWM} < VS < VS_{OVSDR}$ the full PWM operation of the GHx and GLx outputs is allowed;
- when the battery supply voltage is in over−voltage condition $VS > VS_{OVSDR}$, the SR0.CPF bit is masked;
- when the battery supply voltage is in over−voltage condition $VS_{OVSDF} < VS < CP_{OV}$ the charge pump − including the CPSW output − is functional but the GHx outputs are shut down;
- when the battery supply voltage exceeds the maximum supply voltage for the charge pump $VS > CP_{OV}$ the charge pump is disabled and the charge pump buffer capacitor is discharged to VS in order to protect the device from destruction.

Please refer to § *Device Fault (Global) Protection* to restart the outputs after a shutdown event.

Over−voltage Condition

During VS over−voltage, the behavior of the gate drivers (GHx and GLx) depends on the programmed operation mode:

- the high side gate drivers (GHx) are latched off immediately after de−glitch time t_{OVDGL} (see § *Electrical Characteristics: VS Supply*) in order to protect the application from over load condition; while the low−side gate driver outputs (GLx) are operable in order to provide controlled braking (e.g. for lift gate motors);
- GH_X pull−down current is reduced to 1 mA typ.(register contents are not changed − the current will revert to its prior value after VS over−voltage is resolved);
- the HBx test currents (see § *OFF−state Monitoring of Half−bridge Drivers*) are disabled immediately.

The VS over−voltage condition is reported by the SR0.OVF bit in the device status register (see Table 27, Table 28). When the battery supply voltage is in over−voltage condition $VS > VS_{OVSDR}$ the SR0.CPF bit is masked. Please refer to § *Device Fault (Global) Protection* to restart the outputs after a shutdown event.

A VCC overvoltage condition can occur during breakdown of the external voltage regulator. Please refer to § *Failure of External Voltage Regulator* for details.

Under Voltage Condition

In case of VS under voltage condition:

- all outputs (GHx, GLx) are disabled immediately after the de−glitch time t_{UVDGL} and the condition is reported by the SR0.UVF bit in the device status register (see Table 27, Table 28);
- the charge pump circuit and the switched charge pump output (CPSW) are still functional in order to keep the optional reverse battery and security switches active.

Please refer to § *Device Fault (Global) Protection* to restart the outputs after a shutdown event.

In case of VCC under voltage condition (power−on reset condition, $VCC < VCC_{POR}$):

- the device enters **SLEEP MODE** immediately without de−glitch time;
- logic input pull−up/down resistors, GHx & GLx output pull−down resistors, and VCC under voltage lockout assure safe operating states for all outputs.

To restart the device after this condition a wake−up sequence is necessary (see § *Operating Modes*).

Logic I/O Plausibility Check

The logic I/O pins are protected against mistreatment by input de−glitch circuits. The de−glitch circuits are implemented digitally, refer to § *Electrical Characteristics: Digital I/O for values*.

FUNCTIONAL SAFETY SUPPORT STRATEGY

The device uses a closed−loop verification strategy in order to avoid mistreatment of the outputs and to support functional safety. The verification strategy is implemented based on the features in the following sections.

SPI Communication Monitoring

The SPI is protected against communication errors by use of the WD toggle bit and protocol check features (see § *SPI Interface*). In case of SPI communication error the device enters **FAILSAFE MODE** immediately (see § *Operating Modes*). A correct communication is reported in the NM bit (see § *SPI Diagnosis Set*).

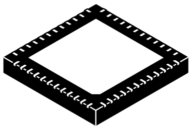
Gate Driver Status Monitoring

The correct activation of the half−bridge drivers can be monitored by the microcontroller by means of SPI communication (see § *SPI Diagnosis Set*). The switching status of the output drivers is indicated by the SWLx and SWHx bits in the half− bridge status monitor register SR1. The bit value corresponds to the logic status of the driver. In PWM mode, both SWHx = 1 and SWLx = 1.

In case of a discrepancy between control data and status information from the device, the microcontroller has to drive the device into **FAILSAFE MODE** in order to avoid mistreatment of the motor drives, then transition the device to **NORMAL MODE** for reprogramming.

Output Status Monitoring

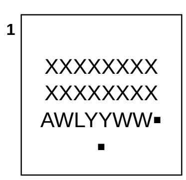
The status of the MOS switches and the motor connection lines can be monitored during **NORMAL MODE**



SCALE 2:1

= 0008019 0 .028 0 c 6.5949 Tm(1c-000289.86 c.8 l-1.284 9J/TT3 1 2..928 1.14

GENERIC
MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package