# FLEXMOS<sup>™</sup> 7x Half-bridge MOSFET Pre-driver

The NCV7547 programmable seven channel half-bridge MOSFET pre-driver is one of a family of FLEXMOS automotive grade products for driving logic-level NMOS FETs. The product is controllable by a combination of serial SPI and CMOS-compatible parallel inputs. An internal power-on reset provides controlled power up. A reset input allows external re-initialization and a failsafe input allows the device to be safely disabled in the event of system upset.

Each channel independently monitors its external MOSFETs' drain-source voltages for fault conditions. Overload detection thresholds are SPI-selectable and the product allows different detection thresholds for each channel.

The FLEXMOS family of products offers application scalability through choice of external MOSFETs.

#### Features

- Supports Functional Safety Compliance
- 7 Half-bridge Pre-drivers for External Logic-level NMOS FETs
  - One Channel with Separated High-side & Low-side Pre-drivers Configurable as a Half-bridge or as Independent Pre-drivers
- Integrated Charge Pump for:
  - ♦ High-side Gate Drive
  - Switched Reverse Battery Protection
- 5 V CMOS Compatible I/O:
  - 16-bit SPI Interface for Control and Diagnosis
  - Reset and Failsafe Inputs
  - 4 PWM Control Inputs
- Programmable:
  - ♦ Slew Rate Control
  - Overload Protection Thresholds
- Low Quiescent Current
- Wettable Flanks Pb-free Packaging
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable

#### Benefits

• Scalable to Load by Choice of External MOSFET





QFNW48 7x7, 0.5P CASE 484AJ





#### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NCV7547MWTXG	QFN-48 (Pb-Free)	2500 / Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1





Figure 2. Application Diagram

#### PACKAGE PIN DESCRIPTION

Pin	Label	Function	Description					
48 PII	8 PIN QFN EXPOSED PAD PACKAGE							
42	VS	Main Power Supply	Main high-power device supply (battery) input; VDS sense reference node for the half- bridge high-side drivers. An external ceramic bypass capacitor shall be connected be- tween VS and GND close to the pin.					
36	VCC	Logic Supply	SPI block and internal logic and low power (analog) supply input. An external ceramic bypass capacitor shall be connected between VCC and GND close to the pin.					
24	AGND	Signal Ground	Low power return path; reference for the analog circuitry.					
25	DGND	Digital Ground	Low power return path; reference for the digital circuitry.					
13	PGND	Power Ground	High power return path; reference for the half–bridge drivers; VDS sense reference node for the half–bridge low–side drivers.					
45	C1A	Charge Pump	Switching nodes for external ceramic charge pumping capacitors 1 & 2.					
46	C1B	Switch Node						
47	C2A							
48	C2B							
43	СР	Charge Pump Output	Charge pump output; an external ceramic buffer capacitor shall be connected between CP and VS to provide stable output voltage during transient noise on VS.					
44	CPSW	Charge Pump						

#### PACKAGE PIN DESCRIPTION

Pin	Label	Function	Description
48 PI	N QFN EXPOSE	D PAD PACKAGE	
1	GL1	Low–side Pre–driver Output	Low-side pre-drivers with pull-down resistor to PGND; gatATT2 1 Tf2 -1.1055 TD0f>Tj/TT2 1 Tf.58<00ef>expm

MAXIMUM RATINGS	(Except as noted,	voltages are with res	spect to AGND =	DGND = PGND = GND.)
-----------------	-------------------	-----------------------	-----------------	---------------------

Rating	Symbol	Value	Unit

 $\label{eq:expectation} \begin{array}{l} \textbf{ELECTRICAL CHARACTERISTICS} \\ (4.5 \ V \leq VCC \leq 5.5 \ V, \ 7.0 \ V \leq VS \leq 18 \ V, \ RSTB = VCC, \ CR1.D[10] = 1, \ -40^{\circ}C \leq T_J \leq 150^{\circ}C, \ unless \ otherwise \ specified.) \ (Note \ 5) \end{array}$ 

Characteristic	Symbol	Conditions	Min	Тур	Max	Unit
CHARGE PUMP						
Charge Pump Fail Detection	CP <sub>FAIL</sub>	V(CP, VS) decreasing, SR0.D[6] $\rightarrow$ 1	4.925	5.375	5.750	V
Charge Pump Fail Detection Filter Time	t <sub>CPF_DGL</sub>		120	150	180	μs
Charge Pump Fail Hysteresis	CP <sub>FAIL_HY</sub>	SR0.D[6] $\rightarrow$ 0 (after read status if V(CP,VS) > CP <sub>FAIL+FAIL_HY</sub> )	-	100	-	mV
Charge Pump Over-voltage Detection	CP <sub>OV</sub>	VS increasing	28.0	30.25	32.5	V
Charge Pump Over–voltage Hysteresis	CP <sub>OV_HYS</sub>		0.5	1.0	2.0	V
CP Switch Resistance	R <sub>CPTOT</sub>	*Guaranteed by Simulation* 8x CP switches in parallel, T <sub>A</sub> = 25°C	-	1.5	-	Ω
Switched CP Output Resis- tance	R <sub>CPSW_ON</sub>	CR1.D[9] = 1, I(CPSW) = 5 mA	-	-	100	Ω
Switched CP Output Leakage	CP <sub>SW_LKG</sub>	CR1.D[9] = 0	-1.0	0	1.0	uA
DIGITAL I/O						
V <sub>IN_X</sub> High	V <sub>INHX</sub>	CSB, SCLK, SI, RSTB, FSM, PWMx	3.5	-	-	V
V <sub>IN_X</sub> Low	V <sub>INLX</sub>	CSB, SCLK, SI, RSTB, FSM, PWMx	-	-	1.5	V
Input Pull-down Resistance	R <sub>PDX</sub>	SCLK, SI, RSTB, FSM, PWMx, V <sub>INX</sub> = VCC	70	100	130	kΩ
Input Pull-up Resistance	R <sub>PU</sub>	CSB, V <sub>IN</sub> = 0V	70	100	130	kΩ
Input Current	I <sub>INX</sub>	$V_{INX}$ = 5.5V: SCLK, SI, RSTB, FSM, PWMx $V_{INX}$ = 0V: CSB	_ _80	0	80 -	μΑ
Input Leakage	I <sub>IN_LKG</sub>	V <sub>INX</sub> = 0V: SCLK, SI, RSTB, FSM, PWMx V <sub>INX</sub> = VCC: CSB	-1.0	0	1.0	μΑ
Input Filter Time	t <sub>IN_DGL</sub>	FSM input	8.0	10	12	μs

Input Leakage	I <sub>IN_LKG</sub>	V <sub>INX</sub> = 0V: SCLK, SI, RSTB, FSM, PWMx V <sub>INX</sub> = VCC: CSB	-1.0	0	1.0	μΑ	
Input Filter Time	t <sub>IN_DGL</sub>	FSM input	8.0	10	12	μs	
Reset De-glitch Time	t <sub>RST_DGL</sub>	Minimum RSTB pulse (H $\rightarrow$ L $\rightarrow$ H) detected	8.0	-	-	μs	
Reset Assert Time	t <sub>WRST</sub>	Minimum RSTB hold after $H \rightarrow L$ transition	-	11	15	μs	
SO Low Voltage	V <sub>SOL</sub>	I <sub>SINK</sub> = 1.0 mA	-	-	0.4	V	
SO High Voltage	V <sub>SOH</sub>	I <sub>SOURCE</sub> = 1.0 mA	VCC - 0.4	-	-	V	
SO Tri-State Leakage Current	SO <sub>LKG</sub>	CSB = VCC, SO = VCC/2	-1.0	-	1.0	μΑ	
SERIAL PERIPHERAL INTERF	ACE (See Fi	gure 4)					
VCC - 5 0V ESCLK - 2 5 MHz CLOAD - 80 pE all timing is at 30% and 70% VCC unless otherwise specified							

VCC = 5.0V, FSCLK = 2.5 MHz, CLOAD = 80 pF, all timing is at 30% and 70% VCC unless otherwise specified.								
SCLK Clock Period	t <sub>SCLK</sub>		400	-	-	ns		
SCLK High Time	t <sub>CLKH</sub>	SCLK = 70% VCC to 70% VCC	200	-	-	ns		
SCLK Low Time	t							

SCLK Low Time

**ELECTRICAL CHARACTERISTICS** (4.5 V  $\leq$  VCC  $\leq$  5.5 V, 7.0 V  $\leq$  VS  $\leq$  18 V, RSTB = VCC, CR1.D[10] = 1, -40°C  $\leq$  T<sub>J</sub>  $\leq$  150°C, unless otherwise specified.) (Note 5)

Characteristic	Symbol	Conditions	Min	Тур	Max	Unit	
SERIAL PERIPHERAL INTERFACE (See Figure 4)							
CSB to SO Assert Time	t <sub>SO_A</sub>	CSB = 30% VCC to SO = 30% 70% VCC					

#### ELECTRICAL CHARACTERISTICS

 $(4.5 \text{ V} \leq \text{VCC} \leq 5.5 \text{ V}, 7.0 \text{ V} \leq \text{VS} \leq 18 \text{ V}, \text{RSTB} = \text{VCC}, \text{CR1.D[10]} = 1, -40^{\circ}\text{C} \leq \text{T}_{J} \leq 150^{\circ}\text{C}, \text{ unless otherwise specified.}) (\text{Note 5})$ 

Characteristic	Symbol	Conditions	Min	Тур	Max	Unit			
PRE-DRIVER SLOPE CONTROL									
High-side Pre-charge Current		I_PCFx[2:0] = 0x00	24.84	28.88	32.92				
GHx Falling Slope		I_PCFx[2:0] = 0x01	30.64	35.63	40.62				
V(GHx) = (VS + 3.5) V		I_PCFx[2:0] = 0x02	36.12	42.00	47.88				
		I_PCFx[2:0] = 0x03	41.61	48.38	55.15	~ ^			
	IPRCX_F	I_PCFx[2:0] = 0x04	47.41	55.13	62.85	mA			
		I_PCFx[2:0] = 0x05	52.89	61.50	70.11				
		I_PCFx[2:0] = 0x06	58.38	67.88	77.38				
		I_PCFx[2:0] = 0x07	64.18	74.63	85.08				
High-side Slew Current		SR_CTRLx[2:0] = 0x00	1.23	1.50	1.77				
GHx Rising and Falling Slope		SR_CTRLx[2:0] = 0x01	1.94	2.25	2.57				
Rising: V(GHx) = (VS + 3.5) V		SR_CTRLx[2:0] = 0x02	2.91	3.38	3.85				
Falling: V(GHx) = 3.5 V		SR_CTRLx[2:0] = 0x03	4.52	5.25	5.99	~ ^			
	ISRX	SR_CTRLx[2:0] = 0x04	6.78	7.88	8.98	mA			
		SR_CTRLx[2:0] = 0x05	10.00	11.63	13.26				
		SR_CTRLx[2:0] = 0x06	14.84	17.25	19.67				
		SR_CTRLx[2:0] = 0x07	21.93	25.50	29.07				
Low-side Drive Current		SR_CTRLx[2:0] = 0x00	5.16	6.00	6.84				
GLx Rising and Falling slope		SR_CTRLx[2:0] = 0x01	7.74	9.00	10.26				
V(GLx) = 3.5 V		SR_CTRLx[2:0] = 0x02	11.63	13.52	15.41				
		SR_CTRLx[2:0] = 0x03	18.06	21.00	23.94	~ ^			
	LSX	SR_CTRLx[2:0] = 0x04	27.11	31.52	35.93	mA			
		SR_CTRLx[2:0] = 0x05	40.01	46.52	53.03				
		SR_CTRLx[2:0] = 0x06	59.34	69.00	78.66				
		SR_CTRLx[2:0] = 0x07	87.72	102.00	116.28				

#### SLOPE CONTROL CALIBRATION UNIT

Window Thresholds	Falling slope window lower thresho	5ld 3.0	5.0	7.0

#### **ELECTRICAL CHARACTERISTICS**

 $(4.5 \text{ V} \le \text{VCC} \le 5.5 \text{ V}, 7.0 \text{ V} \le \text{VS} \le 18 \text{ V}, \text{RSTB} = \text{VCC}, \text{CR1.D[10]} = 1, -40^{\circ}\text{C} \le \text{T}_J \le 150^{\circ}\text{C}, \text{ unless otherwise specified.}) (Note 5)$ 

Characteristic	Symbol	Conditions	Min	Тур	Max	Unit
SLOPE CONTROL CALIBRAT	ION UNIT					
Calibration Pre-charge Time		CAL_PC[3:0] = 0x06		650		
		CAL_PC[3:0] = 0x07		750	1	
HBX Rising & Falling Slope		CAL_PC[3:0] = 0x08		850	1	
		CAL_PC[3:0] = 0x09		950	1	
		CAL_PC[3:0] = 0x0A	() ( , , , , , 7)	1050	() (, (, , , 7))	
	<sup>t</sup> CAL_PCx	CAL_PC[3:0] = 0x0B	(Note 7)	1150	(Note 7)	ns
		CAL_PC[3:0] = 0x0C		1250	1	
		CAL_PC[3:0] = 0x0D		1350		
		CAL_PC[3:0] = 0x0E		1450		
		CAL_PC[3:0] = 0x0F		1550		
Calibration Delay Time		CAL_DLY[3:0] = 0x00		0.35		
		CAL_DLY[3:0] = 0x01		0.55		
HBX Rising & Falling Slope		CAL_DLY[3:0] = 0x02		0.75		
		CAL_DLY[3:0] = 0x03		0.95	1	
		CAL_DLY[3:0] = 0x04		1.15	1	
		CAL_DLY[3:0] = 0x05		1.35	1	
		CAL_DLY[3:0] = 0x06		1.55		
		CAL_DLY[3:0] = 0x07	(Nata 7)	1.75	(Niete 7)	
	<sup>I</sup> CAL_DLYx	CAL_DLY[3:0] = 0x08	(Note 7)	1.95	(Note 7)	μs
		CAL_DLY[3:0] = 0x09		2.15	1	
		CAL_DLY[3:0] = 0x0A		2.35		
		$CAL_DLY[3:0] = 0x0B$		2.55		
		CAL_DLY[3:0] = 0x0C		2.75	]	
		CAL_DLY[3:0] = 0x0D		2.95	]	
		CAL_DLY[3:0] = 0x0E		3.15	]	
		$CAL_DLY[3:0] = 0x0F$		3.35	]	

#### HALF-BRIDGE DIAGNOSTICS

VDS Monitor Thresholds		VDSx[2:0] = 0x00	263	300	337		
		VDSx[2:0] = 0x01	356	400	444		
VDS = V(VS, HBx)		VDSx[2:0] = 0x02	445	500	555	mV	
		VDSx[2:0] = 0x03	534	600	666		
– or–	VDSTHRX	VDSx[2:0] = 0x04	623	700	777		
		VDSx[2:0] = 0x05	712	800	888		
VDS = V(IIDX, GIVD)		VDSx[2:0] = 0x06	801	900	999		
		VDSx[2:0] = 0x07	890	1000	1110		
VDS Monitor Filter Time	t <sub>DGL_STAT</sub>		0.92	1.15	1.38	μs	
VDS Monitor Propagation Delay	t <sub>VDSS_PD</sub>		_	550	750	ns	

5. Min/Max values are valid for the stated temperature range unless noted otherwise. Min/Max values are guaranteed by test, design or statistical correlation

6. No production test

These values, measured in production via test mode, result in values that are t<sub>SYNC</sub> longer than the stated values. The specification limits shall therefore be: (t<sub>CAL\_PCx</sub> Typ + t<sub>SYNC</sub> Typ) ±20%, (t<sub>CAL\_DLYx</sub> Typ + t<sub>SYNC</sub> Typ) ±20%, and (t<sub>DLYx</sub> Typ + t<sub>SYNC</sub> Typ) ±20%.

 $\label{eq:expectation} \begin{array}{l} \textbf{ELECTRICAL CHARACTERISTICS} \\ (4.5 \ V \leq VCC \leq 5.5 \ V, \ 7.0 \ V \leq VS \leq 18 \ V, \ RSTB = VCC, \ CR1.D[10] = 1, \ -40^{\circ}C \leq T_J \leq 150^{\circ}C, \ unless \ otherwise \ specified.) \ (Note \ 5) \end{array}$ 

Characteristic	Symbol	Conditions	Min	Тур	Max	Unit
HALF-BRIDGE DIAGNOST	ICS					
VDS Overload Detection		T_DLYX[3:0] = 0x00		1.05		
Rising or Falling Slope		T_DLYX[3:0] = 0x01		1.65		
		T_DLYX[3:0] = 0x02		2.25		
		T_DLYX[3:0] = 0x03		2.85		
		T_DLYX[3:0] = 0x04		3.45		
		T_DLYX[3:0] = 0x05		4.05		
		T_DLYX[3:0] = 0x06		4.65		
		T_DLYX[3:0] = 0x07	() (a (a 7)	5.25	(Note 7)	_
	<sup>t</sup> DLYX	T_DLYX[3:0] = 0x08	(Note 7)	5.85		μs
		T_DLYX[3:0] = 0x09		6.45		
		T_DLYX[3:0] = 0x0A		7.05		
		T_DLYX[3:0] = 0x0B		7.65		
		T_DLYX[3:0] = 0x0C		8.25		
		T_DLYX[3:0] = 0x0D		8.85		
		T_DLYX[3:0] = 0x0E		9.45		
		T_DLYX[3:0] = 0x0F		10.05		
HBx Input Resistance	R <sub>HBX</sub>	HBx, SH7, DL7 – Pull-down to AGND	-	26	-	kΩ
HBx Monitor Threshold	VHB <sub>THR</sub>		45	50	55	



#### DETAILED OPERATING DESCRIPTION

#### **Power Supply**

The power supply block provides:

- all internal supply and reference voltages;
- all internal bias and reference currents;
- VCC power-on reset (POR) and VS under/over-voltage lockout signals.

The analog and power portions of the device (reference voltages/currents, charge pump, low-side gate drivers, etc.) are supplied from the VS terminal. Each of the low-side gate driver outputs (GLx) is supplied from VS via an individual buffer (source follower) with voltage limit functionality. The high-side gate driver outputs (GHx) are supplied from a regulated charge pump.

The logic core and the SPI communication interface are supplied from the VCC terminal in order to achieve a high frequency operation by use of external bypass capacitors. In case of breakdown of the external voltage regulator, the device can be protected by use of an external voltage limiter, which must limit the maximum voltage at the VCC terminal to VCC<sub>MAX</sub> (see § *MAXIMUM RATINGS*).

The outputs are disabled during device initialization at power–up via an interlock between VS and VCC and such that no control is available until after VCC > VCC<sub>PORR</sub> (see § *Electrical Characteristics: VCC Supply*). Reverse battery protection for VS and the VCC regulator is provided externally by the application (see Figure 2).

- VS<sub>OVSDF</sub> < VS < VS(CP<sub>OV</sub>) the charge pump including the CPSW output is functional, but the GHx outputs are shut down;
- $VS > VS(CP_{OV})$

the charge pump is disabled and the charge pump buffer capacitor is discharged to VS in order to protect the device from destruction.

In the case of VS overvoltage, the charge pump automatically resumes normal operation when the VS voltage returns to below  $CP_{OV} - CP_{OV_HYS}$ . In the case of VS < VS<sub>PWM</sub> or V(CP, VS) < CP<sub>LOW</sub> it should be considered for the microcontroller to adopt a PWM duty ratio management schema in order to minimize charge pump loading while ensuring smooth motor operation.



Figure 5. Charge Pump Characteristics



Figure 6. Charge Pump Overvoltage Behavior

#### **SPI Interface**

A full-duplex synchronous serial data transfer interface (SPI) is used to control the device and provide diagnosis during normal operation. Daisy chain capability of the interface is implemented in order to minimize circuit expenditure and communication efforts. The SPI protocol utilizes 16-bit data words (B15 = MSB). The idle state of SCLK is

#### Table 2. SPI INPUT DATA FORMAT

	Command Input Message Format														
MSB															LSB
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
A3	A2	A1	A0	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
4-bit REGISTER ADDRESS WATCH DOG					11-bit INPUT DATA										

### Table 3. INPUT DATA STRUCTURE PROTOTYPE

Input Data Prototype												
CRx	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	?	?	?	?	?	?	?	?	?	?	?	?

#### Table 4. SPI INPUT REGISTER DEFINITIONS

Defined Co	ommand Input	Register	s (CRx)				
		D15	D14	D13	D12	D11	D10
Register Name	Alias	A3	A2	A1	A0		D10
Status Output Mode & HBx Enable	CR0	0	0	0	0		

Table 6. CR0 INSTRUCTION DEFINITIONS

Mnemonic Value

#### Table 12. CR3 INSTRUCTION DEFINITIONS

Mnemonic	Value	Comment						
PWMx[1:0]	00	Output PWM source is input PWM1 (default).						
1 11111/[1.0]	01 Output PWM source is input PWM2.							
	10	Output PWM source is input PWM3.						
	11	Output PWM source is input PWM4.						

#### Table 13. CR4: HBx CALIBRATION CONTROL REGISTER

0.0.4	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CR4	WD		CAL_D	LY[3:0]			CAL_F	PC[3:0]		CAL_SEL[2:0]		

#### Table 14. CR4 INSTRUCTION DEFINITIONS

Mnemonic	Value	Comment
CAL_DLY[3:0]	0000	Delay time: end of rising falling slope 0.35 $\mu$ s (default).
	0001	Delay time: end of rising falling slope 0.55 $\mu$ s.
	0010	Delay time: end of rising falling slope 0.75 μs.
	0611B40	መୁ <b>ጀሬ፰፶ሽሸተቆጀ</b> 1end of rising falling slope 0.95 μs.
	0100	Delay time: end of rising falling slope 1.15 $\mu$ s.

0108 0 0 8 163.04 0 8 163.0488 476.2772.07949 501.871 49.663 .907.4 ref552.189 471.798 .907d0484287.093 590.457 .907

### Table 14. CR4 INSTRUCTION DEFINITIONS

Mnemonic	Value	Comment
CAL_SEL[2:0]	000	Calibration unit disabled (default).
	001	Select output HB1.
	010	Select output HB2.
	011	Select output HB3.
	100	Select output HB4.
	101	Select output HB5.
	110	Select output HB6.
	111	Select output SH7.

#### Table 15. CR5A – CR11A: HBx CONFIGURATION A REGISTER

CR11A: HBx CONFIGURA018 Tc(:8. .90 Tw[(1HB3.)TjET1970.7181 564.5481Tw<00ef>Tj8.4(1A: HBx CONFIGURA)7.55334 Tm0 Tc0 Tw(001)TjET147.4

Mnemonic	Value	Comment
VDSx[2:0]	000	Select VDS sense threshold 300 mV (default).
	001	Select VDS sense threshold 400 mV.
	010	Select VDS sense threshold 500 mV.
	011	Select VDS sense threshold 600 mV.
	100	Select VDS sense threshold 700 mV.
	101	Select VDS sense threshold 800 mV.
	110	Select VDS sense threshold 900 mV.
	111	Select VDS sense threshold 1000 mV.
T_DLY[3:0]	0000	Select VDS overload detect delay 1.05 µs (default).
	0001	Select VDS overload detect delay 1.65 µs.
	0010	Select VDS overload detect delay 2.25 µs.
	0011	Select VDS overload detect delay 2.85 $\mu$ s.
	0100	Select VDS overload detect delay 3.45 µs.
	0101	Select VDS overload detect delay 4.05 µs.
	0110	Select VDS overload detect delay 4.65 µs.
	0111	Select VDS overload detect delay 5.25 $\mu$ s.
	1000	Select VDS overload detect delay 5.85 $\mu$ s.
	1001	Select VDS overload detect delay 6.45 $\mu$ s.
	1010	Select VDS overload detect delay 7.05 $\mu$ s.
	1011	Select VDS overload detect delay 7.65 $\mu$ s.
	1100	Select VDS overload detect delay 8.25 $\mu$ s.
	1101	Select VDS overload detect delay 8.85 $\mu$ s.
	1110	Select VDS overload detect delay 9.45 $\mu$ s.
	1111	Select VDS overload detect delay 10.05 µs.
SR_CTRL[2:0]	000	Select rising/falling slope slew phase current 1.5 mA (default).
	001	Select rising/falling slope slew phase current 2.25 mA.
	010	Select rising/falling slope slew phase current 3.38 mA.
	011	Select rising/falling slope slew phase current 5.25 mA.
	100	Select rising/falling slope slew phase current 7.88 mA.
	101	Select rising/falling slope slew phase current 11.63 mA.
	110	Select rising/falling slope slew phase current 17.25 mA.
	111	Select rising/falling slope slew phase current 25.50 mA.

### Table 18. CR5B – CR11B INSTRUCTION DEFINITIONS

### Table 19. CR12: HBx DIAGNOSIS CONTROL REGISTER

CR12	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	WD	0	0	0	TST_LS7	TST_LS5	TST_LS3	TST_LS1	TST_HS7	TST_HS5	TST_HS3	TST_HS1

### Table 20. CR12 INSTRUCTION DEFINITIONS

Mnemonic	Value	Comment
TST_LSx	0	Disable low-side test current (default).
	1	Enable low-side test current.
TST_HSx	0	Disable high-side test current (default).
	1	Enable high-side test current.

#### Table 21. CR14: HBx PWM DE-GLITCH

CR14	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	WD	0	0	0	0	DGL7	DGL6	DGL5	DGL4	DGL3	DGL2	DGL1

#### Table 22. CR14 INSTRUCTION DEFINITIONS

Mnemonic	Value	Comment
DGLX	0	Type 1 de–glitch: $t_{PWM}$ _DGL = $t_{BLANKx}$ + $t_{PRCx}$ + $t_{DLYx}$ (default).
- 3-24	1	Type 2 de–glitch: $t_{PWM_DGL} = t_{PRCx} + t_{DLYx}$

#### Table 23. CR15: TEST MODE REGISTER

CR15	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	WD	Factory Use Only										

#### SPI Diagnosis Set

The first 3 bits D[15:13] serve as address bits, while the 13 bits D[12:0] are used as data bits. Output data for "not used" register adresses is D[11:0] = 0. The address of the Status Register (SRx) accessed for status information to be retrieved via a subsequent SPI frame is selected by the control register bits CR0.SRA\_MODE and CR0.SRA[2:0] (see Table 5, Table 6).

Two different reading modes are provided depending on the SRA\_MODE bit:

- when CR0.SRA\_MODE = 0, the SRx address selected via bits CR0.SRA[2:0] will be used for a single status read command and the SR address returns to SR0 (device status register, default state) after reading;
- when CR0.SRA\_MODE = 1, the SRx address selected via bits CR0.SRA[2:0] will be used for the next and all further status read commands until a new address or mode is selected.

The default reading mode and address after VCC POR or wake-up is  $CR0.SRA\_MODE = 0$ , CR0.SRA[2:0] = 00.

All status diagnosis bits are initialized to logic 0 after a reset event and in normal operation except:

- the NORMAL MODE (NM) bit indicates NORMAL MODE when SRx.NM = 1;
- the Register Clear Flag (RCF) bit is set (SR0.RCF = 1) after a mode change to NORMAL MODE (see § *Operating Modes*).

The RCF bit indicates that all input and output registers were initialized; the bit is cleared after SR0 is read.

All status diagnosis bits are latched with the exception of the SR5.D[3:0] bits (see § *Output Status Monitoring*). To de–latch a diagnosis:

- the referring failure has to be removed;
- the referring failure bit has to be read by SPI diagnosis.

Refer to § *Protection and Diagnosis* to restart the outputs after a fault condition. The SPI diagnosis set (output data map) and output data structure prototype are shown in the following tables.

	Status Output Message Format														
MSB															LSB
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
A2	A1	A0	NM	D11	D10	D9	D8	D7	D5	D5	D4	D3	D2	D1	D0
3-bit REGISTER ADDRESS MODE				12-bit OUTPUT DATA											

#### Table 24. SPI OUTPUT DATA FORMAT

#### Table 25. OUTPUT DATA STRUCTURE PROTOTYPE

	Output Data Prototype													
5	SRx	NM	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		NM	?	?	?	?	?	?	?	?	?	?	?	?

#### Table 26. SPI OUTPUT REGISTER DEFINITIONS

Defined Status Outpu	t Registers (SRx)				
		D15	D14	D13	D12
Register Name	Alias	A2	A1	A0	NM
Device Status	SR0	0	0	0	
HB 16 Status Monitor	SR1	0	0	1	
HB 7 Status & VDS Monitors	SR2	0	1	0	
HB 16 VDS Monitor	SR3	0	1	1	
HBx Calibration Result	SR4	1	0	0	NIVI
SH7, DL7 & HB 16 Output Status	SR5	1	0	1	
Not Used	SR6	1	1	0	
Device ID/Test Mode	SR7	1	1	1	

#### Table 27. SR0: DEVICE STATUS REGISTER

SR0	NM	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0.10	NM	ТМ	RCF	FSM	SPIF	CPL	CPF	UVF	OVF	0	0	HB_QSB	0

#### Table 28. SR0 RESPONSE DEFINITIONS

Mnemonic	Value	Comment
ТМ	0	Test mode inactive (default).
	1	Test mode active.
RCF	0	Registers not cleared (command input and status output registers).
	1	Registers cleared (after mode change to "NORMAL").
FSM	0	FSM input pin = 0 (FSM not asserted).
	1	FSM input pin = 1 (FSM asserted).
SPIF	0	SPI message correct.
	1	SPI message failure.
CPI	0	Charge pump in regulation
OI L	1	V(CP, VS) < CP <sub>LOW</sub> – <i>OR</i> – VS < VSPWM (Charge Pump Low).
CPF	0	Half bridge high-side pre-driver activation allowed.
0	1	Half bridge high-side pre-driver activation not allowed (Charge Pump Fail).
UVE	0	VS supply in normal range.
011	1	VS supply below normal range.
OVE	0	VS supply in normal range.
•	1	VS supply above normal range.
D3	0	Not used.
D2	0	Not used.
HB QSB	0	Quick Status Bit: VDS normal – no overload detected.
	1	Quick Status Bit: VDS failure – overload detected (VDS_Hx or VDS_Lx).
D0	0	Not used.

#### Table 29. SR1: HBx STATUS MONITOR REGISTER

SR1	NM	D11	D10	D9	D8	D7	D6	D5	D4	D3
Until										

### Table 30. SR1 RESPONSE DEFINITIONS

Mnemonic	Value	Comment
SWHx	0	GHx output is "low" (default).
	1	GHx output is "high".
SWLX	0	GLx output is "low" (default).
01124	1	GLx output is "high".

#### Table 31. SR2: HB 7 STATUS & VDS MONITOR REGISTER

SR2	NM	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	NM	0	0	0	0	0	0	0	0	VDS_H7	VDS_L7	SWH7	SWL7

#### Table 32. SR2 RESPONSE DEFINITIONS

Mnemonic	Value	Comment
	0	SH7 high-side power switch normal - no overload detected (default).
VDS_H/	1	SH7 high-side power switch failure – overload detected.
	0	DL7 low-side power switch normal - no overload detected (default).
VD5_L7	1	DL7 low-side power switch failure -overload detected.
S/M/HZ	0	GH7 output is "low" (default).
3007	1	GH7 output is "high".
014# 7	0	GL7 output is "low" (default).
SVVL7	1	GL7 output is "high".

#### Table 33. SR3: HBx VDS MONITOR REGISTER

SR3	NM	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	NM	VDS_H6	VDS_L6	VDS_H5	VDS_L5	VDS_H4	VDS_L4	VDS_H3	VDS_L3	VDS_H2	VDS_L2	VDS_H1	VDS_L1

#### Table 34. SR3 RESPONSE DEFINITIONS

Mnemonic

#### Table 36. SR4 RESPONSE DEFINITIONS

00

CAL\_DLY\_F[1:0]

When not in test mode (SR0.TM = 0), a status request via CR0.D[10:7] returns SR7.D[11:0] = DEV\_ID[11:0] as defined in Table 41. The default content of SR7 after VCC POR or wake–up is SR7.D[11:0] = 0.

The DEV\_ID[5:0] revision value may be changed based on whether the entire die (silicon) or intermediate layer (mask) is affected. The revisions can be e.g. classified accordingly:

- silicon revision: defined area changed (isolation pocket or other boundary, bond pad etc. changed/moved) or digital core changed (isolation pocket changed or unchanged);
- mask revision: interconnect changed (metal and/or polysilicon/contact/via).

The mask revision value is set to  $DEV_{ID}[2:0] = 000$  whenever the die revision is incremented. Table 42 shows how the value encoding scheme is used to indicate the device revision level.

Silicon Rev	ision/	Mask Revision			
DEV_ID[5:3]	LEVEL	DEV_ID[2:0]	LEVEL		
000	А	000	0		
001	В	001	1		
010	С	010	2		
011	D	011	3		
100	E	100	4		
101	F	101	5		
110	G	110	6		
111	Н	111	7		

#### Table 42. DEVICE REVISION LEVEL ENCODING

#### Half-bridge Gate Drivers

The half-bridge drivers are used to control the gates of external logic-level NMOS power switches. Drivers HB1 ... HB6 are dedicated to e.g. motor control – the switches are normally connected in half-bridge configuration. HB7 is dedicated to e.g. heater control – the switches are normally connected independently in a split configuration but may be optionally connected in a half-bridge configuration (see Figure 2). The device is initialized at power-up into a reduced power state (CR1.DRV\_EN = 0, see Table 7, Table 8):

- the charge pump is disabled;
- all gate drive currents are disabled.
- HBx diagnostic test currents are available (see § *Monitoring of Half-bridge Drivers in OFF-state*).

The device is placed into a full power state when  $CR1.DRV_EN = 1$ . The half-bridges are held in high-impedance state (external NMOS are off) via gate pull-down structures which are activated during power-up, while in reduced power state, or when in sleep mode.

#### Control of Half-bridge Drivers

The operation of the drivers is controlled by SPI configuration individually for each driver. All half–bridges can be operated in 100% "ON" mode as well as in PWM mode.

The control schema for HB1 ... HB7 in half-bridge configuration and for HB7 in split configuration is shown in Table 44 (see also § *SPI Control Set*).

The CR0.HB\_ENx bits are used to enable the operation of the selected half-bridges and to re-start the drivers after a fault condition:

- when CR0.HB\_ENx=0, the GHx and GLx outputs are disabled (i.e. VGS ≈ 0 V);
- when CR0.HB\_ENx=1, the GHx and GLx outputs are enabled.

The CR1.HB\_CFG7 bit is used to enable the split configuration of half-bridge HB7:

- when CR1.HB\_CFG7=0, HB7 is in operating in half-bridge configuration;
- when CR1.HB\_CFG7=1, HB7 is in operating in split configuration.
- NOTE: When operating HB7 in split configuration, both the high-side and low-side switches are in ON-state simultaneously. Therefore the CR1.HB\_CFG7 bit should only be set to '1' when the application hardware is configured correctly. In case of erratic hardware configuration, VDS overload monitoring protects the external power switches.

The CR1.HB\_MODEx bits are used to control the polarity of the selected half-bridge:

- when CR1.HB\_MODEx=0, the low-side driver (PDL) is in an ON state (i.e. GLx = VGS ≈ V<sub>PDLX</sub>, see § *Electrical Characteristics: Half-Bridge Pre-Driver Outputs*);
- when CR1.HB\_MODEx=1, the high-side driver (PDH) is in an ON state (i.e. GHx = VGS ≈ V<sub>PDHX</sub>, see § *Electrical Characteristics: Half-Bridge Pre-Driver Outputs*).



Figure 8. Gate Drive Operation in PWM Mode

For each individual half-bridge:

- cross-conduction blanking time is selected via the BLANKx[1:0] bits;
- pre-charge current is selected via the I\_PCRx[2:0] bits for the rising slope and via the I\_PCFx[2:0] bits for the falling slope;
- pre-charge time for both slopes is selected via the T\_PCx[1:0] bits;
- slew current for both slopes is selected via the SR\_CTRLx[2:0] bits – this parameter controls the external NMOS switches' rise/fall times to adopt proper EMC performance and minimize switching losses;
- VDS overload detection delay is selected via the T\_DLYx[3:0] bits this parameter controls when the VDS overload detection is performed (see § *Overload Protection*);
- VDS overload detection threshold is selected via the VDSx[2:0] bits this parameter controls the VDS monitoring comparator threshold (see Table 17, Table 18);
- adaptive PWM input de–glitch construction when in half–bridge configuration is selected by DGLx[6:0] bits (see Figure 10, Figure 11, Table 21 and Table 22).

Please refer to § *Electrical Characteristics* for defined blanking (t<sub>BLANKX</sub>), pre-charge (t<sub>PRCX</sub>, I<sub>PRCX\_R</sub>, I<sub>PRCX\_F</sub>), slew (I<sub>SRX</sub>), delay (t<sub>DLYX</sub>) and VDS threshold (VDS<sub>THRX</sub>) parametric values.

NOTE: A proper initial switching parameter set (e.g. VDS<sub>THRX</sub>, t<sub>PRCX</sub>, I<sub>PRCX\_R</sub>, I<sub>SRX</sub>, I<sub>PRCX\_F</sub>) for a chosen MOSFET has to be evaluated for a desired switching speed (see also § *Overload Protection*).

When operated in PWM mode, the PWMx input signals are each provided with a symmetrical de–glitch within a half– bridge's control logic. The de–glitch time  $(t_{PWM_DGL})$  is adapted to the SPI settings  $t_{BLANKX}$ ,  $t_{PRCX}$ ,  $t_{DLYX}$  and DGLx as selected for each channel (see § *Electrical Characteristics: Half–Bridge Pre–Driver Outputs & Pre–driver Slope Control*).

The adapted  $t_{PWM\_DGL}$  avoids mistreatment of the half-bridge drivers by ensuring that a complete turn-on or turn-off sequence is executed (erratic pulse widths are thereby avoided) and assures correct operation of the VDS overload protection (see § *Overload Protection*).







Figure 12. HBx Output Switching in Half-Bridge Configuration

I t<sub>BLANK</sub> →

Figure 13. HB7 Output Switching in Split Configuration

Calibration is enabled when the

The temporal position (see Figure 13) of the target transition detection point (e.g. 10%, 90%) with respect to  $t_{CAL\_PCx}$  or  $t_{CAL\_DLYx}$  (or in normal operation,  $t_{DLYX}$ ) of the channel selected for calibration is dependent upon:

- the PWMx\_DGL resulting from the channel's operating configuration (see § *Switching Behavior of Half-bridge Drivers*, Figure 10 and Figure 11);
- the t<sub>BLANKX</sub> cross–conduction blank time setting as applicable;
- the t<sub>PRCX</sub>, I<sub>PRCX\_R</sub> and I<sub>PRCX\_F</sub> pre-charge phase time and current settings;

• the I<sub>SRX</sub> slew phase current setting.

Calibration may be performed at the application level during module end–of–line (EOL) test where the (adjusted) settings may be stored in a microcontroller's EEPROM. In order to maintain stable function and proper EMC performance with temperature drift and output load variations, the calibration can be verified/updated on a sample basis during normal application operation.



Figure 14. HBx Slope Control Calibration

The diagnostic consists of (see Figure 14 and Figure 15):

- a high-side and a low-side test current source at each odd-numbered HBx feedback input;
- a comparator (CMP5) at each HBx feedback input.

Provided the device is in NORMAL MODE (see § *Operating Modes*) and no global failure (see § *Device Fault* (*Global*) *Protection*) has been detected, the test current sources can be

activated individually by the TST\_HSx and TST\_LSx bits in the HB diagnosis register (CR12.D[5:0] – see Table 19, Table 20). Active pull-down current sources are disabled in

- when the battery supply voltage VS is below the minimum supply voltage for a regulated charge pump voltage OR V(CP,VS) drops below the minimum output voltage CP<sub>LOW</sub> this status is reported by the SR0.CPL bit in the device status register immediately after a de–glitch time t<sub>CPL\_DGL</sub> (see Table 27, Table 28). During this condition it should be considered for the microcontroller to adopt a PWM duty ratio management schema in order to minimize charge pump loading while ensuring smooth motor operation.
- when the charge pump output voltage V(CP, VS) drops below the charge pump fail threshold CP<sub>FAIL</sub>, the half bridge high–side and low–side gate drivers are latched off immediately after a de–glitch time t<sub>CPF\_DGL</sub> and the status is reported by the SR0.CPF bit in the device status register (see Table 27, Table 28).
- when the battery supply voltage VS is in the nominal operation range VS<sub>PWM</sub> < VS < VS<sub>OVSDR</sub> the full PWM operation of the GHx and GLx outputs is allowed;
- when the battery supply voltage is in over-voltage condition VS > VS<sub>OVSDR</sub>, the SR0.CPF bit is masked;
- when the battery supply voltage is in over-voltage condition VS<sub>OVSDF</sub> < VS < CP<sub>OV</sub> the charge pump including the CPSW output is functional but the GHx outputs are shut down;
- when the battery supply voltage exceeds the maximum supply voltage for the charge pump VS > CP<sub>OV</sub> the charge pump is disabled and the charge pump buffer capacitor is discharged to VS in order to protect the device from destruction.

Please refer to § *Device Fault (Global) Protection* to restart the outputs after a shutdown event.

#### **Over-voltage Condition**

During VS over-voltage, the behavior of the gate drivers (GHx and GLx) depends on the programmed operation mode:

 the high side gate drivers (GHx) are latched off immediately after de–glitch time t<sub>OVDGL</sub> (see § *Electrical Characteristics: VS Supply*) in order to protect the application from over load condition; while the low–side gate driver outputs (GLx) are operable in order to provide controlled braking (e.g. for lift gate motors);

- GH<sub>X</sub> pull-down current is reduced to 1 mA typ.(register contents are not changed – the current will revert to its prior value after VS over-voltage is resolved);
- the HBx test currents (see § *OFF-state Monitoring of Half-bridge Drivers*) are disabled immediately.

The VS over–voltage condition is reported by the SR0.OVF bit in the device status register (see Table 27, Table 28). When the battery supply voltage is in over–voltage condition VS > VS<sub>OVSDR</sub> the SR0.CPF bit is masked. Please refer to § *Device Fault (Global) Protection* to restart the outputs after a shutdown event.

A VCC overvoltage condition can occur during breakdown of the external voltage regulator. Please refer to *§ Failure of External Voltage Regulator* for details.

#### **Under Voltage Condition**

In case of VS under voltage condition:

- all outputs (GHx, GLx) are disabled immediately after the de–glitch time t<sub>UVDGL</sub> and the condition is reported by the SR0.UVF bit in the device status register (see Table 27, Table 28);
- the charge pump circuit and the switched charge pump output (CPSW) are still functional in order to keep the optional reverse battery and security switches active.

Please refer to § *Device Fault (Global) Protection* to restart the outputs after a shutdown event.

In case of VCC under voltage condition (power–on reset condition, VCC < VCC<sub>POR</sub>):

- the device enters **SLEEP MODE** immediately without de-glitch time;
- logic input pull–up/down resistors, GHx & GLx output pull–down resistors, and VCC under voltage lockout assure safe operating states for all outputs.

To restart the device after this condition a wake-up sequence is necessary (see § *Operating Modes*).

#### Logic I/O Plausibility Check

The logic I/O pins are protected against mistreatment by input de–glitch circuits. The de–glitch circuits are implemented digitally, refer to § *Electrical Characteristics: Digital I/O for values*.

#### FUNCTIONAL SAFETY SUPPORT STRATEGY

The device uses a closed-loop verification strategy in order to avoid mistreatment of the outputs and to support functional safety. The verification strategy is implemented based on the features in the following sections.

#### **SPI Communication Monitoring**

The SPI is protected against communication errors by use of the WD toggle bit and protocol check features (see § *SPI Interface*). In case of SPI communication error the device enters **FAILSAFE MODE** immediately (see § *Operating Modes*). A correct communication is reported in the NM bit (see § *SPI Diagnosis Set*).

#### **Gate Driver Status Monitoring**

The correct activation of the half-bridge drivers can be monitored by the microcontroller by means of SPI communication (see § *SPI Diagnosis Set*). The switching status of the output drivers is indicated by the SWLx and SWHx bits in the half-bridge status monitor register SR1. The bit value corresponds to the logic status of the driver. In PWM mode, both SWHx = 1 and SWLx = 1.

In case of a discrepancy between control data and status information from the device, the microcontroller has to drive the device into FAILSAFE MODE in order to avoid mistreatment of the motor drives, then transition the device to NORMAL MODE for reprogramming.

#### **Output Status Monitoring**

The status of the MOS switches and the motor connection lines can be monitored during NORMAL MODE



= 0008019 0 .028 0 c 6 3949 Tm(1c-000289.86 6 .5 14.284 9J/TT31 2..928 1.13

#### GENERIC MARKING DIAGRAM\*



onsemi, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries. onsemi owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of onsemi's product/patent coverage may be accessed at <a href="http://www.onsemi.com/site/pdf/Patent-Marking.pdf">www.onsemi.com/site/pdf/Patent-Marking.pdf</a>. Onsemi reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and onsemi makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or incruit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using onsemi