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DATA SHEET
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Enhanced 100 mA Linear Current Regulator and Controller for Automotive Sequenced LED Lighting

NCV7683

The NCV7683 consists of eight linear programmable constant current sources. The part is designed for use in the regulation and control of LED based Rear Combination Lamps and blinking functions for automotive applications. System design with the NCV7683 allows for two programmed levels for stop (100% Duty Cycle) and tail illumination (programmable Duty Cycle), or an optional external PWM control can be implemented.

LED brightness levels are easily programmed (stop is programmed to the absolute current value, tail is programmed to the duty cycle) with two external resistors. The use of an optional external ballast FET allows for power distribution on designs requiring high currents. Set back power limit reduces the drive current during overvoltage conditions. This is most useful for low power applications when no external FET is used.

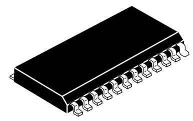
Sequencing functionality is activated, controlled, and programmed by individual pins. In addition to programming of the sequence interval, the device can sequence 8 individual output channels, 4 pairs of output channels, 2 quad output channels, or all 8 at once (for multi IC use at high currents).

Enhanced features of this device are a global enable function and display sequencing.

The device is available in a SSOP24 package with exposed pad.

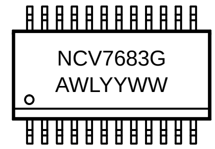
Features

- Constant Current Outputs for LED String Drive
- LED Drive Current up to 100 mA per Channel
- Open LED String Diagnostic with Open−Drain Output in All Modes
- Slew Rate Control Eliminates EMI Concerns
- Low Dropout Operation for Pre−Regulator Applications
- External Modulation Capable
- On−chip 800 Hz Tail PWM Dimming
- Single Resistor for Stop Current Set Point
- Single Resistor for Tail Dimming Set Point
- Overvoltage Set Back Power Limitation
- Improved EMC Performance
- Programmable Latch−Off function on Open String
  - Restart Option of Unaffected Strings
- Over Temperature Fault Reporting
- Global Enable
- Display Sequencing
- SSOP−24 Fused Lead Package with Exposed Pad
- AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices

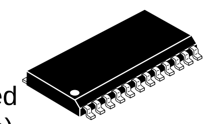


SSOP24 NB EP
CASE 940AP

MARKING DIAGRAM

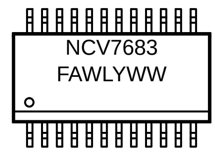


NCV7683 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package



SSOP24 NB EP
CASE 940AQ

MARKING DIAGRAM



NCV7683 = Specific Device Code
F = Fab Location
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
= Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping †
NCV7683DQR2G*	SSOP24 −EP (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Applications

- Rear Combination Lamps (RCL)
- Daytime Running Lights (DRL)
- Fog Lights
- Center High Mounted Stop Lamps (CHMSL) Arrays
- Turn Signal and Other Externally Modulated Applications
- Signature Lamp

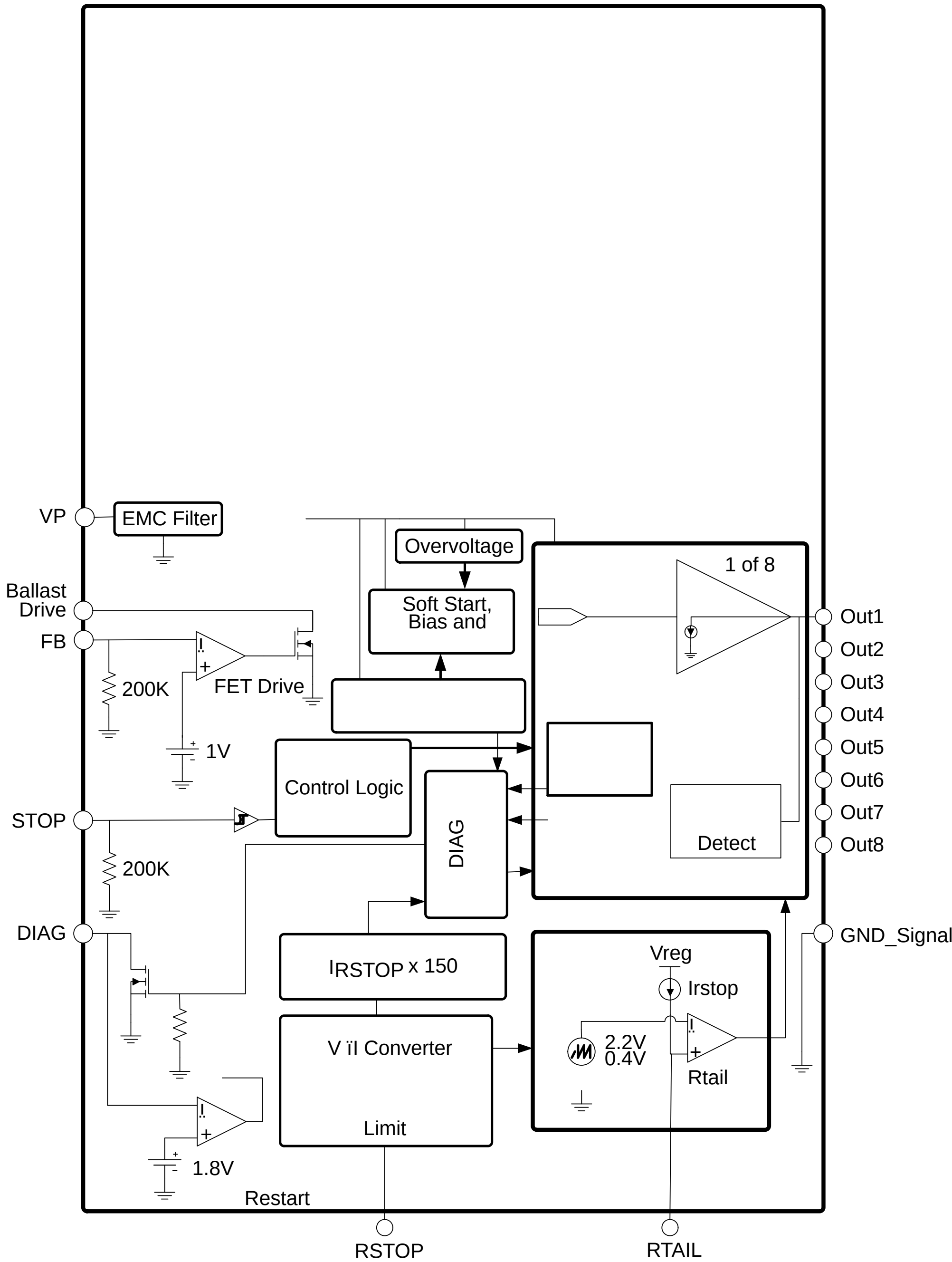


Figure 1. Block Diagram

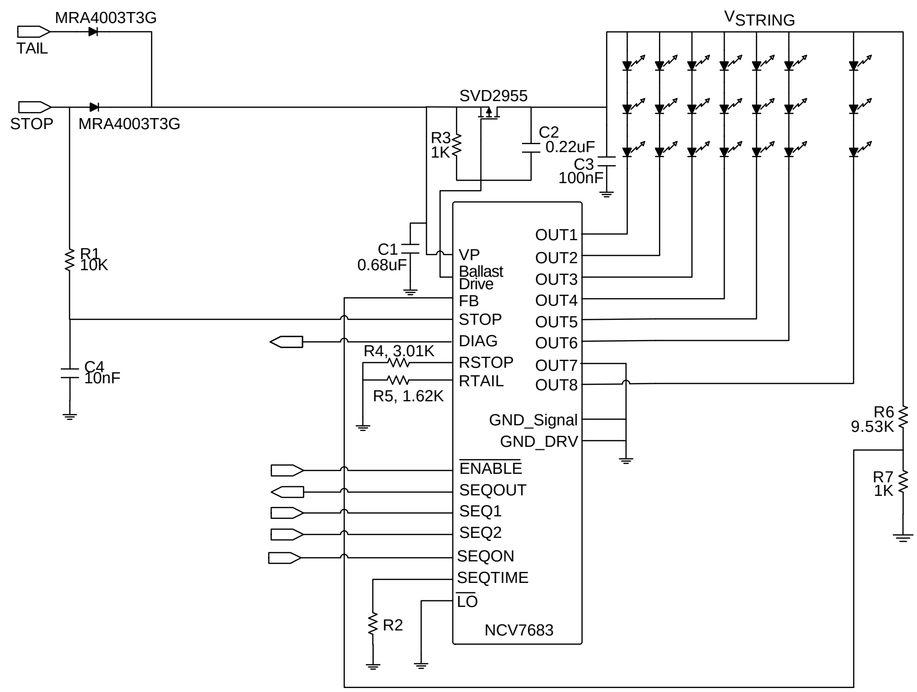


Figure 3. Application Diagram with External FET Ballast Transistor

R6 and R7 values shown yield 10.5 V regulation on V_{STRING}.
C1 is for line noise and stability considerations.
C3 is for EMC considerations.
.513 05175.321 00.51 m 1175.306 .7 0 0051175.4057 l01175.4057 l40.202175.306 .7-71 -2175.2457 l40107 175.0D (l40 -

P

Table 1. APPLICATION I/O TRUTH TABLE

$\overline{EN}$	SEQON	STOP INPUT	TAIL MODE	OUTx LATCH OFF (w/ $\overline{LO}$ = GND)	OUTX CURRENT	FAULT STATE*	DIAG STATE**
1	X	X	X	no	OFF	ï	1
0	0	0	0	no	OFF	ï	1
0	0	1	X	no	I_{STOP}	NORMAL	0
0	0	1	X	no	I_{STOP}	OPEN CIRCUIT***	1
0	0	1	X	yes	OFF	OPEN CIRCUIT***	1
0	0	0	1	no	PWM	NORMAL	0
0	0	0	1	no	PWM	OPEN CIRCUIT***	PWM
0	1	X	X	no	I_{STOP}	NORMAL	0
0	1	X	X	no	I_{STOP}	OPEN CIRCUIT***	1
0	1	X	X	yes	OFF	OPEN CIRCUIT***	1

Reference Figures below.
X = don’t care
0 = LOW
1 = HIGH
* Open Circuit, RSTOP Current Limit, Set Back Current Limit down 20%, and thermal shutdown
**Pull ïup resistor to DIAG and SEQOUT required.
*** OPEN CIRCUIT = Any string or SEQOUT open.

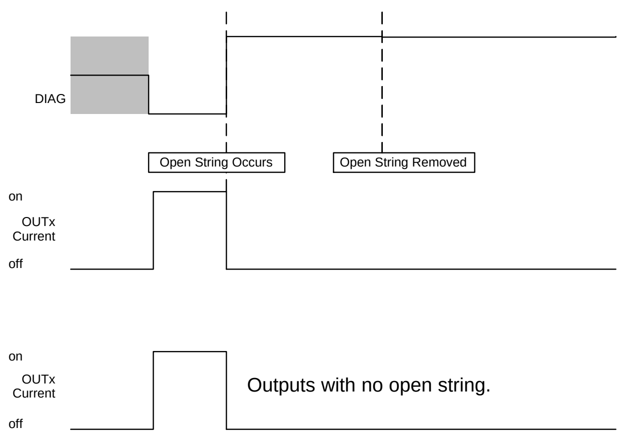


Figure 5. DIAG timing diagram WITH Open String Latch Active
All outputs latch off.

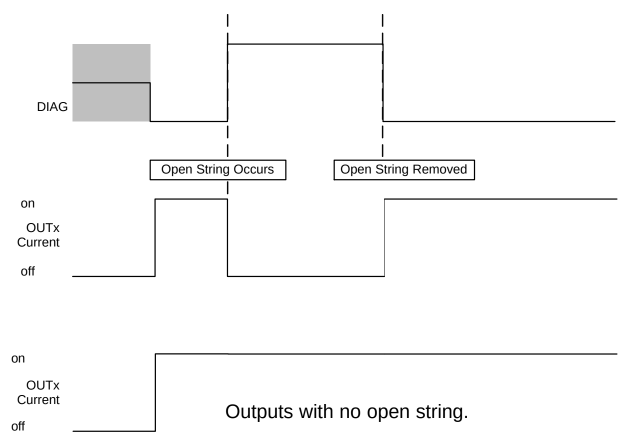


Figure 6. DIAG timing diagram WITHOUT Open String Latch Active
No outputs are turned off.
DIAG will report the state.

Sequence Programming Timing Diagrams

Table 2. PIN FUNCTION DESCRIPTION

SSOP ï24 Exposed Pad Package		
Pin #	Label	Description
1	DIAG	Open

Table 3. MAXIMUM RATINGS (Voltages are with respect to device substrate.)

Rating	Value	Unit
Supply Input (VP, Ballast Drive, STOP, DIAG, $\overline{\text{ENABLE}}$, SEQON, SEQOUT) DC Peak Transient	 ï0.3 to 40 40	V
Output Pin Voltage (OUTX)	ï0.3 to 40	V
Output Pin Current (OUTX)	200	mA
DIAG Pin Current	10	mA
Input Voltage (RTAIL, RSTOP, FB, SEQTIME, SEQ1, SEQ2, $\overline{\text{LO}}$)	ï0.3 to 3.6	V
Junction Temperature, T_J	ï40 to 150	°C
Peak Reflow Soldering Temperature: Lead ïfree 60 to 150 seconds at 217°C (Note 1)	260 peak	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 4. ATTRIBUTES

Characteristic	Value
ESD Capability Human Body Model Machine Model	 ≥ ± 4.0 kV ≥ ± 200 V
Moisture Sensitivity (Note 1)	MSL3
Storage Temperature	ï55 to 150°C
Package Thermal Resistance (Note 2) SSOP24 Junction–to–Board, $R_{\theta JB}$ Junction–to–Ambient, $R_{\theta JA}$ Junction–to–Lead, $R_{\theta JL}$	 18°C/W 78°C/W 54°C/W

1. For additional information, see or download onsemi

Table 5. ELECTRICAL CHARACTERISTICS
(4.5 V < VP < 16 V, STOP = VP, RSTOP = 3.01 kΩ, RTAIL = 1.62 kΩ, RSEQTIME = 4.99 kΩ, ï40°C ≤ T_J ≤ 150°C, unless otherwise specified.)

Characteristic	Conditions	Min	Typ	Max	Unit
SEQ1/SEQ2/$\overline{LO}$ LOGIC					
Input High Threshold		0.75	1.25	1.75	V
Input Low Threshold		0.70	1.00	1.44	V
V_{IN} Hysteresis		100	250	400	mV
Input Pull ïup Current	SEQx = 0 V	5	10	20	µA
CURRENT PROGRAMMING					
RSTOP Bias Voltage	Stop current programming voltage	0.94	1.00	1.06	V
RSTOP K multiplier I_{OUTX}/I_{RSTOP}		ï	150	ï	ï
RSTOP Over Current Detection	RSTOP = 0 V	0.70	1.00	1.45	mA
RTAIL Bias Current	Tail duty cycle programming current	290	330	370	µA
Duty Cycle	RTAIL = 0.49 V RTAIL = 0.76 V RTAIL = 1.66 V	3.5 17 59.5	5 20 70	6.5 23 80.5	%
SEQTIME Voltage		0.94	1.00	1.06	V
DIAG / SEQOUT OUTPUT					
Output Low Voltage	Output Active, $I_{DIAG,SEGOUT}$ = 1 mA	–	0.1	0.40	V
DIAG Output Leakage	V_{DIAG} = 5 V	ï	ï	10	µA
Open Load Reset Voltage on DIAG		1.6	1.8	2.0	V
SEQOUT Open Load Detection Threshold Voltage		0.70	0.8	0.90	V
SEQOUT Open Load Detection Sink Current		10	20	35	µA
AC CHARACTERISTICS					
Stop Turn ïon Delay Time	V(STOP) > 1.75 V to I(OUTx) = 90%				

TYPICAL CHARACTERISTICS

100
90
70
60
40
30
10
0
0 1 2 3 5 6 7 9
RSTOP (kΩ)

Figure 11. Iout vs. RSTOP

53
52
51
50
49
48
47
ï40 ï20 0 20 60 80 120 140
TEMPERATURE (°C)

Figure 12. Iout vs. Temperature

100
90
70
50
40
30
10
0
0 1 2 3 4 5 6 7
RTAIL (kΩ)

Figure 13. Duty Cycle vs. RTAIL

100
80
70
50
40
30
10
0
0 0.5 1.0 1.5 2.0 2.5
V(RTAIL)

Figure 14. Duty Cycle vs. V(RTAIL)

ï40 ï20 0 40 60 80 100 140
TEMPERATURE (°C)

Figure 15. Duty Cycle vs. Temperature

TYPICAL CHARACTERISTICS

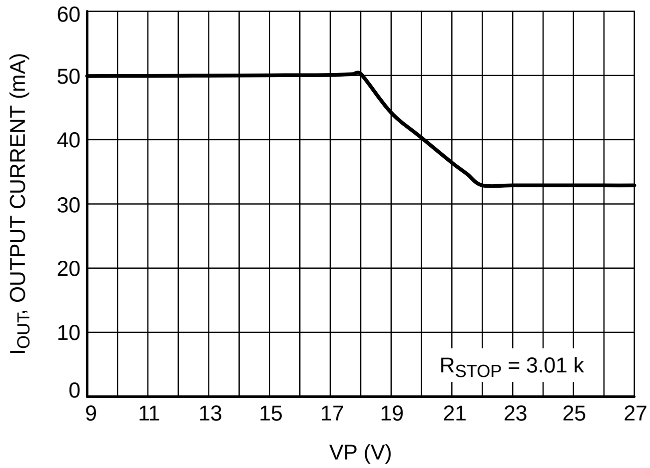


Figure 16. I $_{OUT}$ vs. VP

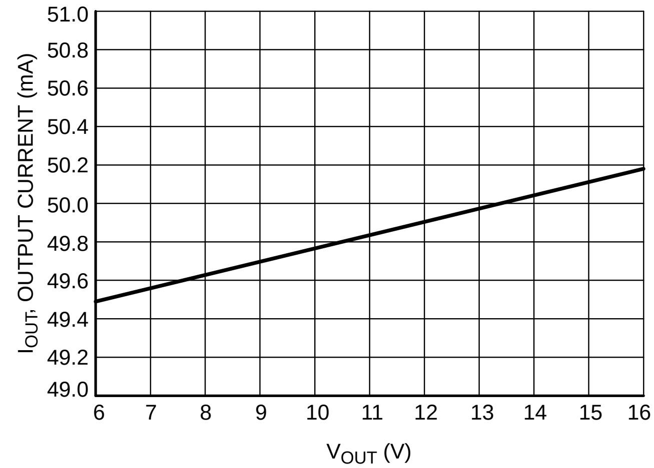


Figure 17. I $_{OUT}$ Line Regulation

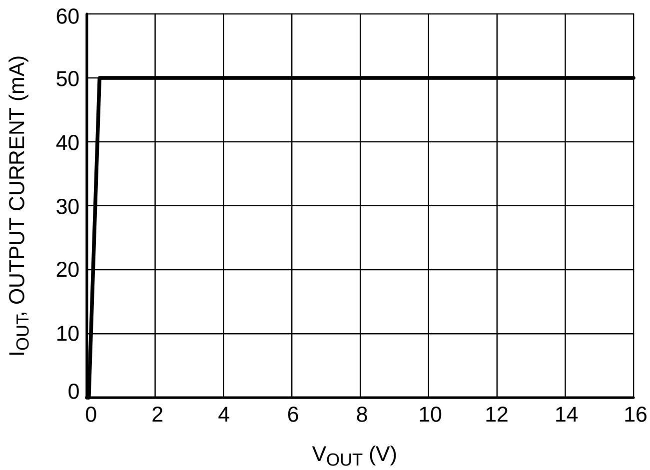


Figure 18. I $_{OUT}$ vs. V $_{OUT}$

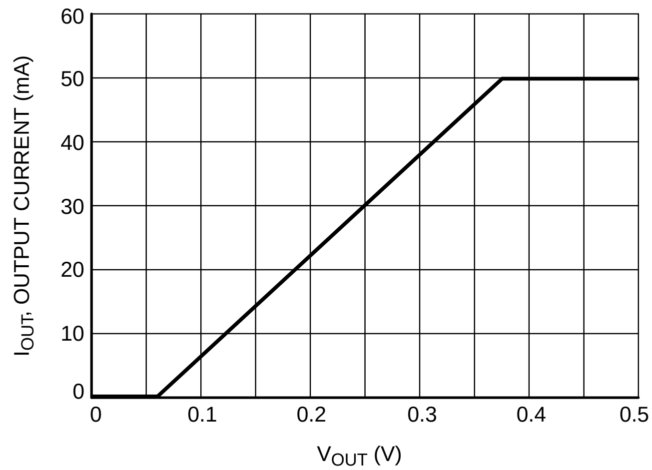


Figure 19. I $_{OUT}$ vs. V $_{OUT}$

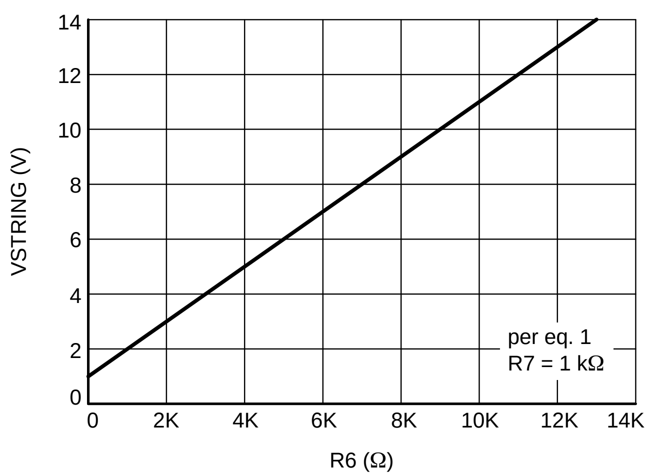


Figure 20. VSTRING vs. R6

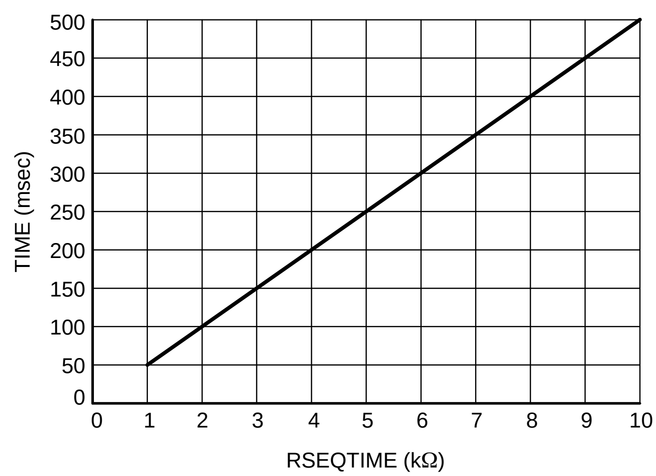


Figure 21. (Sequence Time / Re ïEnable Time) vs. RSEQTIME

TYPICAL CHARACTERISTICS

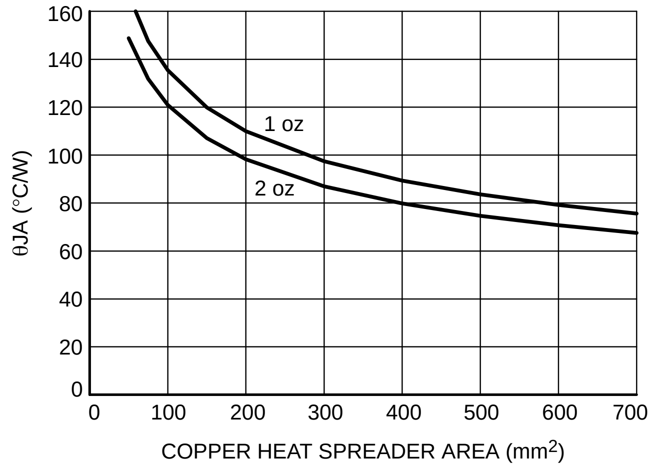


Figure 22. θ_{JA} Copper Spreader Area

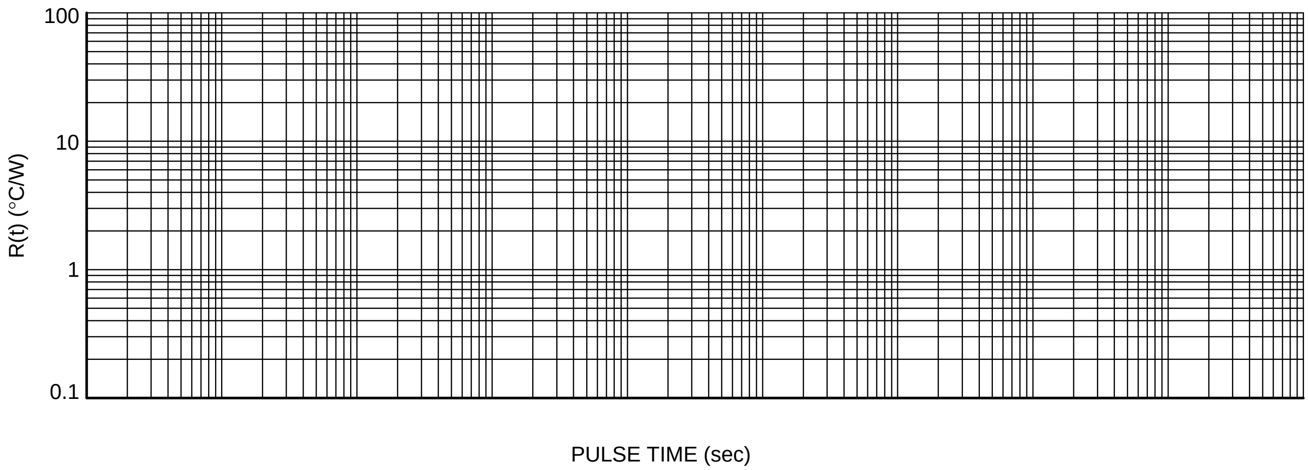


Figure 23. Thermal Duty Cycle Curves on 645 mm^2 Spreader Test Board

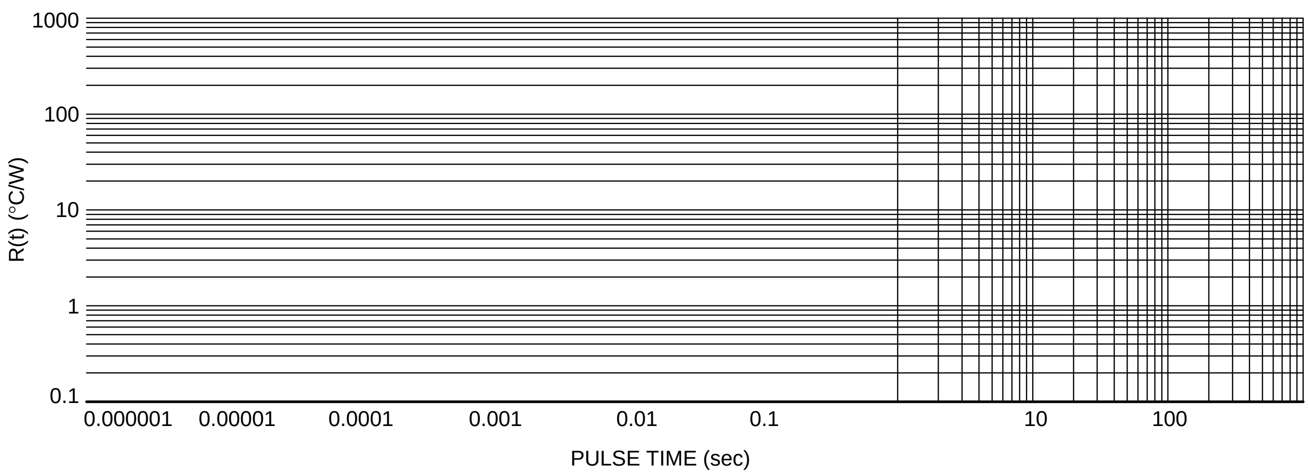


Figure 24. Single Pulse Heating Curve

Unused Outputs

Unused outputs should be shorted to ground. The NCV7683 detects the condition during power-up using the open load disable threshold and disables the open circuit detection circuitry. The timing diagrams below highlight the impacts in time with the sequencing function when an output is not used. In this example (Figures 26 and 27), OUT7 is not used and is grounded with SEQ1=0 and SEQ2=0. The subsequent output (OUT8) has been pulled in (in time) as shown by the 1st arrow. The 2nd arrow shows the SEQOUT signal has also been pulled in (in time). For instances which are coupled with others (in time) (e.g. SEQ1=1 and SEQ2=0 with OUT7 GND), there is no change in the ensuing waveforms. Figure 27 shows there is no impact for channel 8 when OUT7 is not used.

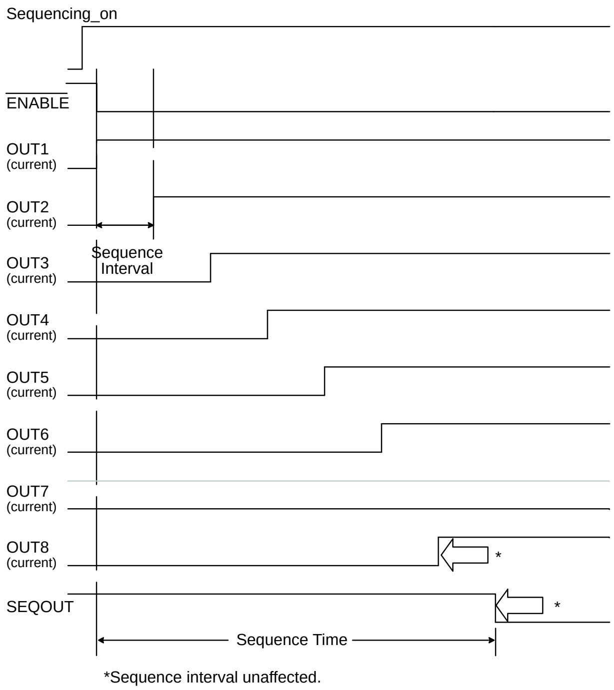


Figure 26. Unused Output time shift.
(SEQ1=0, SEQ2=0)

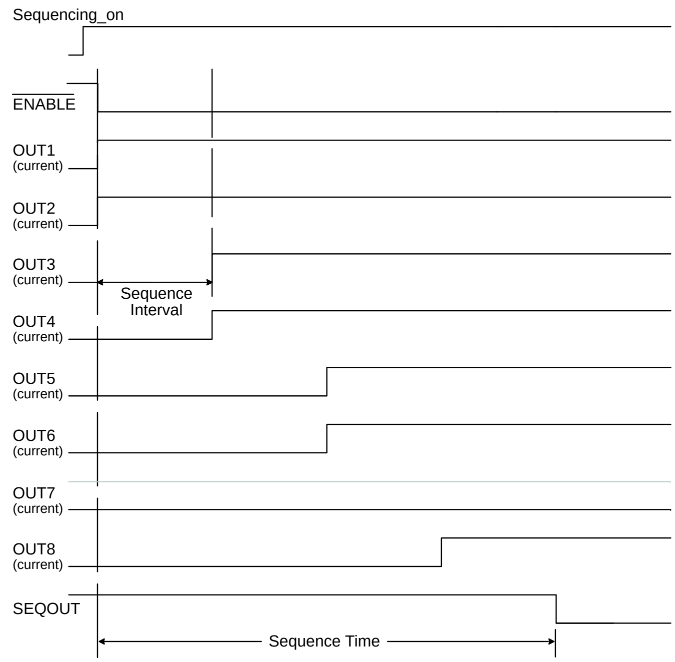


Figure 27. Unused Output No Time Shift.
(SEQ1=1, SEQ2=0)

Sequencing

Output sequencing is controlled by the SEQON, SEQTIME, SEQ1, and SEQ2 pins. The SEQON pin must be high to enable any of the sequencing functions. With the SEQON pin in a low state, all 8 outputs turn on at the same time and SEQOUT remains high all the time (via the external pull-up resistor). The SEQ1 and SEQ2 programming pins are utilized by grounding them or leaving them floating. They follow Table 6 (reference timing diagrams in Figure 7, Figure 8, Figure 9, and Figure 10). The sequence interval is defined by the delay of the $\overline{ENABLE}$ pin going low to OUT2 turning on (OUT1 turns on coincident with $\overline{ENABLE}$). The same sequence time interval is present for each additional sequential turn-on output of the IC.

Forcing an $\overline{ENABLE}$ high or SEQON low will cause a device which is operating in the sequence mode to leave the sequence mode. $\overline{ENABLE}$ going from low to high (Figure 28) will turn off all outputs. With SEQON going high to low (Figure 29 and Figure 30), operation will continue as a device which is not using the sequence mode feature. A device which was previously in TAIL mode (STOP=0) (Figure 29) will revert to TAIL mode. A device which was previously in STOP mode (STOP=1) Figure 30 will revert to STOP mode.

Before a sequence event, SEQOUT is high impedance.
After a sequence event, SEQOUT is high impedance.

Sequence and Re-Enable Time Programming

Sequence time is programmed using a resistor from the SEQTIME pin to ground. Figure 21 displays the expected time using the program resistor. Acceptable values for the resistor are between 1 K and 10 K. These provide 49 msec and 490 msec times respectively.

The Sequence Re-Enable Time uses the same internal timer as the Sequence Time. The Sequence Re-Enable Time is provided to prevent an immediate feedback triggering in a daisy chain setup. Reference Figures 33 and Figure 36 for details.

The program resistor used can be calculated by using the electrical parameters

1. Sequence Time / $R_{SEQTIME}$
2. Sequence Re-Enable Time / $R_{SEQTIME}$

$$\text{Sequence Time} = \frac{\text{Sequence\_Time}}{R_{SEQTIME}} \cdot R_{SEQTIME}$$

$$\text{Sequence ReEnable\_Time} = \frac{\text{Sequence ReEnable\_Time}}{R_{SEQTIME}} \cdot R_{SEQTIME}$$

Example:

Electrical Parameter (typ)

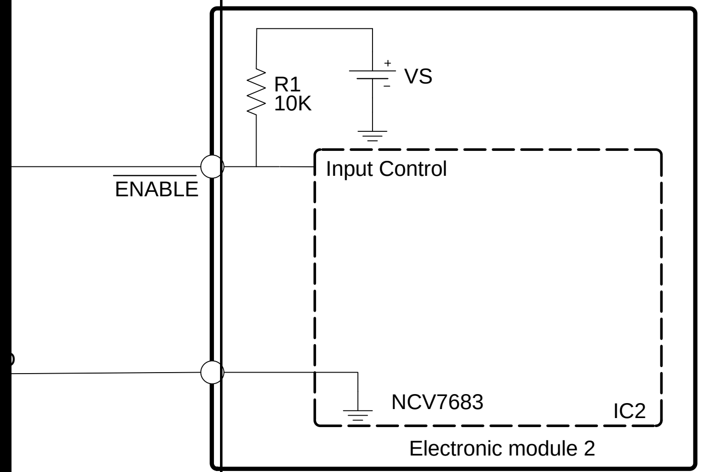
Sequence Time / $R_{SEQTIME}$ = 49 msec/kΩ

$R_{SEQTIME}$ = 1 kΩ

controllervia the DIAG pin, and turn off all driver ICs in the daisy chain eliminating any spurious lighting events.

SEQOUT is not active during STOP/TAIL modes (SEQOUT=0).

[redacted]



[redacted]terface between Multiple ICs

[redacted]	Fault State			
	Condition	DIAG	SEQOUT	Current Sources Status
	X	1	Hi Z	ALL OFF
	NORMAL	0	ACTIVE	SEQUENCING
	BIAS ERROR	1	ACTIVE	SEQUENCING
	OPEN CIRCUIT	1	ACTIVE	SEQUENCING
	TSD	1	Hi Z	ALL OFF
	OPEN CIRCUIT	1	Hi Z	ALL OFF
	SEQOUT OPEN	1	Hi Z	SEQUENCING
	NORMAL	0	0	ALL ON
	BIAS ERROR	1	0	ALL ON
	OPEN CIRCUIT	1	0	ALL ON
	TSD	1	0	ALL OFF
	OPEN CIRCUIT	1	0	ALL OFF
	NORMAL	0	0	ALL PWM
	BIAS ERROR	1	0	ALL PWM
	OPEN CIRCUIT	PWM	0	ALL PWM
	TSD	1	0	ALL OFF
	OPEN CIRCUIT			

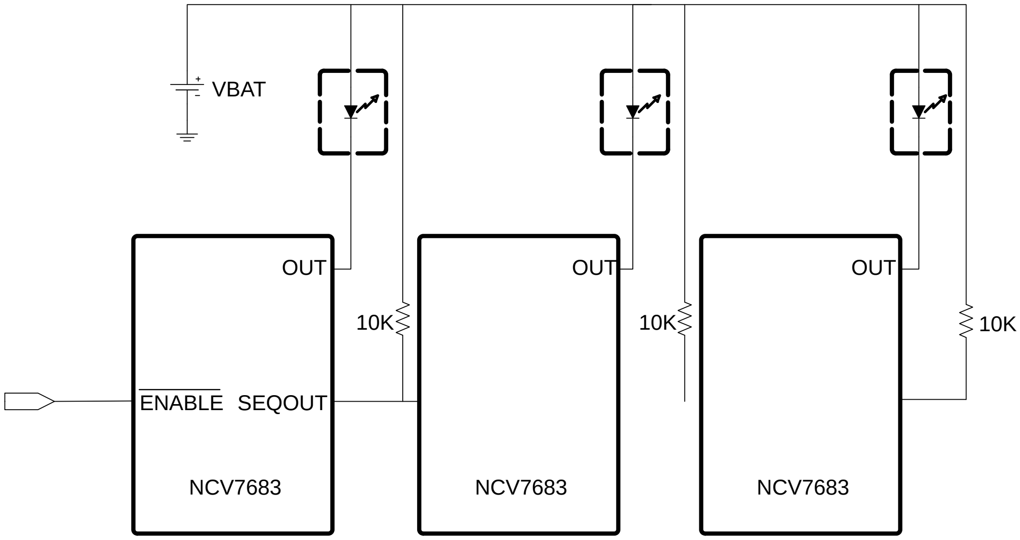


Figure 32. Daisy Chain Sequencing

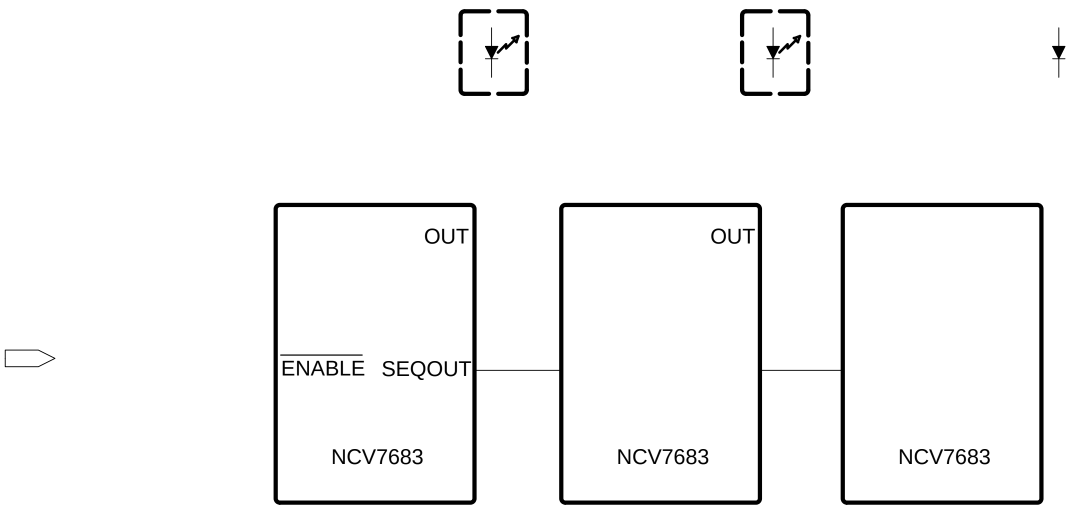


Figure 33. Retriggerable Daisy Chain Sequencing using the Sequence Re ïEnable Time

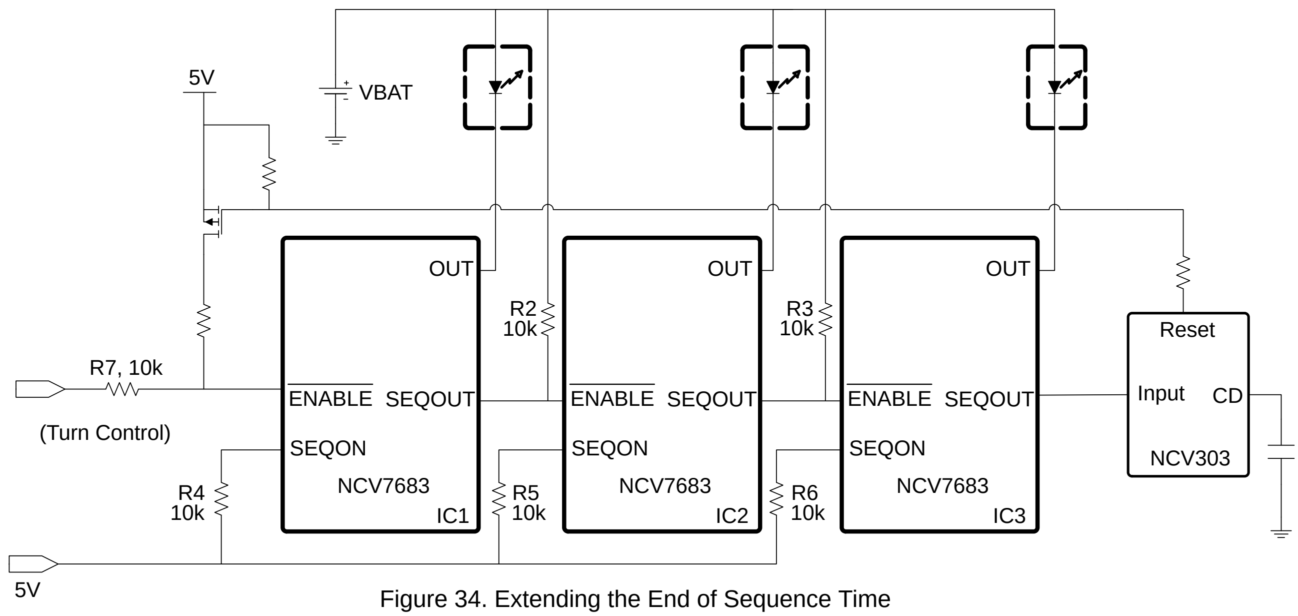


Figure 34. Extending the End of Sequence Time

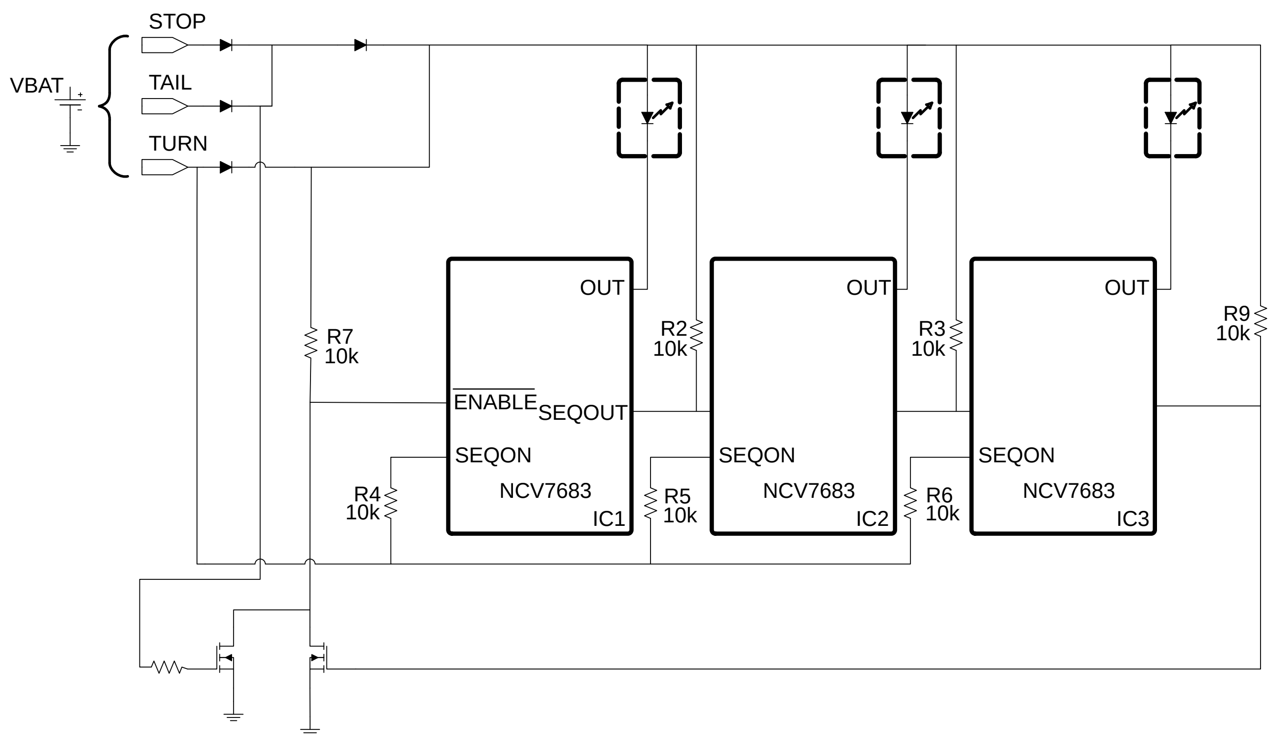


Figure 35. Alternate Retriggerable Daisy Chain Sequencing using Sequence Re ïEnable Time

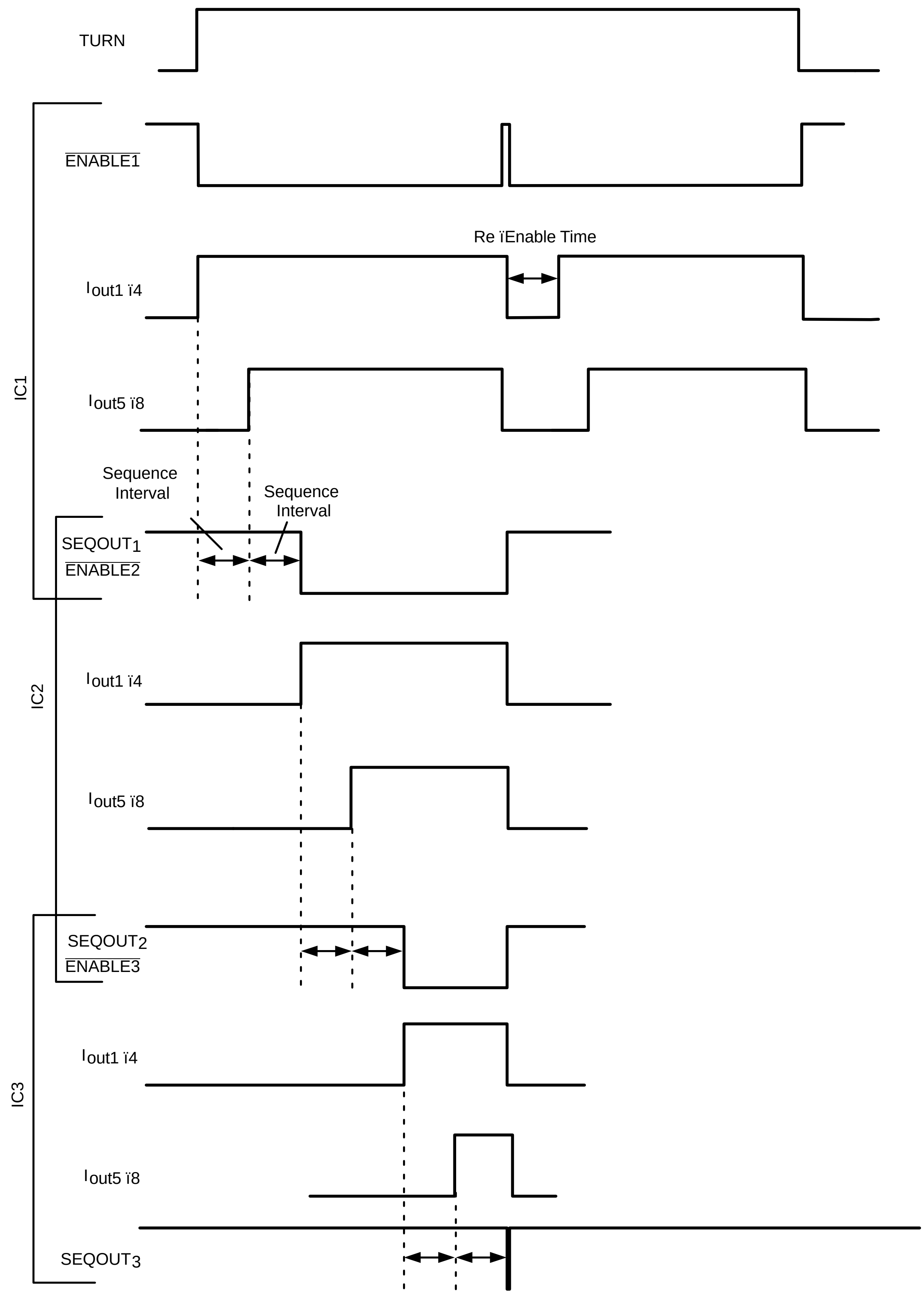


Figure 36. Sequencing Timing Diagram with Re ïEnable Time Delay

Programmability

Strings of LEDs are a common configuration for RCL applications. The NCV7683 provides eight matched outputs allowing individual string drive with current set by a single resistor. Output currents are mirrored and matched within ±4% at hot temperature.

A high STOP condition sets the output current using equation 1 below.

A low STOP condition, modulates the output currents at a duty cycle (DC) programmed using equation 2 below.

Note, current limiting on RSTOP limits the current which can be referenced from the RSTOP Pin. Exceeding the RSTOP Current Limit will set the output current to less than 100 mA, and the DIAG Pin will go high. This helps limit output current (brightness and power) for this type of fault.

The average ISTOP Duty Cycle current provides the dimmed tail illumination function and assures a fixed brightness level for tail. The PWM generator's fixed frequency (800 Hz typ.) oscillator allows flicker-free illumination. PWM control is the preferred method for dimming LEDs.

The diagnostic function allows the detection of an open in any one of the output circuits. The active-low diagnostic output (DIAG) is coincident with the STOP input and the ON state in the tail mode. DIAG remains high (pulled up) if an openload is detected in any LED string when STOP is high.

Output Current Programming

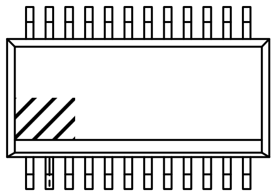
Reference Figure 11 (typ performance graph) to choose programming resistor (RSTOP) value for stop current. Reference Figure 13 Typical Performance Graph (Duty

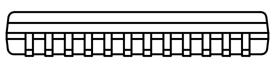
PACKAGE DIMENSIONS

PACKAGE DIMENSIONS

SSOP24 NB EP
CASE 940AQ
ISSUE O

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.10 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOO Tc6(T)0(MMC. DAMB613 cm 0)-20N THE LOWER RADIUS OF THE





	MILLIMETERS	
DIM	MIN	MAX
A		1.75
A1	0.00	0.10
b	0.1	0.30
c	0.0	0.20
e	0.65	
h	0.25	0.50
L	0.40	0. 5
L2	0.25	
M	0	

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Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
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