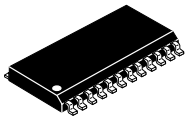
12 Channels 60 mA LED Linear Current Driver I²C Controllable for Automotive Applications

NCV7685



SSOP24−NB EP
CASE 940AQ

The NCV7685 consists of twelve linear programmable constant current sources with common reference. The part is designed for use in the regulation and control of LED for automotive applications. The NCV7685 allows 128 different duty cycle levels adjustable using pulse width modulation (PWM) independently for each output channel programmable via I²C serial interface. PWM frequency can be chosen in four different configurations up to 1200 Hz. The device can be used with micro−controller applications using the I²C bus or in stand−alone applications where a choice could be done in between two different static configuration settings. The IC also provides 3.3 V voltage reference to the application for loads up to 1 mA.

LED brightness level is easily programmed using an external resistor. Each channel has an internal circuitry to detect open−load conditions with an optional auto−recovery mode. If one driver is in open−load condition, all other channels could be turned off according to the programmable bit setting.

The device is available in small body size SSOP24−EP package.

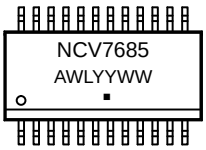
Features

- 12 Common Current Programmable Sources up to 60 mA
- Independent PWM Duty Cycle Control for each Channel via PC
- Common PWM Duty Cycle Control via I²C
- On−Chip 150, 300, 600 and 1200 Hz PWM
- Open LED String Diagnostics
- Low Dropout Operation for Pre−Regulator Applications
- Single Resistor for Current Set Point
- Voltage Reference 3.3 V/1 mA
- 8 Bits I²C Interface with CRC8 Error Detection
- OTP Bank for Stand−Alone Operation (2 Configurations)
- Output Enable Pin
- Detection and Protection Against Open Load and Under−Voltage
- Over Temperature Detection and Protection
- Low Emission with Spread Spectrum Oscillator
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- SSOP24−EP Packaging

Applications

- Dashboard Applications
- Rear Combination Lamps (RCL)
- Daytime Running Lights (DRL)
- Fog Lights
- Center High Mounted Stop Lamps (CHMSL) Arrays
- Turn Signal and Other Externally Modulated Applications

MARKING DIAGRAM



NCV7685 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NCV7685DQR2G	SSOP24−EP (Pb−Free)	2500/ Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

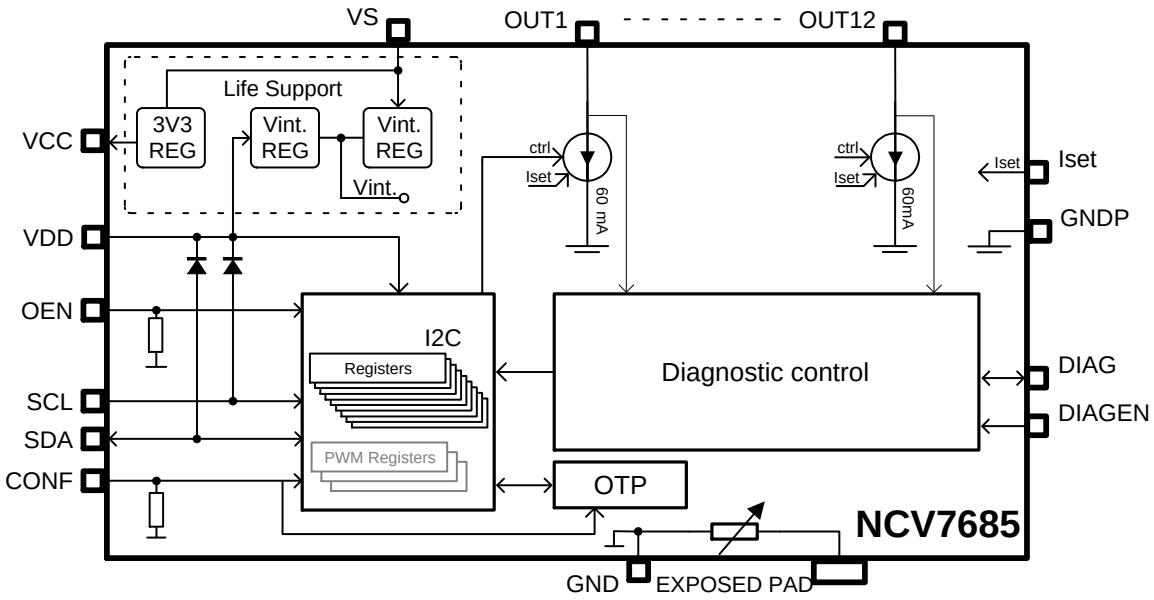


Figure 1. Block Diagram

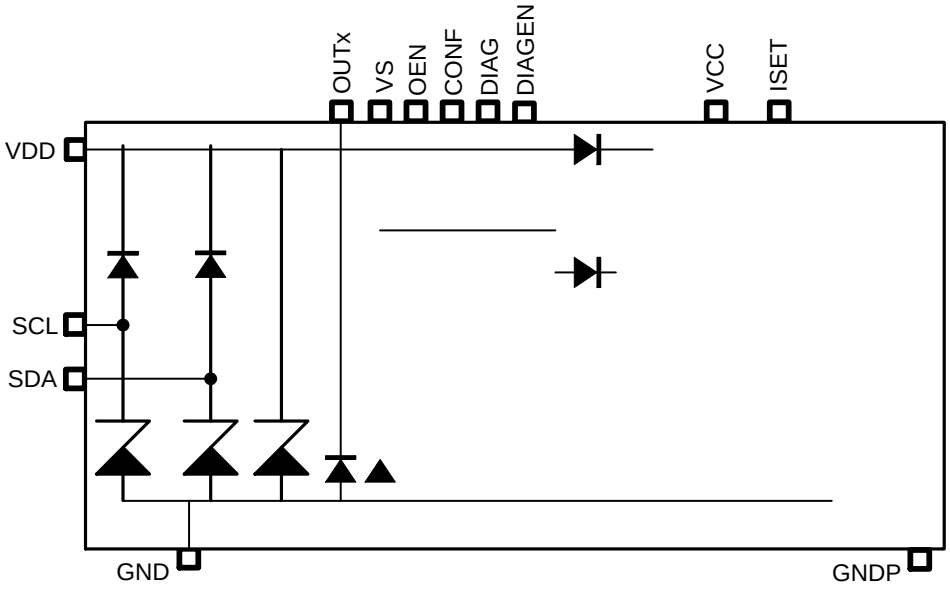


Figure 2. ESD Schematic

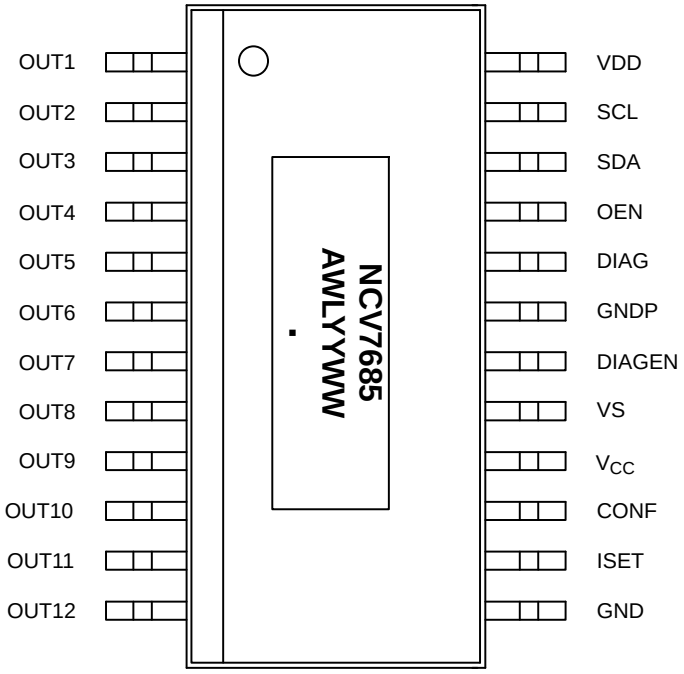


Figure 3. Pinout Diagram

Figure 4. Application Diagram with Micro−controller (I^2C Mode)

Table 5. ELECTRICAL CHARACTERISTICS (continued)
(5 V < VS < 18 V, 3.15 V < VDD < 5.5 V, R1 = 1.82 kΩ, −40 C T_J 150 C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CURRENT SOURCE OUTPUTS						
Output current	IOUThot	OUTx = 1 V, T_J = 150 C	50	55	60	mA
	IOUTcold	OUTx = 0.5 V, T_J = −40 C	50	55	60	mA
Current Matching from channel to channel	ImatchCold	T_J = −40 C (Note 10)	−7	0	7	%
	Imatch	T_J = 25 C (Note 10)				

Table 5. ELECTRICAL CHARACTERISTICS (continued)
(5 V < VS < 18 V, 3.15 V < VDD < 5.5 V, R1 = 1.82 kΩ, −40 C T_J 150 C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Setup−up Time to 90% of the ISET Regulated Value	tsetupISET	VS > 5 V	−	−	50	μs
INTERNAL PWM CONTROL UNIT (OUT1− OUT12)						
PWM1 Frequency, I^2C Mode	PWM1	Configuration Via I^2C	132	150	168	Hz
PWM2 Frequency, I^2C Mode	PWM2	Configuration Via I^2C	264	300	336	Hz
PWM3 Frequency, I^2C Mode	PWM3	Configuration Via I^2C	528	600	672	Hz
PWM4 Frequency, I^2C Mode	PWM4	Configuration Via I^2C	1056	1200	1344	Hz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 6. THERMAL WARNING AND THERMAL SHUTDOWN PROTECTION

Symbol

Power Supply and Voltage Reference (VS, V_{CC}, V_{DD})

VS is the analog power supply input of the device. VS supply is monitored with respect to the crossing of VSUV level (typ. 4.1 V). When VS rises above VSUV, the device starts the power−up state. When VS is above the VS_OP minimum level (typ. 5 V), the device can work properly.

VCC is a voltage reference providing 3.3 V derived from the VS main supply. It is able to deliver up to 1 mA and is primarily intended to supply 3.3 V loads. If VCC output reference is not used, then the VCC capacitor can be omitted.

VDD is the digital power supply input of the device.

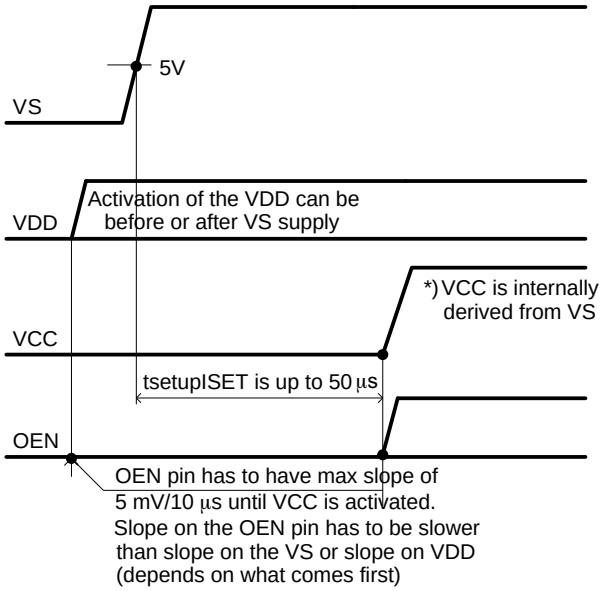


Figure 7. Power−up Sequence for OEN pin

Ground Connections (GND: Pin 13 and GNDP Pin 19)

The device ground connection is split to two pins called GND and GNDP. Both pins have to be connected on the application PCB.

Chip Select for OTP Programing (Using I_{SET})

The device can be programmed using the I^2C bus in End of Line cases. When the voltage on the ISET pin is pulled higher than 2.5 V, the device can be set in OTP control mode via the I^2C bus. During normal mode where only an external ISET resistor is connected to the I_{SET} pin, the access to the OTP registers is not possible. Zapping is only possible with VS above 13 V. The outputs are disabled as soon as 2.5 V is applied to the ISET pin. After the ID_LOCK_OTP I2C message is properly received, no further OTP zapping is possible.

Output Enable (OEN)

When the OEN input voltage is high, all output channels are programmed according to the I2C or SAM configuration. When OEN voltage is b d 1.758 1.6

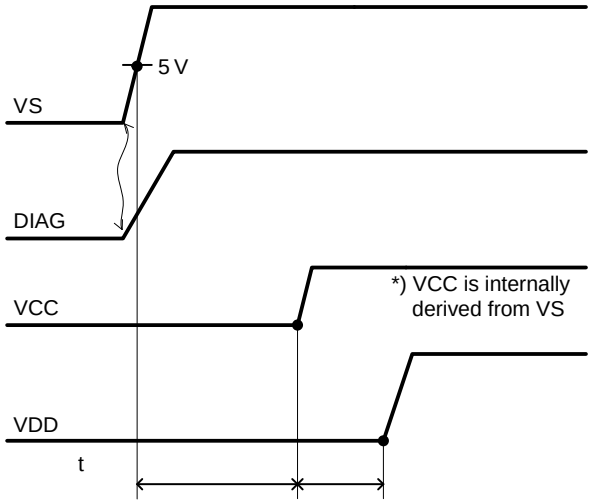


Figure 8. Power−up Sequence for DIAG pin. VS is supplied first, VDD comes up later.

DIGITAL PART AND I2C REGISTERS

The I^2C bus consists of two wires, serial data (SDA) and serial clock (SCL), carrying information between the devices connected on the bus. Each device connected to the bus is recognized by a unique address. The NCV7685 can both receive and transmit data with CRC8 error detection algorithm.

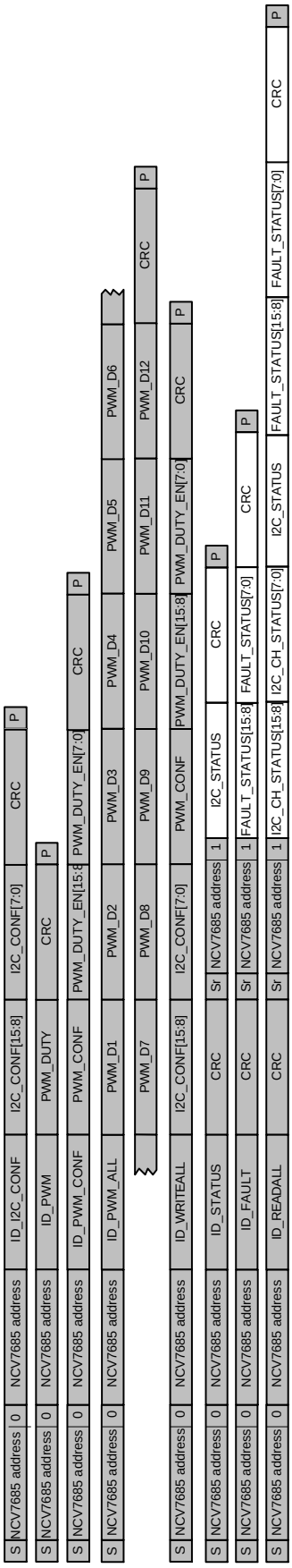


Figure 13. Format of I2C Frames

Figure 14. Format of I2C OTP Frames

There is a safety mechanism implemented by repeating the address. Since the I^2C address is 7 bits long, first bit of the second address byte starts with a “0” in the repeated byte (see tables below).

Table 8.

1st byte							
7	6	5	4	3	2	1	0
I^2C device Address							R/W Bit
2nd byte							
7	6	5	4	3	2	1	0
I^2C device Address							0

CRC ERROR DETECTION ALGORITHM

The CRC protection is turned off by default. It can be enabled by activation of the OTP ERREN bit (ERREN = 1). The every I^2C byte including both addresses with R/W flag are calculated using CRC8 algorithms. The CRC polynomial is following: $x^8 + x^5 + x^3 + x^2 + x + 1$.

Example of the CRC used in the I^2C message with I2C_CONF byte = 0xCFFF and with I^2C address 0x60 (0xC0) is 0x2E.

HARD CODING REGISTERS

Table 9. HARD CODING REGISTERS

Bit	**D7**

Table 11. SAM_CONF

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SAM_CONF_1																
Access type	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit name	–	–	–	–	SAM1conf[11:0]											
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SAM_CONF_2																
Access type	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit name	–	–	–	–	SAM2conf[11:0]											
Reset value	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	

SC_Iset: SC_Iset = 1 means there is short−circuit on the external resistor on I_{SET} pin and drivers are switched OFF and DIAG pin is set. SC_Iset=0 no short−circuit.

I2Cerr: I2Cerr=1 means an error has been detected during the I2C communication, I2Cerr=0 means no error during I2C communication has been detected.

UV: the device is in under voltage condition (VS is below VSUV threshold, all channels OFF).

diagRange: when diagRange = 1 the divided voltage is above the typical value of 2 V (LED diagnostic is enabled), diagRange = 0 means the divided voltage is below the typical value of 2 V (LED diagnostic is disabled).

TW: when TW=1 the device is in the thermal warning range (typ 140 C), this flag is just a warning no action is foreseen on the output drivers. TW=0 means the device is below the thermal warning range.

TSD: when TSD = 1 the device is in the Thermal shutdown range, TSD = 0 means the device is below the thermal shutdown range.

DIAGERR: DIAGERR = 1 means an error is detected by DIAG pin forced externally.

OL: OL = 1 means at least one channel is in Open Load condition, OL = 0 no Open Load.

Table 14.

SC_Iset	set when a short−circuit on the external resistor on I_{SET} pin, latched if permanent after 10 μs. Reset in case of short−circuit disappear permanently for at least 10μs.
I2Cerr	set if an error has been detected during the I2C communication. Reset on register reading.
UV	set when device is in under voltage condition (VS is below VSUV, all channels OFF).
diagRange	set when divided voltage is above the VDiagenTH threshold. Reset when the divided voltage is below the VDiagenTH threshold.
TW	set when junction temperature is above the Tjwar_on threshold. Reset on register reading AND temperature is below the (Tjwar_on − Tjsd_hys) threshold
TSD	set when junction temperature is above the TSD threshold. Reset on register reading AND temperature is below the TSD − Tjsd_hys) threshold
DIAGERR	set by DIAG pin forced low externally, latched if permanent after 10 μs. Reset in case DIAG pin is not forced permanently for at least 10 μs.
OL	set in Open Load condition and DIAGEN is high, latched if permanent after 10 μs. Reset if Open Load disappear permanently for at least 10 μs. Fault information is maintained on falling DIAGEN threshold exceeded

Table 15. I2C_CH_STATUS

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit name	I2CFLAG	I2CautoR	I2CdOnly	PWMEN	I2C_CH_STATUS[11:0]											
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

I2CFLAG: same as I2C_CONF register

I2CautoR: same as I2C_CONF register

I2CdOnly: same as I2C_CONF register

PWMEN: same as I2C_CONF register

I2C_CH_STATUS[11:0]: same as I2C_CONF[11:0] bits in I2C mode or same as SAM_CONF_1[11:0], SAM_CONF_2[11:0] bits in Standalone mode.

Remark: When NCV7685 is configured in I2C mode and output channel OUTx is configured to operate in PWM mode, I2C_CH_STATUS[x] shall contain value ‘1’.

Table 16. FAULT_STATUS

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit name	−	−	−	−	FAULT[11:0]											
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FAULT[11:0]: when FAULT[x] = 1 the OUTx channel is in fault mode (Open Load latched when the duration is longer than 10 μs), when FAULT[x] = 0 the OUTx channel is working properly. The register is reset on each read operation.

Table 17. PWM_DUTY

Bit	D7	D6	D5	D4	D3	D2	D1	D0

Table 20. PWM_CONF

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Access type	W	W	W	W	W	W	W	W
Bit Name	−	−	−	−	−	PWMLIN	PWMF2	PWMF1
Reset Value	0	0	0	0	0	0	0	0

PWMLIN bit shall select between between logarithmic (PWMLIN=0) and linear (PWMLIN=1) translation of PWMDUTY bits to duty cycle of internal PWM signal.

PWMF2 and *PWMF1* bits set typical PWM frequency settings according to the Table 21.

Table 21. TYPICAL PWM FREQUENCY SETTINGS

PWMF2	PWMF1	typ. PWM frequency [Hz]
0	0	150
0	1	300
1	0	600
1	1	1200

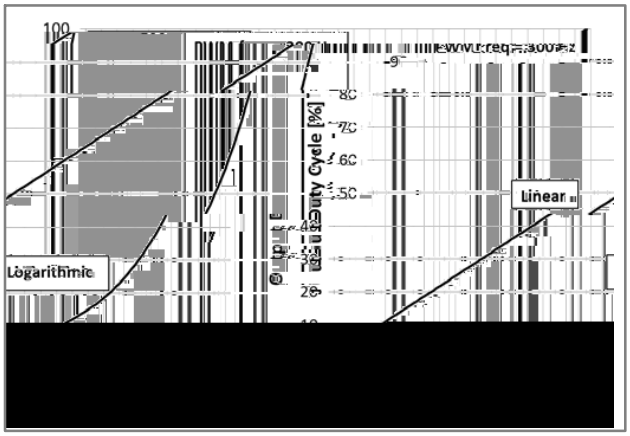


Figure 15. Output Duty Cycle vs. Register Setting

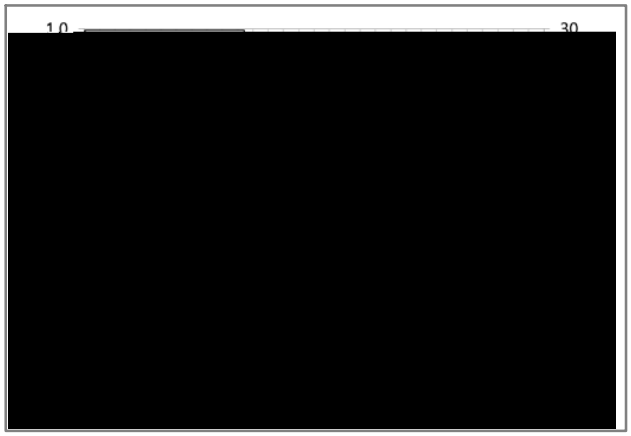
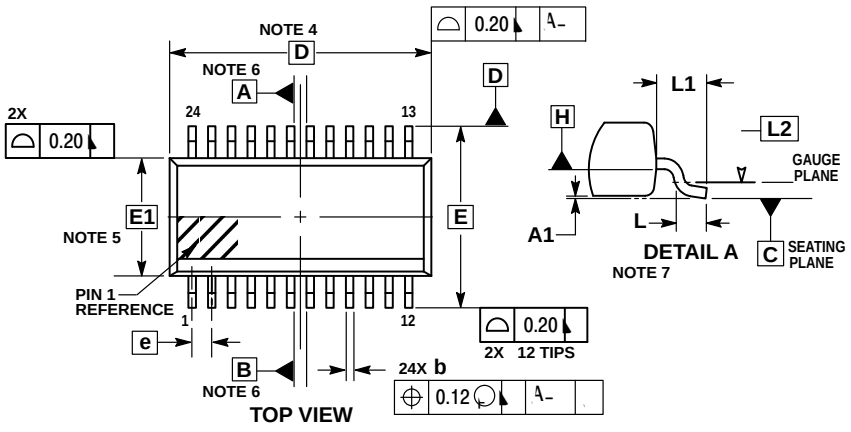


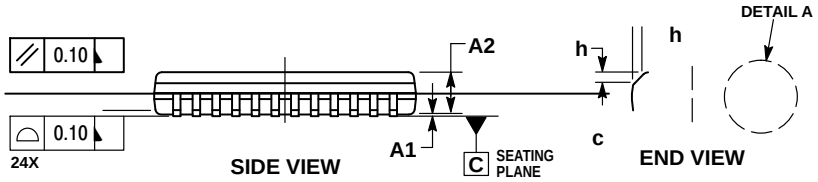
Figure 16. Output Duty Cycle vs. Register Setting − Detail

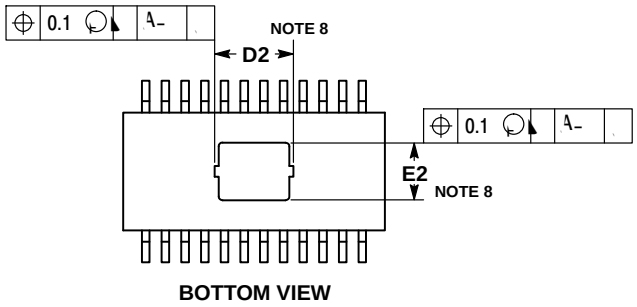
SSOP−24 NB EP
CASE 940AQ
ISSUE O

DATE 18 AUG 2017

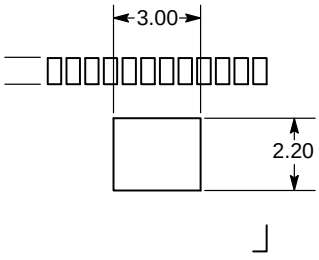
SCALE 1:1







RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.10 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. DIMENSION b APPLIES TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D IS DETERMINED AT DATUM PLANE H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM PLANE H.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. CONTOURS OF THE THERMAL PAD ARE UNCONTROLLED WITHIN THE REGION DEFINED BY DIMENSIONS D2 AND E2.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.
A1	0.00	0.10
A2	1.10	16
b	0.1	0. 0
c	0.0	0.20
D	6	
D2	2. 0	2. 0
E	6 .00	
E1	. 0	
E2	1. 0	2.00
e	06	
h	0.2	0. 0
L	0. 0	0.
L1	1.00	
L2	0.2	
M	0°	°

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.