NCV7703B

T H -B D SPI C

The NCV7703B is a fully protected Triple Half−Bridge Driver designed specifically for automotive and industrial motion control applications. The three half−bridge drivers have independent control. This allows for high side, low side, and H−Bridge control. H−Bridge control provides forward, reverse, brake, and high impedance states. The drivers are controlled via a standard Serial Peripheral Interface (SPI). This device is fully compatible with ON Semiconductor's NCV7708 Double Hex Driver.

Features

- Ultra Low Quiescent Current in Sleep Mode, 1 □A for V_S and V_{CC}
- Power Supply Voltage Operation down to 5 V
- 3 High−Side and 3 Low−Side Drivers Connected as Half−Bridges
- Internal Free−Wheeling Diodes
- Configurable as H−Bridge Drivers
- 0.5 A Continuous (1 A peak) Current
- $R_{DS(on)}$ = 0.8 □ (typ)
- 5 MHz SPI Control with Daisy Chain Capability
- Compliance with 5 V and 3.3 V Systems
- Overvoltage and Undervoltage Lockout
- Fault Reporting
- 1.4 A Overcurrent Threshold Detection with Optional Shutdown
- 3 A Current Limit with Auto Shutdown
- Overtemperature Warning and Protection Levels
- Internally Fused Leads in SOIC−14 Package for Better Thermal Performance
- ESD Protection up to 6 kV
- These are Pb−Free Devices

Typical Applications

- Automotive
- Industrial
- DC Motor Management

March, 2017 − Rev. 4
Publication Order Number:
NCV7703B/D

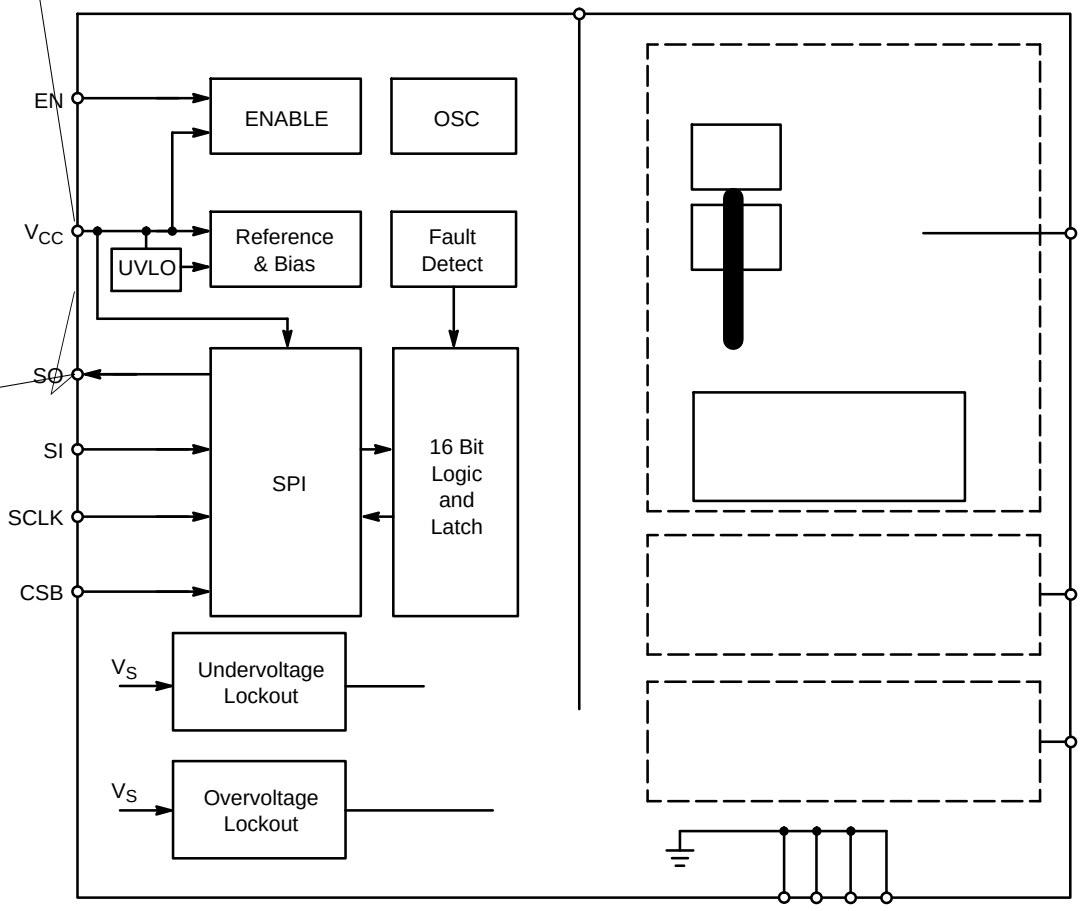


Figure 2. Block Diagram

MAXIMUM RATINGS

Rating	Value	Unit
Power Supply Voltage (V_S) (DC) (AC), t < 500 ms, Ivs > −2 A	 −0.3 to 40 −1	V
Output Pin OUTx (DC) (AC), t < 500 ms, IOUTx > −2 A	 −0.3 to 40 −1	V
Pin Voltage (Logic Input pins, SI, SCLK, CSB, SO, EN, V_{CC})	−0.3 to 7	V
Output Current (OUTx) (DC) (AC) (50 ms pulse, 1 s period)	 −1.8 to 1.8 Internally Limited	A
Electrostatic Discharge, Human Body Model, V_S, OUT1, OUT2, OUT3 (Note 3)	6	kV
Electrostatic Discharge, Human Body Model, all other pins (Note 3)	2	kV
Electrostatic Discharge, Machine Model, V_S, OUT1, OUT2, OUT3 (Note 3)	300	V
Electrostatic Discharge, Machine Model, all other pins (Note 3)	200	V
Operating Junction Temperature	−40 to 150	°C
Storage Temperature Range	−55 to 150	°C
Moisture Sensitivity Level (MAX 260°C Processing)	MSL3	−

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Thermal Parameters	Test Conditions (Typical Value)		Unit
14 Pin Fused SOIC Package	min−pad board (Note 1)	1″ pad board (Note 2)	
Junction−to−Lead (psi−JL8, Ψ_{JL8}) or Pins 1, 7, 8, 14	23	22	°C/W
Junction−to−Ambient ($R_{\theta JA}$, Ψ_{JA})	122	83	°C/W

1. 1−oz copper, 67 mm^2 copper area, 0.062″ thick FR4.
2. 1−oz copper, 645 mm^2 copper area, 0.062″ thick FR4.
3. This device series incorporates ESD protection and is characterized by the following methods:
   ESD HBM according to AEC−Q100−002 (EIA/JESD22−A114)
   ESD MM according to AEC−Q100−003 (EIA/JESD22−A115)

ELECTRICAL CHARACTERISTICS

(−40°C ≤ T_J ≤ 150°C, 5.5 V ≤ V_S ≤ 40 V, 3 V ≤ V_{CC} ≤ 5.25 V, EN = V_{CC}, unless otherwise specified)

Characteristic		Conditions	Min	Typ	Max	Unit
GENERAL						
Supply Current (V_S) Sleep Mode (Note 5)		V_S = 13.2 V, OUTx = 0 V EN = SI = SCLK = 0 V, CSB = V_{CC} 0 V < V_{CC} < 5.25 V (T_J = −40°C to 85°C)	−	1.0	5.0	□A
		V_S = 13.2 V, OUTx = 0 V EN = SI = SCLK = 0 V, CSB = V_{CC} 0 V < V_{CC} < 5.25 V, T_J = 25°C	−	−	2.0	
Supply Current (V_S) Active Mode		EN = V_{CC}, 5.5 V < V_S < 35 V No Load	−	2.0	4.0	mA
Supply Current (V_{CC}) Sleep Mode (Note 6)		V_{CC} = CSB, EN = SI = SCLK = 0 V (T_J = −40°C to 85°C)	−	0	2.5	□A
Supply Current (V_{CC}) Active Mode		EN = V_{CC}	−	1.5	3.0	mA
V_{CC} Power−On−Reset Threshold			2.60	2.80	3.00	V
V_S Undervoltage Detection	Threshold Hysteresis	V_S decreasing	4.3 100	4.7 −	5.1 400	V mV
V_S Overvoltage Detection	Threshold Hysteresis	V_S increasing	34.0 1.5	37.5 3.5	40.0 5.5	V
Thermal Warning (Note 4)	Threshold Hysteresis		120 −	145 30	170 −	°C
Thermal Shutdown (Note 4)	Threshold Hysteresis		155 −	175 30	195 −	°C

Ratio of Thermal Shutdown to Thermal
W Tme552.189 ET516.3.0019 Tc(CC)Tj8 0 0 8 136.2Tture236 -1.1055 f444.54 414.97 395.986 .90707 ref230.74 415.3.43991071 24.945 ref230.754 414.97

ELECTRICAL CHARACTERISTICS

(−40°C ≤ T_J ≤ 150°C, 5.5 V ≤ V_S ≤ 40 V, 3 V ≤ V_{CC} ≤ 5.25 V, EN = V_{CC}, unless otherwise specified)

Characteristic		Conditions	Min	Typ	Max	Unit
OUTPUTS						
Source Leakage Current Sum of I(OUTx) x = 1, 2, 3		OUTx = 0 V, V_S = 40 V, EN = 0 V CSB = V_{CC} 0 V < V_{CC} < 5.25 V Sum(I(OUTx) OUTx = 0 V, V_S = 40 V, EN = 0 V CSB = V_{CC} 0 V < V_{CC} < 5.25 V, T_J = 25°C Sum(I(OUTx)	−5.0 −1.0	− −	− −	□A
Sink Leakage Current		OUTx = V_S = 40 V, EN = 0 V CSB = V_{CC} 0 V < V_{CC} < 5.25 V OUTx = V_S = 13.2 V, EN = 0 V CSB = V_{CC} 0 V < V_{CC} < 5.25 V, T_J = 25°C	− −	− −	300 10	□A
Over Current Shutdown Threshold	Source Sink		−1.8 1.0	−1.4 1.4	−1.0 1.8	A
Current Limit	Source Sink		−5.0 2.0	−3.0 3.0	−2.0 5.0	A
Under Load Detection Threshold	Source Sink		−15 3.0	−7.0 7.0	−2.0 15	mA
Power Transistor Body Diode Forward Voltage		I_f = 500 mA	−	0.9	1.3	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Thermal characteristics are not subject to production test
5. For temperatures above 85°C, refer to Figure 4.
6. For temperatures above 85°C, refer to Figure 5.

ELECTRICAL CHARACTERISTICS
(−40°C ≤

TYPICAL CHARACTERISTICS

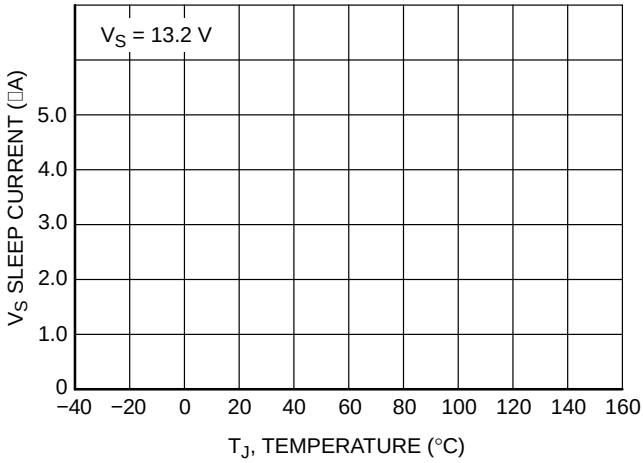


Figure 4. V_S Sleep Supply Current vs. Temperature

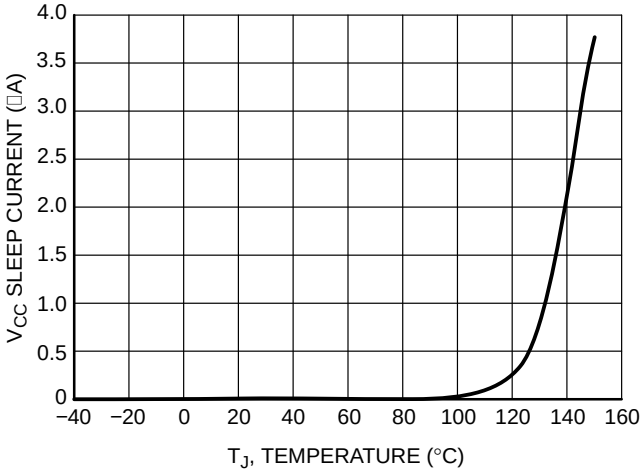
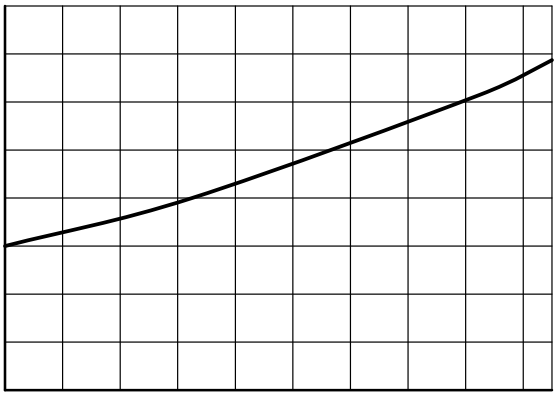
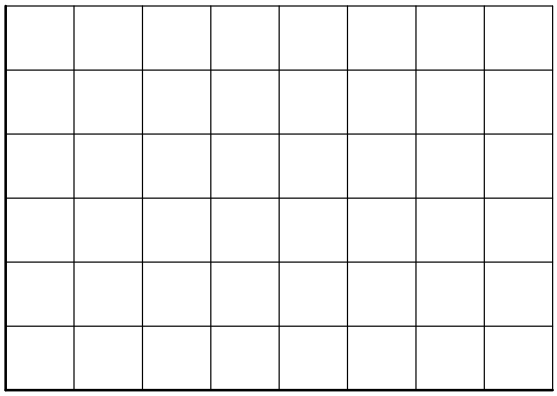


Figure 5. V_{CC} Sleep Supply Current vs. Temperature





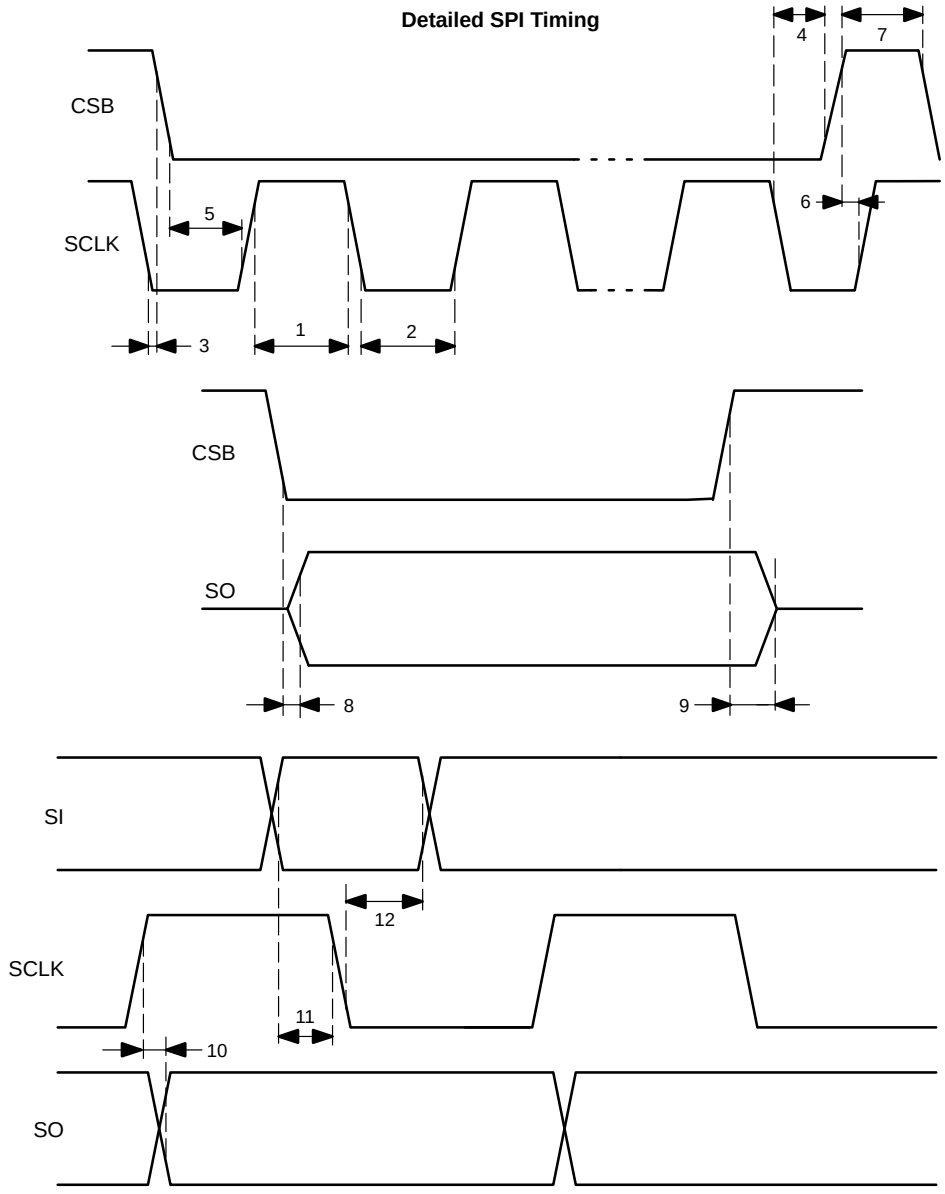


Figure 8. SPI Timing Waveforms

TYPICAL CHARACTERISTICS

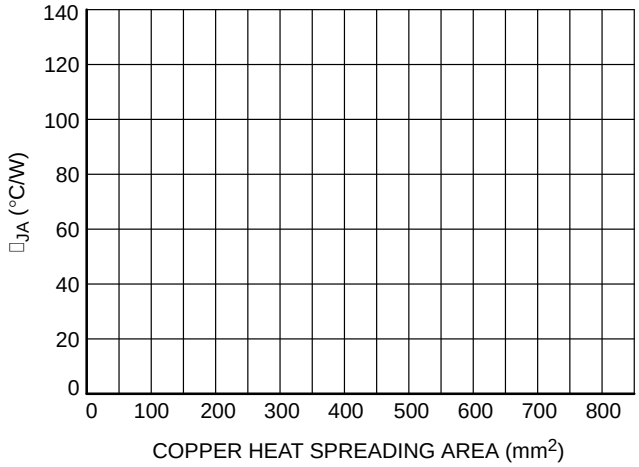


Figure 9. θ_{JA} vs. Copper Spreader Area, 14 Lead SON (fused leads)

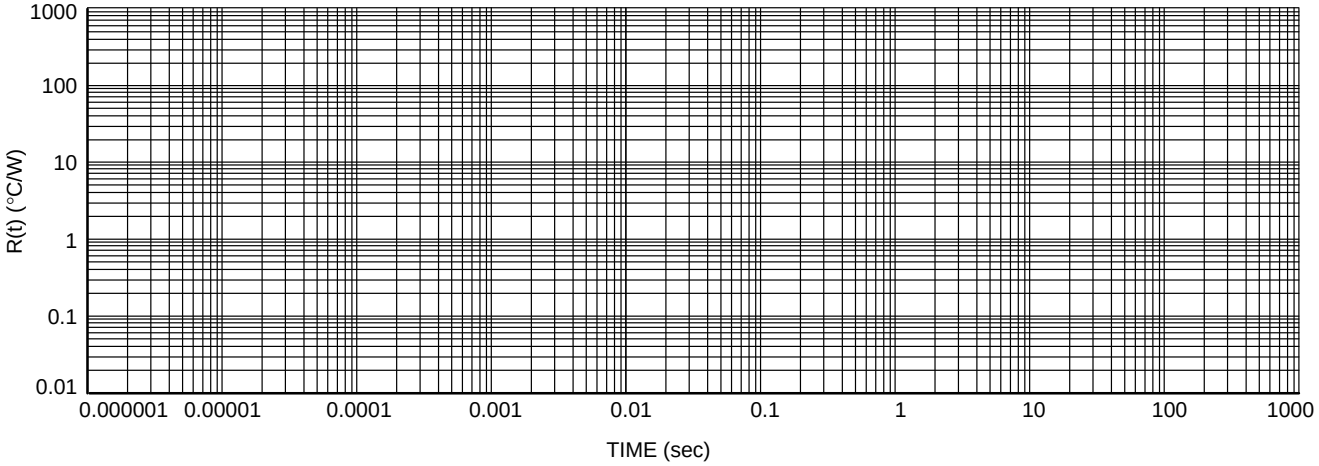


Figure 10. Transient Thermal Response to a Single Pulse 1 oz Copper (Log−Log)

Figure 11. Transient Thermal Response to a Single Pulse 1 oz Copper (Semi−Log)

SPI Communication

Standard 16−bit communication has been implemented to this IC to turn drivers on/off, and to report faults. (See Figure 13). The LSB (Least Significant Bit) is clocked in first.

Communication is Implemented as Follows:

1. CSB goes low to allow serial data transfer.
2. A 16 bit word is clocked (SCLK) into the SI (Serial Input) pin.
3. CSB goes high to transfer the clocked in information to the data registers.

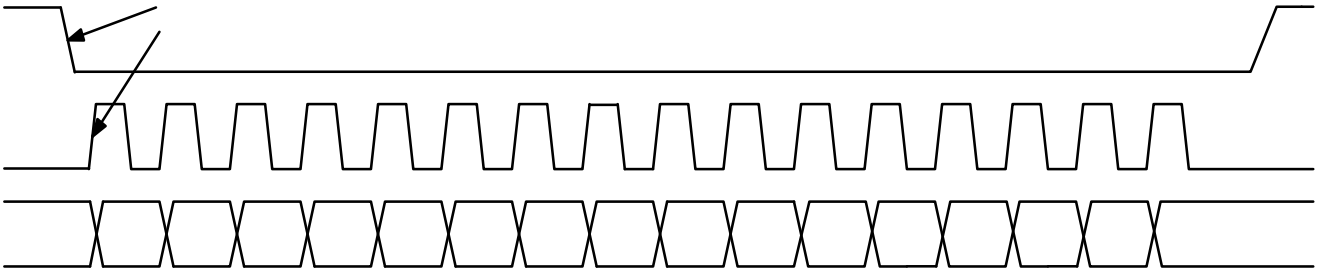
NOTE: SO is tristate when CSB is high.

Frame Detection

Input word integrity (SI) is evaluated by the use of a frame consistency check. The word frame length is compared to an x 16 bit acceptable word length before the data is latched into the input register. This guarantees the proper word length has been imported and allows for daisy chain operation applications.

The frame length detector is enabled with the CSB falling edge and the SCLK rising edge.

SCLK must be low during the CSB rising edge. The fault register is cleared with a valid frame detection. Existing faults are re−latched after the fault filter time.



H−Bridge Driver Configuration

The NCV7703B has the flexibility of controlling each half bridge driver independently. This allows for high side, low side and H−bridge control. H−bridge control provides forward, reverse, brake and high impedance states.

Overvoltage Clamping − Driving Inductive Loads

Each output is internally clamped to ground and Vs by internal free wheeling diodes. The diodes have ratings that

Thermal Shutdown

Three

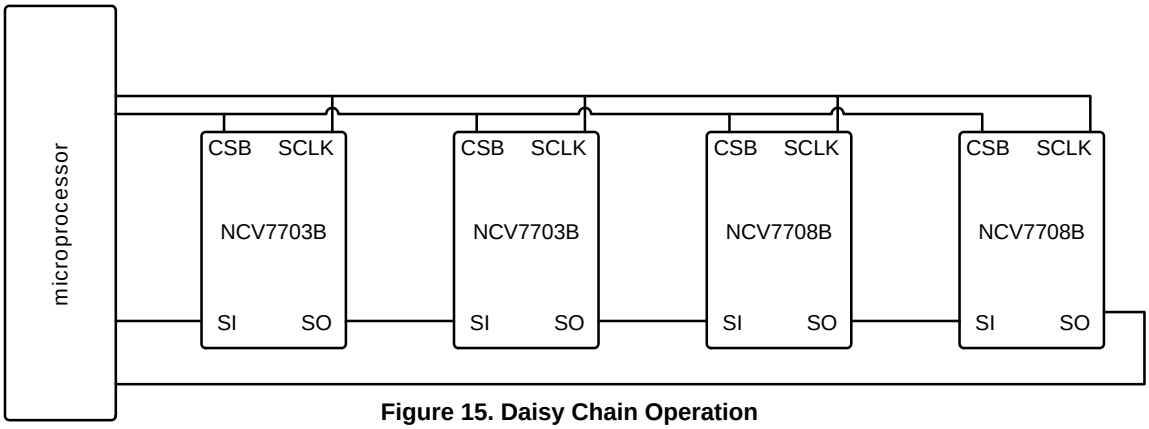
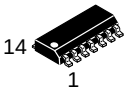


Figure 15. Daisy Chain Operation

Parallel Control

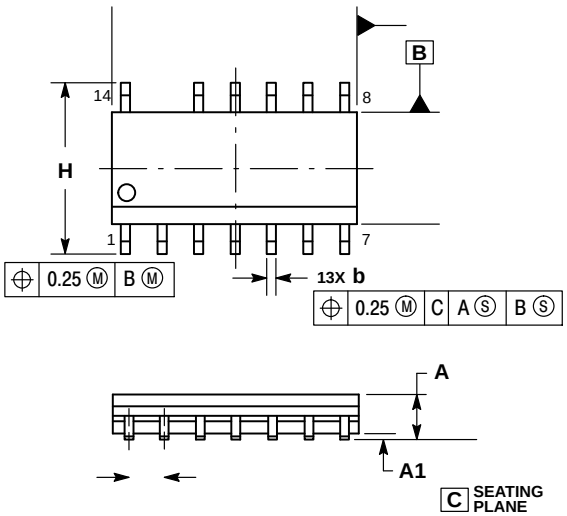
A more efficient way to control multiple SPI compatible devices is to connect them in a parallel fashion and allow each device to be controlled in a multiplex mode. The diagram below shows a typical connection between the microprocessor or microcontroller and multiple SPI compatible devices. In a daisy chain configuration, the programming information for the last device in the serial string must first pass through all the previous devices. The parallel



SCALE 1:1

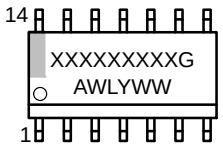
SOIC 14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

STYLES ON PAGE 2

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STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE