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SPI C

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DIAGRA

SOIC−14
D2 SUFFIX

NCV7703C

The NCV7703C is a fully protected Triple Half−Bridge Driver designed specifically for automotive and industrial motion control applications. The three half−bridge drivers have independent control. This allows for high side, low side, and H−Bridge control. H−Bridge control provides forward, reverse, brake, and high impedance states (with EN = 0). The drivers are controlled via a standard Serial Peripheral Interface (SPI).

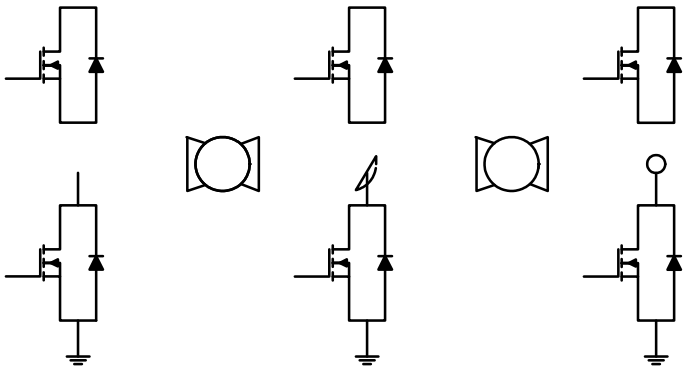
Features

- Ultra Low Quiescent Current in Sleep Mode, 1 μA for V_S and V_{CC}
- 3 High−Side and 3 Low−Side Drivers Connected as Half−Bridges
- Internal Free−Wheeling Diodes
- Configurable as H−Bridge Drivers
- 500 mA (typ), 1.1 A (max) Drivers
- $R_{DS(on)}$ = 0.8 Ω (typ), 1.7 Ω (max)
- 5 MHz SPI Control with Daisy Chain Capability
- Compliance with 5 V and 3.3 V Systems
- Overvoltage and Undervoltage Lockout
- Fault Reporting
- 1.45 A Overcurrent Threshold Detection
- 3 A Current Limit
- Shoot−Through Attempt Detection
- Overtemperature Warning and Protection Levels
- Internally Fused Leads in SOIC−14 for Better Thermal Performance
- ESD Protection up to 6 kV
- These are Pb−Free Devices

Typical Applications

- Automotive
- Industrial
- DC Motor Management

Figure 1. Cascaded Application



ORDERING INFORMATION

Device	Package	Shippi

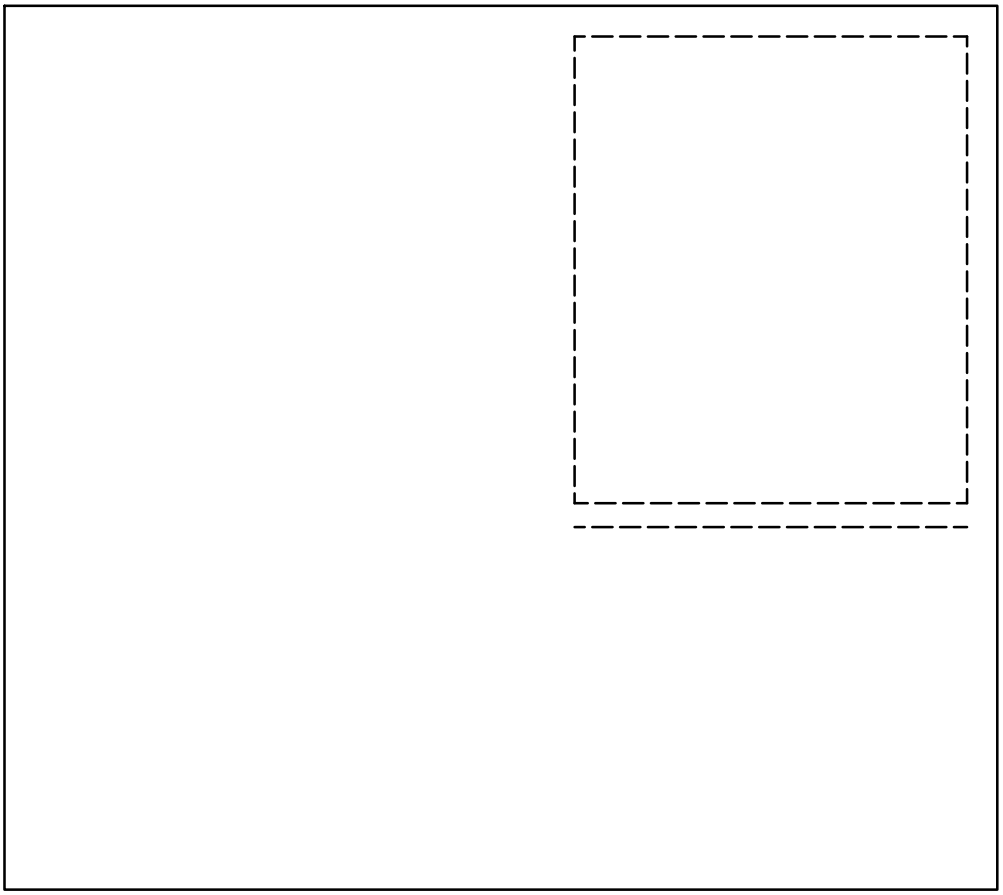


Figure 2. Block Diagram

MAXIMUM RATINGS

Rating	Value	Unit
–	– –	
–	– –	
	–	

ELECTRICAL CHARACTERISTICS

– ° ≤ ≤ ° ≤ ≤ ≤ ≤

Characteristic	Conditions	Min	Typ	Max	Unit
GENERAL					
		–			µ
	– ° °				
		–	–		µ
	°				
		–			
		–			µ
	– ° °				

ELECTRICAL CHARACTERISTICS

– ° ≤ ≤ ° ≤ ≤ ≤ ≤

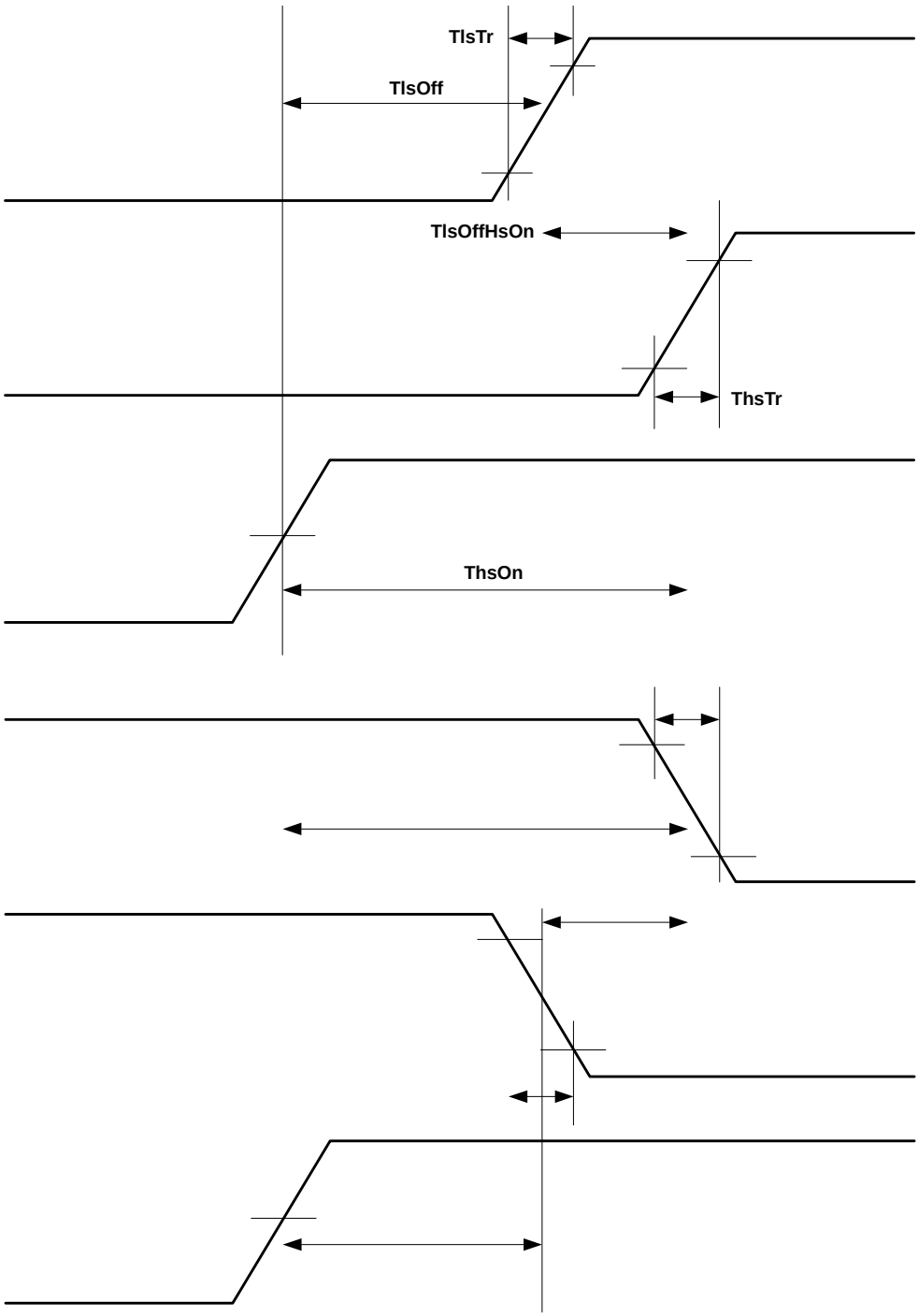
Characteristic	Conditions	Min	Typ	Max	Unit
OUTPUTS					
		–	–	–	

ELECTRICAL CHARACTERISTICS

– ° ≤ ≤ ° ≤ ≤ ≤ ≤

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
SERIAL PERIPHERAL INTERFACE						
		–	–	–		

CHARACTERISTIC TIMING DIAGRAMS



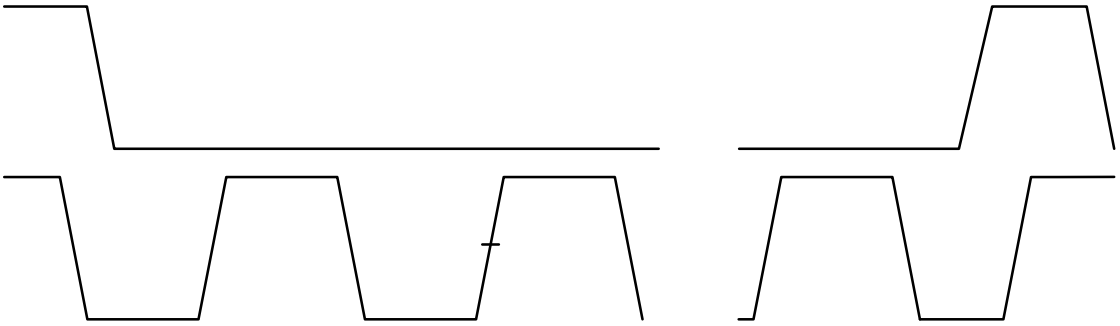


Figure 5. SPI Timing Diagram

SPI Communication

Standard 16−bit communication has been implemented to this IC to turn drivers on/off, and to report faults. (See Figure 12). The LSB (Least Significant Bit) is clocked in first.

Communication is Implemented as Follows:

1. CSB goes low to allow serial data transfer.
2. A 16 bit word is clocked (SCLK) into the SI (Serial Input) pin.
3. CSB goes high to transfer the clocked in information to the data registers.

NOTE: SO is tristate when CSB is high.

Frame Detection

Input word integrity (SI) is evaluated by the use of a frame consistency check. The word frame length is compared to an η x 16 bit acceptable word length before the data is latched into the input register. This guarantees the proper word length has been imported and allows for daisy chain operation applications.

The frame length detector is enabled with the CSB falling edge and the SCLK rising edge.

SCLK must be low during the CSB rising edge. The fault register is cleared with a valid frame detection. Existing faults are re−latched after the fault filter time.

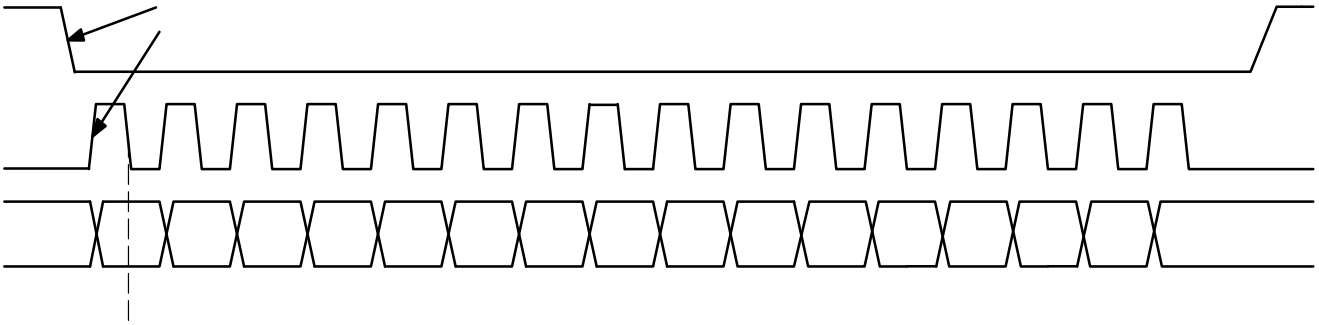


Table 1. SPI BIT DESCRIPTION

Input Data			Output Data		
Bit Number	**Bit Description**	**Bit Status**	**Bit Number**	**Bit Description**	**Bit Status**
		μ μ			
				−	

DETAILED OPERATING DESCRIPTION

General

The NCV7703C Triple Half Bridge Driver provides drive capability for 3 Half−Bridge configurations. Each output drive is characterized for a 500 mA load and has a typical 1.4 A surge capability. Strict adherence to integrated circuit die temperature is necessary, with a maximum die temperature of 150°C. This may limit the number of drivers enabled at one time. Output drive control and fault reporting are handled via the SPI (Serial Peripheral Interface) port.

An Enable function (EN) provides a low quiescent sleep current mode when the device is not being utilized. A pull down is provided on the EN, SI and SCLK inputs to ensure they default to a low state in the event of a severed input signal. A pull−up is provided on the CSB input disabling SPI communication in the event of an open CSB input.

Power Up/Down Control

A feature incorporated in the IC is an under voltage lockout circuit that prevents the output drivers from turning on unintentionally. V_{CC} and V_S are monitored for undervoltage conditions supporting a smooth turn−on transition. All drivers are initialized in the off (high impedance) condition, and will remain off during a V_{CC} or V_S undervoltage condition. This allows power up sequencing of V_{CC}, and V_S up to the user. Once V_{CC} is above the Power−On−Reset threshold, SPI communication can begin regardless of the voltage on V_S. The V_S supply input does not ever affect the SPI logic. However, drivers will remain off if V_S is in an undervoltage condition. Hysteresis in both V_{CC} and V_S circuits results in glitch free operation during power up/down.

Overvoltage Shutdown (Table 2)

Overvoltage lockout circuitry monitors the voltage on the V_S pin. The response to an overvoltage condition is selected by SPI input bit 15. PSF output bit 15 is set when a V_S overvoltage condition exists. If input bit 15 (OVLO) is set to “1”, all outputs will turn off during this overvoltage condition. Turn On/Off status is maintained in the logic circuitry, so that when proper input voltage level is reestablished, the programmed outputs will turn back on. The PSF output bit is reset with SRR = 1.

Table 2. INPUT BIT 15, OVERVOLTAGE LOCK OUT (OVLO) SHUT DOWN

OVLO Input Bit 15	V_S OVLO Condition	Output Data Bit 15 Power Supply Fail (PSF) Status	OUTx Status

H−Bridge Driver Configuration

The NCV7703C has the flexibility of controlling each half bridge driver independently. This allows for high side, low side and H−bridge control. H−bridge control provides forward, reverse, brake and high impedance states.

Overvoltage Clamping − Driving Inductive Loads

Each output is internally clamped to ground and VS by internal freewheeling diodes. The diodes have ratings that complement the FETs they protect. A flyback event from driving an inductive load causes the voltage on the output to rise up. Once the voltage rises higher than VS by a diode voltage (body diode of the high−side driver), the energy in the inductor will dissipate through the diode to VS. If a reverse battery diode is used in the system, care must be taken to insure the power supply capacitor is sufficient to dampen any increase in voltage to VS caused by the current flow through the body diode so that it is below 40 V. Negative transients will momentarily occur when a high−side driver driving an inductive load is turned off. This will be clamped by an internal diode from the output pin (OUT1 or OUT2) to the IC ground.

Current Limit

OUTx current is limited per the Current Limit electrical parameter for each driver. The magnitude of the current has a minimum specification of 2 A at V_{CC} = 5 V and V_s = 13.2 V. The output is protected for high power conditions during Current Limit by thermal shutdown and the Overcurrent Detection shutdown function. Overcurrent Detection shutdown protects the device during current limit because the Overcurrent threshold is below the Current Limit threshold. The Overcurrent Detection Shutdown Control Timer is initiated at the Overcurrent Shutdown Threshold which starts before the Current Limit is reached.

Note: High currents will cause a rise in die temperature. Devices will not be allowed to turn on if the die temperature exceeds the thermal shutdown temperature.

Shoot−Through Attempt

The NCV7703C provides detection for attempting to turn on common drivers of the same channel (OUTL1&OUTH1, OUTL2&OUTH2, OUTL3&OUTH3) simultaneously. An attempt to turn on common drivers if allowed would result in a high current event from VS to GND. Any attempt to create this setup is recorded in bit 12 of the output data and forces the common high−side and low−side driver to an off state. The STA output bit is reset with SRR = 1. The STA bit must be cleared before an affected driver can turn on.

Overcurrent Shutdown

Effected outputs will turn off when the Overcurrent Shutdown Threshold has been breached for the Overcurrent Shutdown Delay Time. The respective OCDR status bit will be set to a “1” and the driver will latch off. The driver can only be turned back on via the SPI port with a SPI command that includes an SRR = 1.

Note: High currents will cause a rise in die temperature. Devices will not be allowed to turn on if the die temperature exceeds the thermal shutdown temperature.

Table 3. OVERCURRENT DETECTION SHUT DOWN

OCD Input Bit 13	OUTx OCD Condition	Output Data Bit 13 Over Current Detect (OCDR) Status	OUTx Status	Current Limit of all Drivers
			μ	
			μ	

Overcurrent Detection Shut Down Control Timer

There are two protection mechanisms for output current, overcurrent and current limit.

1. Current limit − Always active with a typical threshold of 3 A (typ).
2. Overcurrent Detection − Selectable shutdown time via B .3f3 Tith a t1.45 (typ). hreshold

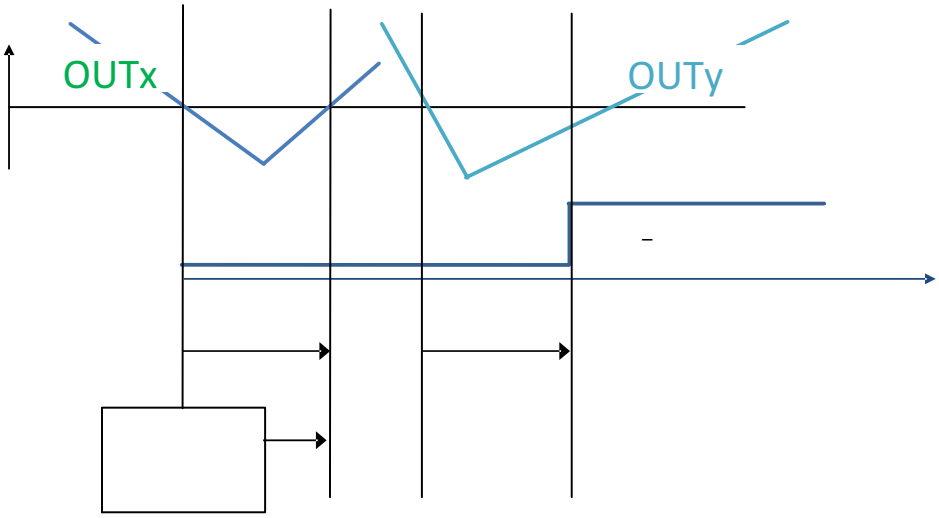


Figure 14. Underload Discontinuous Time

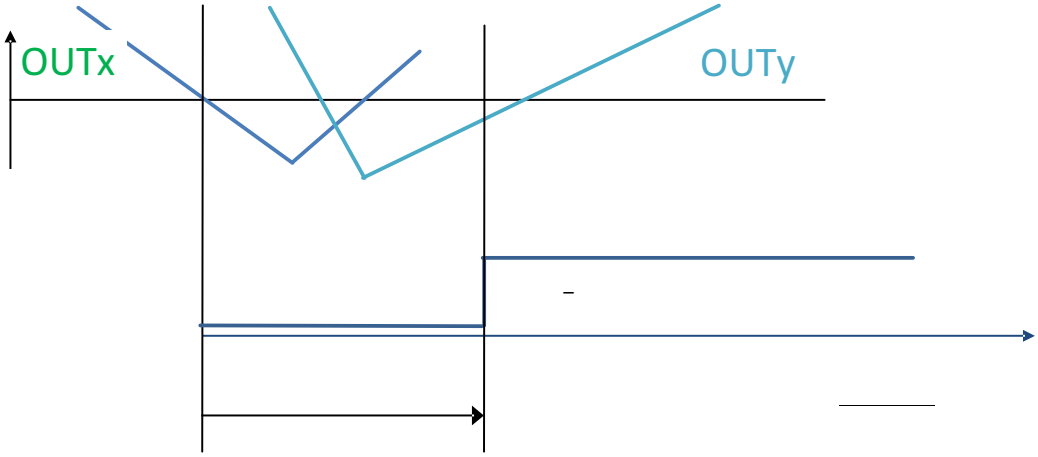
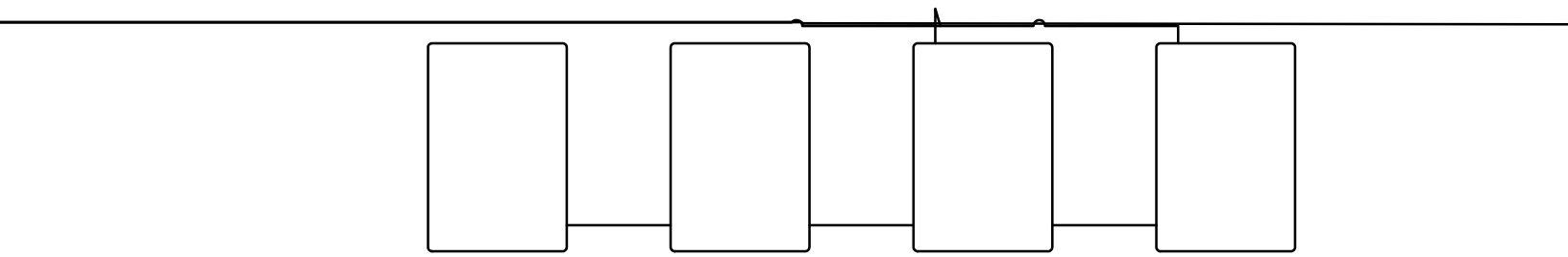


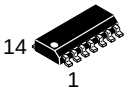
Figure 15. Underload Continuous Time

Thermal Shutdown

Three independent thermal shutdown circuits are featured (one common sensor for each HS and LS transistor pair). Each sensor has two temperature levels; Level 1, Thermal Warning sets the “TW” status bit to a 1 and would have to be reset with a command that includes the SRR after the IC cools to a temperature below Level 1. The output will remain on in this condition.

If the IC temperature reaches Level 2, Over Temperature

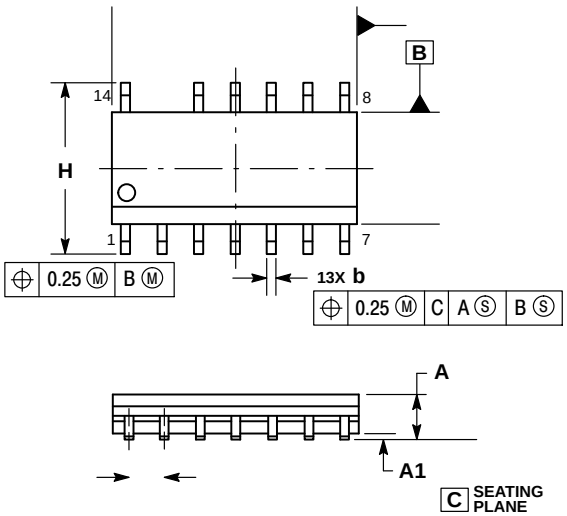




SCALE 1:1

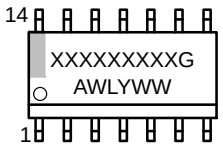
SOIC 14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

STYLES ON PAGE 2

SOIC 14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE