7705(A), 7706

The NCV7705/NCV7706 is a powerful Driver−IC for automotive body control systems. The IC is designed to control several loads in the front door of a vehicle. The monolithic IC is able to control mirror functions like mirror positioning, heating and folding. In addition, NCV7706 includes the electro−chromic mirror feature. The device features four high−side outputs to drive LEDs or incandescent bulbs (up to 5/10 W). To allow maximum flexibility, all lighting outputs can be PWM controlled thru PWM inputs (external signal source) or by an internal programmable PWM generator unit. The NCV7705/NCV7706 is controlled thru a 24 bit SPI interface with in−frame response.

Features

- Operating Range from 5.5 V to 28 V
- Four High−Side and Four Low−Side Drivers Connected as Half−Bridges
  - 2x Half−bridges I_{load} = 0.75 A; $R_{DS(on)}$ = 1.6 Ω @ 25°C
  - 2x Half−Bridges I_{load} = 3 A; $R_{DS(on)}$ = 300 mΩ @ 25°C
- Four High−Side Lamp Drivers
  - 2x LED; I_{load} = 0.3 A; $R_{DS(on)}$ = 1.4 Ω @ 25°C
  - 1x 10 W; Configurable as LED Driver; I_{load} = 2.5 A; $R_{DS(on)}$ = 300 mΩ @ 25°C
  - 1x 5 W; Configurable as LED Driver; I_{load} = 1.25 A; $R_{DS(on)}$ = 600 mΩ @ 25°C
- 1x High−Side Driver for Mirror Heating; I_{load} = 6 A; $R_{DS(on)}$ = 100 mΩ @ 25°C
- Electro Chromic Mirror Control (NCV7706 Only)
  - 1x 6−Bit Selectable Output Voltage Controller
  - 1x LS for EC Control; I_{load} = 0.75 A; $R_{DS(on)}$ = 1.6 Ω @ 25°C
- Independent PWM Functionality for All Outputs
- Integrated Programmable PWM Generator Unit for All Lamp Driver Outputs
  - 7−bit / 10−bit Selectable Duty−cycle Setting Precision
- Programmable Soft−start Function to Drive Loads with Higher Inrush Currents as Current Limitation Value
- Multiplex Current Sense Analog Output for Advanced Load Monitoring
- Very Low Current Consumption in Standby Mode
- Charge Pump Output to Control an External Reverse Polarity Protection MOSFET
-

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NCV7705/D

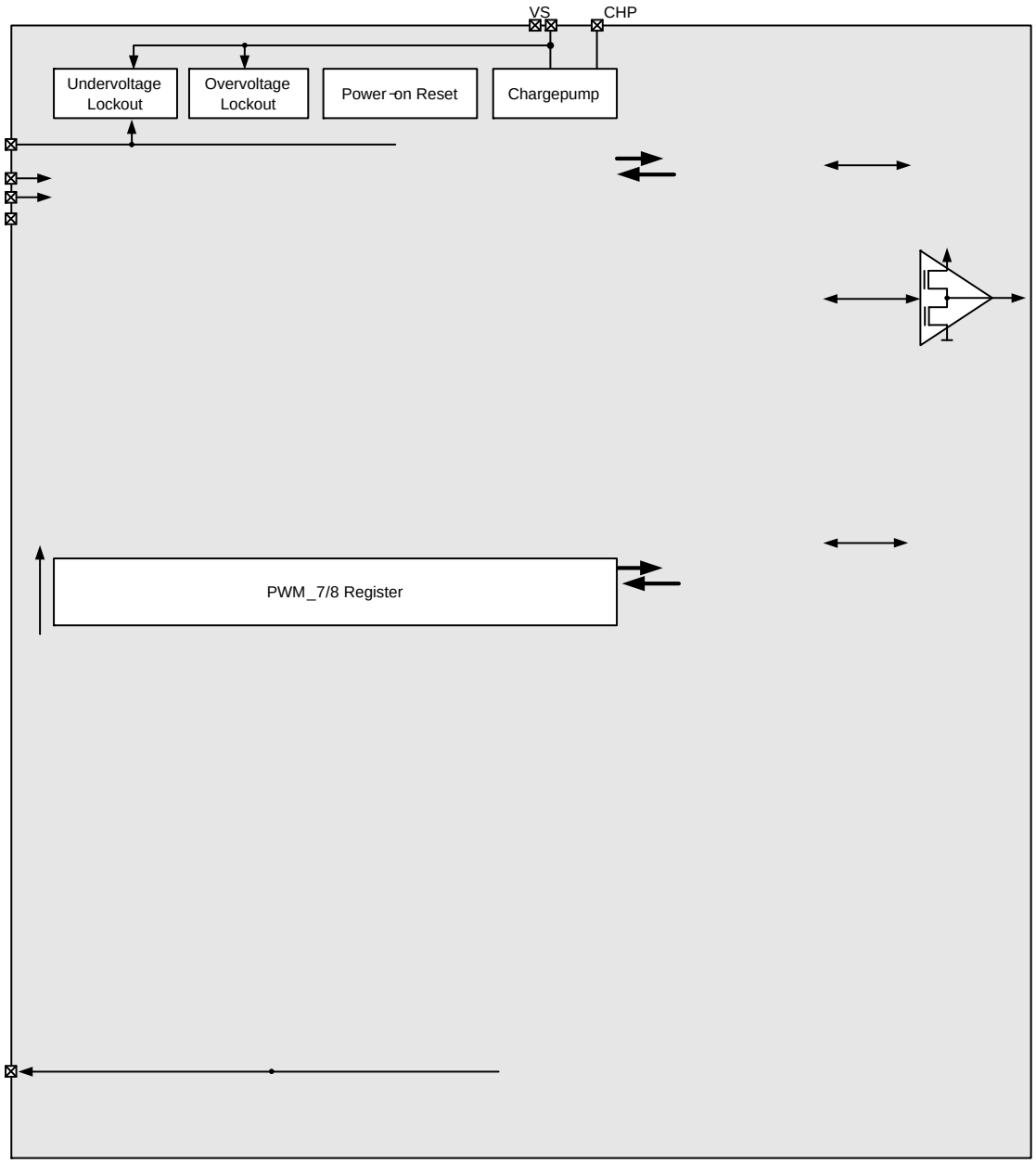


Figure 1. Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Pin Type	Description
1	GND	Ground	

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Min	Max	Unit
Vs	Power supply voltage − Continuous supply voltage − Transient supply voltage (t < 500 ms, ”clamped load dump”)	 −0.3 −0.3	 28 40	

ELECTRICAL CHARACTERISTICS

4.5 V < V_{CC} < 5.25 V, 8 V < Vs < 18 V, −40°C < T_J < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SUPPLY						
Vs	Supply voltage	Functional (see V_{UV_VS} / V_{OV_VS}) Parameter specification	5.5 8		28 18	V
Is(standby)	Supply Current (VS), Standby mode	Standby mode, VS = 16 V, 0 V ≤ V_{CC} ≤ 5.25 V, CSB = V_{CC}, OUTx/ECx = floating, SI = SCLK = 0 V, T_J < 85°C (T_J = 150°C)		3.5 (9)	12 (25)	μA
Is(active)	Supply current (VS), Active mode	Active mode, VS = 16 V, OUTx/ECx = floating		8	20	mA
I_{CC}(standby)	Supply Current (VCC), Standby mode	Standby mode, V_{CC} = 5.25 V, SI = SCLK = 0 V, T_J < 85°C (T_J = 150°C)		4.5 (15)	6 (50)	μA

I

ELECTRICAL CHARACTERISTICS (continued)
4.5 V < V_{CC} < 5.25 V, 8 V < Vs < 18 V, −40°C < T_J < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
MIRROR COMMON OUTPUT (X/Y, FOLD) OUT1, OUT4						
Ron_out1,4	On−resistance HS or LS	T_J = 25°C, Iout1,4 = ±1.5 A		0.3		Ω
		T_J = 125°C, Iout1,4 = ±1.5 A			0.6	
Ioc1,4_hs	Overcurrent threshold HS	T_J < 25°C T_J ≥ 25°C	−5.5 −5		−3	A
Ioc1,4_ls	Overcurrent threshold LS	T_J < 25°C T_J ≥ 25°C	3		5.5 5	A
Vlim1,4	Vds voltage limitation HS or LS		2		3	V
Iuld1,4_hs	Underload detection threshold HS		−80		−5	mA
Iuld1,4_ls	Underload detection threshold LS		5		80	mA
td_HS1,4(on)	Output delay time, HS Driver on	Time from CSB going high to V(OUT1,4) = 0.1·Vs / 0.9·Vs (on/off)		2.5	12	μs
td_HS1,4(off)	Output delay time, HS Driver off			3	12	μs
td_LS1,4(on)	Output delay time, LS Driver on	Time from CSB going low to V(OUT1,4) = 0.9·Vs / 0.1·Vs (on/off)		1	12	μs
td_LS1,4(off)	Output delay time, LS Driver off			1.5	12	μs
tdLH1,4	Cross conduction protection time, low−to−high transition including LS slew−rate			0.5	22	μs
tdHL1,4	Cross conduction protection time, high−to−low transition including HS slew−rate			5.5	22	μs
Ileak_act_hs1,4	Output HS leakage current, Active mode	V(OUT1,4) = 0 V	−40	−16		μA
Ileak_act_ls1,4	Output pull−down current, Active mode	V(OUT1,4) = VS		105	185	μA
Ileak_stdby_hs1,4	Output HS leakage current, Standby mode	V(OUT1,4) = 0 V	−5			μA
Ileak_stdby_ls1,4	Output pull−down current, Standby mode	V(OUT1,4) = VS, T_J ≥ 25°C V(OUT1,4) = VS, T_J < 25°C		80	120 175	μA
td_uld1,4	Underload blanking delay		430		610	μs
tdb_old1,4	Overload shutdown blanking delay	Timer started after output activation	16		25	μs
td_old1,4	Overload shutdown filter time	Timer started after blanking delay				

ELECTRICAL CHARACTERISTICS (continued)
4.5 V < V_{CC} < 5.25 V, 8 V < Vs < 18 V, −40°C < T_J < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
MIRROR X/Y POSITIONING OUTPUTS OUT2, OUT3						
Ron_out2,3	On−resistance HS or LS	T_J = 25°C, Iout2,3 = ±0.5 A		1.6		Ω
		T_J = 125°C, Iout2,3 = ±0.5 A			3	Ω
Ioc2,3_hs	Overcurrent threshold HS	T_J < 25°C T_J ≥ 25°C	−1.35 −1.25		−0.75	A
Ioc2,3_ls	Overcurrent threshold LS	T_J < 25°C T_J ≥ 25°C	0.75		1.35 1.25	A
Vlim2,3	Vds voltage limitation HS or LS		2		3	V
Iuld2,3_hs	Underload detection threshold HS		−32	−20	−10	mA
Iuld2,3_ls	Underload detection threshold LS		10	20	32	mA
td_HS2,3(on)	Output delay time, HS Driver on	Time from CSB going high to V(OUT2,3) = 0.1·Vs / 0.9·Vs (on/off)		2.5	6	μs
td_HS2,3(off)	Output delay time, HS Driver off			3	6	μs
td_LS2,3(on)	Output delay time, LS Driver on	Time from CSB going low to V(OUT2,3) = 0.9·Vs / 0.1·Vs (on/off)		1	6	μs
td_LS2,3(off)	Output delay time, LS Driver off			1	6	μs
tdLH2,3	Cross conduction protection time, low−to−high transition including LS slew−rate			0.5	22	μs
tdHL2,3	Cross conduction protection time, high−to−low transition including HS slew−rate			5.5	22	μs
Ileak_act_hs2,3	Output HS leakage current, Active mode	V(OUT2,3) = 0 V	−40	−16		μA
Ileak_act_ls2,3	Output pull−down current, Active mode	V(OUT2,3) = VS		105	185	μA
Ileak_stdby_hs2,3	Output HS leakage current, Standby mode	V(OUT2,3) = 0 V	−5			μA
Ileak_stdby_ls2,3	Output pull−down current, Standby mode	V(OUT2,3) = VS, T_J ≥ 25°C V(OUT2,3) = VS, T_J < 25°C		80	120 175	μA μA
td_uld2,3	Underload blanking delay		430		610	μs
tdb_old2,3	Overload shutdown blanking delay	Timer started after output activation	16		25	μs
td_old2,3	Overload shutdown filter time	Timer started after blanking delay elapsed	16		50	μs
frec2,3L	Recovery frequency, slow recovery mode	CONTROL_3.OCRF = 0	1		4	kHz
frec2,3H	Recovery frequency, fast recovery mode	CONTROL_3.OCRF = 1	2		6	kHz
dVout2,3	Slew rate of HS driver	Vs = 13.5 V, Rload = 64 Ω to GND	1.3	2.3	3.3	V/μs

ELECTRICAL CHARACTERISTICS (continued)
4.5 V < V_{CC} < 5.25 V, 8 V < Vs < 18 V, −40°C < T_J < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BULB / LED DRIVER OUTPUT OUT5						
Ron_out5_ICB	On−resistance to supply, HS switch, Bulb mode	T_J = 25°C, Iout5 = −1 A		0.3		Ω
		T_J = 125°C, Iout5 = −1 A			0.6	
Ron_out5_LED	On−resistance to supply, HS switch, LED mode	T_J = 25°C, Iout5 = −0.2 A		1.4		Ω
		T_J = 125°C, Iout5 = −0.2 A			3	
Ilim5_ICB	Output current limitation to GND, Bulb mode	T_J < 25°C T_J ≥ 25°C	−3.9 −3.7		−2.5	A
Ilim5_LED	Overcurrent threshold, LED mode		−1.1		−0.5	A
Iuld5_ICB	Underload detection threshold, Bulb mode		−65		−5	mA
Iuld5_LED	Underload detection threshold, LED mode		−15		−5	mA
td_OUT5_ICB(on)	Output delay time, Driver on, Bulb mode	Time from CSB going high to V(OUT5) = 0.1·Vs / 0.9·Vs (on/off); Rload = 16 Ω		15	48	µs
td_OUT5_ICB(off)	Output delay time, Driver off, Bulb mode			21	48	
td_OUT5_LED(on)	Output delay time, Driver on, LED mode	Time from CSB going high to V(OUT5) = 0.1·Vs / 0.9·Vs (on/off); Rload = 64 Ω		15	48	µs
td_OUT5_LED(off)	Output delay time, Driver off, LED mode			21	48	

ELECTRICAL CHARACTERISTICS (continued)
4.5 V < V_{CC} < 5.25 V, 8 V < Vs < 18 V, −40°C < T_J < 150°C; unless otherwise noted.

Symbol	Typ	Max	Unit

ELECTRICAL CHARACTERISTICS (continued)
4.5 V < V_{CC} < 5.25 V, 8 V < Vs < 18 V, −40°C < T_J < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
ELECTROCHROMIC MIRROR CONTROL (ECFB, ECON) (NCV7706 ONLY)						
Ron_ecfb	On−resistance to GND, LS switch	T_J = 25°C, Iecfb = 0.5 A		1.6		Ω
		T_J = 125°C, Iecfb = 0.5 A			3	Ω
Ilim_ecfb_src	Output current limitation to GND	Vs = 13.5 V, V_{CC} = 5 V	0.75		1.25	A
Vlim_ecfb	Vds voltage limitation	Output enabled	2		3	V
Iuld_ecfb	Underload detection threshold	Vs = 13.5 V, V_{CC} = 5 V	10	20	35	mA
td_ecfb(on)	Output delay time, LS Driver on	Vs = 13.5 V, V_{CC} = 5 V, Rload = 64 Ω, V(ECFB) = 0.9·VS / 0.1·VS (on /off)		1	12	µs
td_ecfb(off)	Output delay time, LS Driver off			2	12	
Ileak_ecfb_stdby	Output leakage current, LS off	Vecfb = Vs, Standby mode	−15		15	µA
Ileak_ecfb_act		Vecfb = Vs, Active mode	−10		10	µA
td_uld_ecfb	Underload blanking delay		430		610	µs
tdb_old_ecfb	Overload shutdown blanking delay	Timer started after output activation	30		48	µs
td_old_ecfb	Overload shutdown filter time	Timer started after blanking delay elapsed	16		50	µs
dVecfb/dt(on/off)	Slew rate of ECFB, LS switch	Vs = 13.5 V, V_{CC} = 5 V, Rload = 64 Ω		5		V/µs
Vctrl_max	Maximum EC control voltage	CONTROL_2.FSR = 1	1.4		1.6	V
		CONTROL_2.FSR = 0	1.12		1.28	V
DNL	Differential non linearity	1 LSB = 23.8 mV	−1			

ELECTRICAL CHARACTERISTICS (continued)
4.5 V < V_{CC} < 5.25 V, 8 V < Vs < 18 V, −40°C < T_J < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
CURRENT SENSE MONITOR OUTPUT ISOUT/PWM2						
Vis	Current Sense output functional voltage range	V_{CC} = 5 V, Vs = 8−20 V	0		V_{CC} − 0.5	V
Kis	Current Sense output ratio OUT1/4	K = Iout / Iis, 0 V ≤ Vis ≤ 4.5 V, V_{CC} = 5 V		12000		
	Current Sense output ratio OUT9 and 5 (low on−resistance bulb mode)			10000		
	Current Sense output ratio OUT6 (low on−resistance bulb mode)			5000		
	Current Sense output ratio OUT7/8 and 5/6 (high on−resistance LED mode)			2000		
Iis,acc (Notes 6 and 7)	Current Sense output accuracy OUT1/4	0.3 V ≤ Vis ≤ 4.5 V, V_{CC} = 5 V Iout1/4 = 0.5−2.9 A	−12.5% − 1% FS		12.5% + 1% FS	
	Current Sense output accuracy OUT5/6 (low on−resistance bulb mode)	0.3 V ≤ Vis ≤ 4.5 V, V_{CC} = 5 V Iout5 = 0.5−1.3 A, Iout6 = 0.25−0.65 A	−14% − 1% FS		14% + 1% FS	
	Current Sense output accuracy OUT5/6 (high on−resistance LED mode)	0.3 V ≤ Vis ≤ 4.5 V, V_{CC} = 5 V Iout5,6 = 0.1−0.3 A	−14% − 1% FS		14% + 1% FS	
	Current Sense output accuracy OUT7/8	0.3 V ≤ Vis ≤ 4.5 V, V_{CC} = 5 V	−8% − 1.5% FS		8% + 1.5% FS	
	Current Sense output accuracy OUT9	0.3 V ≤ Vis ≤ 4.5 V, V_{CC} = 5 V Iout9 = 0.5−5.9 A	−10% − 1.5% FS		10% + 1.5% FS	
tis_blank	Current Sense blanking time	Blanking time after current sense selection or driver activation	50		65	μs
tis	Current Sense settling time	0 V to FSR (full scale range)		230	265	μs

6. Current sense output accuracy = Isout−Isout_ideal relative to Isout_ideal
7. FS (Full scale) = Ioutmax/Kis

ELECTRICAL CHARACTERISTICS (continued)
4.5 V < V_{CC} < 5.25 V, 8 V < Vs < 18 V, −40°C < T_J < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DIGITAL INPUTS CSB, SCLK, PWM1/2, SI						
VinI	Input low level	V_{CC} = 5 V			0.3·V	

ELECTRICAL CHARACTERISTICS (continued)
4.5 V < V_{CC} < 5.25 V, 8 V < Vs < 18 V, −40°C < T_J < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DIGITAL OUTPUT SO						
Vsol	Output low level	Iso = 5 mA			0.2·V_{CC}	V
Vsoh	Output high level	Iso = −5 mA	0.8·V_{CC}			V
Ileak_so	Tristate leakage current	Vcsb = V_{CC}, 0 V < Vso < V_{CC}	−10		10	μ

ELECTRICAL CHARACTERISTICS (continued)
4.5 V < V_{CC} < 5.25 V, 8 V < Vs < 18 V, −40°C < T_J < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
THERMAL PROTECTION						
Tjtw_on	Temperature warning threshold	Junction temperature	140		160	°C
Tjtw_hys	Thermal warning hysteresis			5		°C
Tjsd_on	Thermal shutdown threshold, T_J increasing	Junction temperature	160		180	°C
Tjsd_off	Thermal shutdown threshold, T_J decreasing	Junction temperature	160			°C
Tjsd_hys	Thermal shutdown hysteresis			5		°C
Tjsdtw_delta	Temperature difference between warning and shutdown threshold			20		

DETAILED OPERATING AND PIN DESCRIPTION

General

The NCV7705/NCV7706 provides four half−bridge drivers, five independent high−side outputs and a programmable PWM control unit for free configuration. Strict adherence to integrated circuit die temperature is necessary, with a static maximum die temperature of 150°C. This may limit the number of drivers enabled at one time. Output drive control and fault reporting are handled via the SPI (Serial Peripheral Interface) port. A SPI−controlled mode control provides a low quiescent sleep current mode when the device is not being utilized. A pull down is provided on the SI and SCLK inputs to ensure they default to a low state in the event of a severed input signal. A pull−up is provided on the CSB input disabling SPI communication in the event of an open CSB input.

Supply Concept

Power Supply Scheme − VS and VCC

The Vs power supply voltage is used to supply the half bridges and the high−side drivers. An all−internal chargepump is implemented to provide the gate−drive voltage for the n−channel type high−side transistors. The VCC voltage is used to supply the logic section of the IC, including the SPI interface.

Due to the independent logic supply voltage the control and status information will not be lost in case of a loss of Vs supply voltage. The device is designed to operate inside the specified parametric limits if the VCC supply voltage is within the specified voltage range (4.5 V to 5.25 V). Between the operational level and the VCC undervoltage threshold level (Vuv_VCC) it is guaranteed that the device remains in a safe functional state without any inadvertent change to logic information.

Device / Module Ground Concept

The high−side output stages OUT5−9 are designed to handle DC output voltage conditions down to −0.3 V and allow for short negative transient currents due to parasitic line inductances. Therefore the application has to take care that these ratings are not violated under abnormal operating conditions (module loss of GND, ground shift if load connected to external GND) by either implementing external bypass diodes connected to GND or a direct connection between load−GND and module−GND. Since these output stages are designed to drive resistive loads,

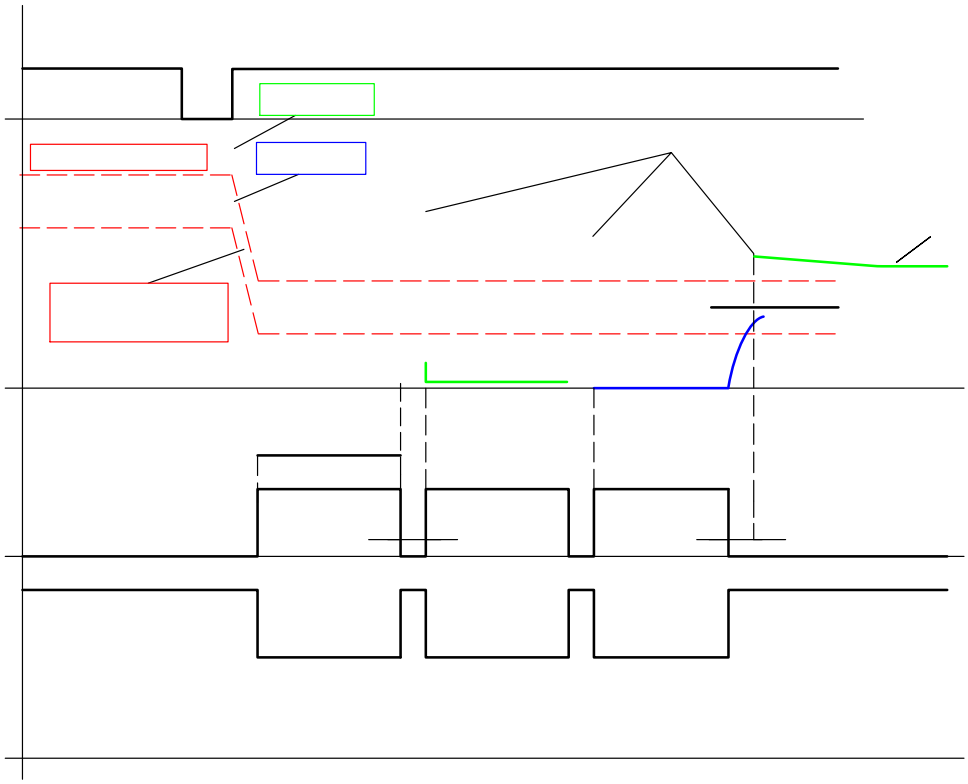


Figure 6. PWM Discharge Mode for ECFB

Diagnostic Functions

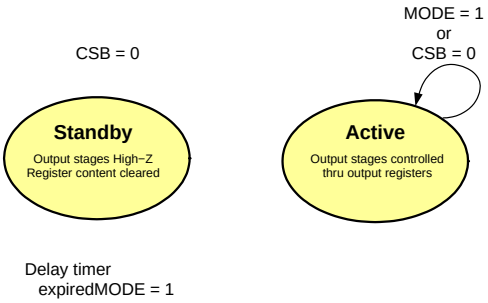
All diagnostic functions (overcurrent, underload, power supply monitoring, thermal warning and thermal shutdown) are internally filtered. The failure condition has to be valid for the minimum specified filtering time (td_old, td_uld, td_uvov and td_tx) before the corresponding status bit in the status register is set. The filter function is used to improve the noise immunity of the device. The undercurrent and temperature warning functions are intended for information purpose and do not affect the state of the output drivers. An overcurrent condition disables the corresponding output driver while a thermal shutdown event disables all outputs into high impedance state. Depending on the setting of the overcurrent recovery bits in the input register, the driver can either perform an auto−retry or remain latched off until the microcontroller clears the corresponding status bits. Overtemperature shutdown is latch−off only, without auto−retry functionality.

Overvoltage / Undervoltage Shutdown

If the supply voltage Vs rises above the switch off voltage Vov_vs(off) or falls below Vuv_vs(off), all output transistors are switched to high−impedance state and the global status bit UOV_OC (multi information) is set. The status flag STATUS_2.VSOV, resp. STATUS_2.VSUV is set, too, to log the over−/under−voltage event. The bit CONTROL_3.OVUVR can be used to determine the recovery behavior once the Vs supply voltage gets back into the specified nominal operating range. OVUVR = 0 enables auto−recovery, with OVUVR = 1 the output stages remain in high impedance condition until the status flags have been cleared. Once set, STATUS2.VSOV / VSUV can only be reset by a read&clear access to the status register STATUS_2.

Thermal Warning and Overtemperature Shutdown

The device provides a dual−stage overtemperature protection. If the junction temperature rises above Tjtw_on, a temperature warning flag (TW) is set in the Global Status Byte and can be read via SPI. The control software can then react onto this overload condition by a controlled disable of individual outputs. If however the junction temperature


MODE = 1
or
CSB = 0
CSB = 0
Standby
Output stages High−Z
Register content cleared
Active
Output stages controlled
thru output registers
Delay timer
expiredMODE = 1

24−bit SPI Interface

Both 24−bit input and output data are MSB first. Each SPI−input frame consists of a command byte followed by two data bytes. The data returned on SO within the same frame always starts with the global status byte. It provides general status information about the device. It is then followed by 2 data bytes (in−frame rF0ata

Table 4. COMMAND BYTE, REGISTER ADDRESS

A[5:0]	Access	Description	Content
00h	R/W	Control Register CONTROL_0	Device mode control, Bridge outputs control
01h	R/W	Control Register CONTROL_1	High−side outputs control, ECM control (NCV7706 only)
02h	R/W	Control Register CONTROL_2	Bridge outputs recovery control, PWM enable, ECM setup (NCV7706 only)
03h	R/W	Control Register CONTROL_3	High−side outputs recovery control, PWM enable, Current Sense selection
08h	R/W	PWM Control Register PWM_5/6	PWM control register for OUT5/6 (7b control only)
09h	R/W	PWM Control Register PWM_7/8	PWM control register for OUT7/8 (7b control only)
10h	R/RC	Status Register STATUS_0	Bridge outputs Overcurrent diagnosis
11h	R/RC	Status Register STATUS_1	Bridge outputs Underload diagnosis
12h	R/RC	Status Register STATUS_2	HS outputs Overcurrent and Underload diagnosis, Vs Over− and Under-voltage, EC−mirror
13h	R/W	PWM Control Register PWM_5	PWM control register for OUT5 (10b control only)
14h	R/W	PWM Control Register PWM_6	PWM control register for OUT6 (10b control only)
15h	R/W	PWM Control Register PWM_7	PWM control register for OUT7 (10b control only)
16h	R/W	PWM Control Register PWM_8	PWM control register for OUT8 (10b control only)
3Fh	R/W	Configuration Register CONFIG	Mask bits for global fault bits

Table 5. CHIP ID INFORMATION

A[5:0]	Access	Description	Content
00h	RDID	ID header	4300h
01h	RDID	Version	0001h (NCV7705, NCV7706) 0004h (NCV7705A)
02h	RDID	Product Code 1	7700h
03h	RDID	Product Code 2	0500h (NCV7705) 0600h (NCV7706)
3Eh	RDID	SPI−Frame ID	0200h

Table 6. GLOBAL STATUS BYTE CONTENT

FLT	Global Fault Bit	
0	No fault Condition	Failures of the Global Status Byte, bits [6:0] are always linked to the Global Fault Bit FLT. This bit is generated by an OR combination of all failure bits of the device (RESB inverted). It is reflected via the SO pin while CSB is held low and NO clock signal is present (before first positive edge of SCLK). The flag will remain valid as long as CSB is held low. This operation does not cause the Transmission error Flag in the Global Status Byte to be set. Signals TW and ULD can be masked.
1	Fault Condition	
TF	**SPI Transmission Error**	
0	0	

SPI REGISTERS CONTENT

CONTROL_0 Register

Address: 00h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access type	RW	RW	RW	RW	RW	RW	−	−	−	−	RW	RW	−	−	−	RW
Bit name	HS1	LS1	HS2	LS2	HS3	LS3	0	0	0	0	HS4	LS4	0	0	0	MODE
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	HSx	LSx		Description	Remark
HS/LS Outputs OUT1−4 Driver Control	0	0	default	OUTx High impedance	If a driver is enabled by the control register AND the corresponding PWM enable bit is set in CONTROL_2 register, the output is only activated if PWM1 (PWM2) input signal is high. Since OUT1..OUT4 are half−bridge outputs, activating both HS and LS at the

CONTROL_1 Register
Address: 01h

NCV7705:

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	−
Bit name	HS5.1	HS5.0	HS6.1	HS6.0	HS7	HS8	HS9	LS ECFB	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0		

	IS3	IS2	IS1	IS0	Description	Remark
Current Sensing Selection	0	0	0	0	OUT1	

PWM_7/8 Register
Address: 09h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	FSEL7	PW7.6	PW7.5	PW7.4	PW7.3	PW7.2	PW7.1	PW7.0	FSEL8	PW8.6	PW8.5	PW8.4	PW8.3	PW8.2	PW8.1	PW8.0
Reset Value																

STATUS_0 Register

Address: 10h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access Type	R/RC	R/RC	R/RC	R/RC	R/RC	R/RC	−	−	−	−	R/RC	R/RC	−	−	−	−
Bit Name	OC HS1	OC LS1	OC HS2	OC LS2	OC HS3	OC LS3	0	0	0	0	OC HS4	OC LS4	0	0	0	0
Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	OCx	Description	Remark
OUT1−4 Overcurrent Detection	0	No overcurrent detected	During an overcurrent event in one of the HS or LS, the belonging overcurrent status bit STATUS_0.OCx is set and the dedicated output is switchedng

STATUS_2 Register
Address: 12h

NCV7705:

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access type	R/RC	R/RC	R/RC	R/RC	R/RC	R/RC	R/RC	R/RC	R/RC	R/RC	−	−	R/RC	R/RC	−	−
Bit name	OC HS5	ULD HS5	OC HS6	ULD HS6	OC HS7	ULD HS7	OC HS8	ULD HS8	OC HS9	ULD HS9	0	0	VSUV	VSOV	0	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

PWM_5 Register
Address: 13h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access Type	RW	–	–	–	–	–	RW	RW	RW	RW	RW	RW	RW	RW		

PWM_7 Register
Address: 15h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access Type	RW	–	–	–	–	–	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

CONFIG Register

Address: 3Fh

NCV7705:

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

F