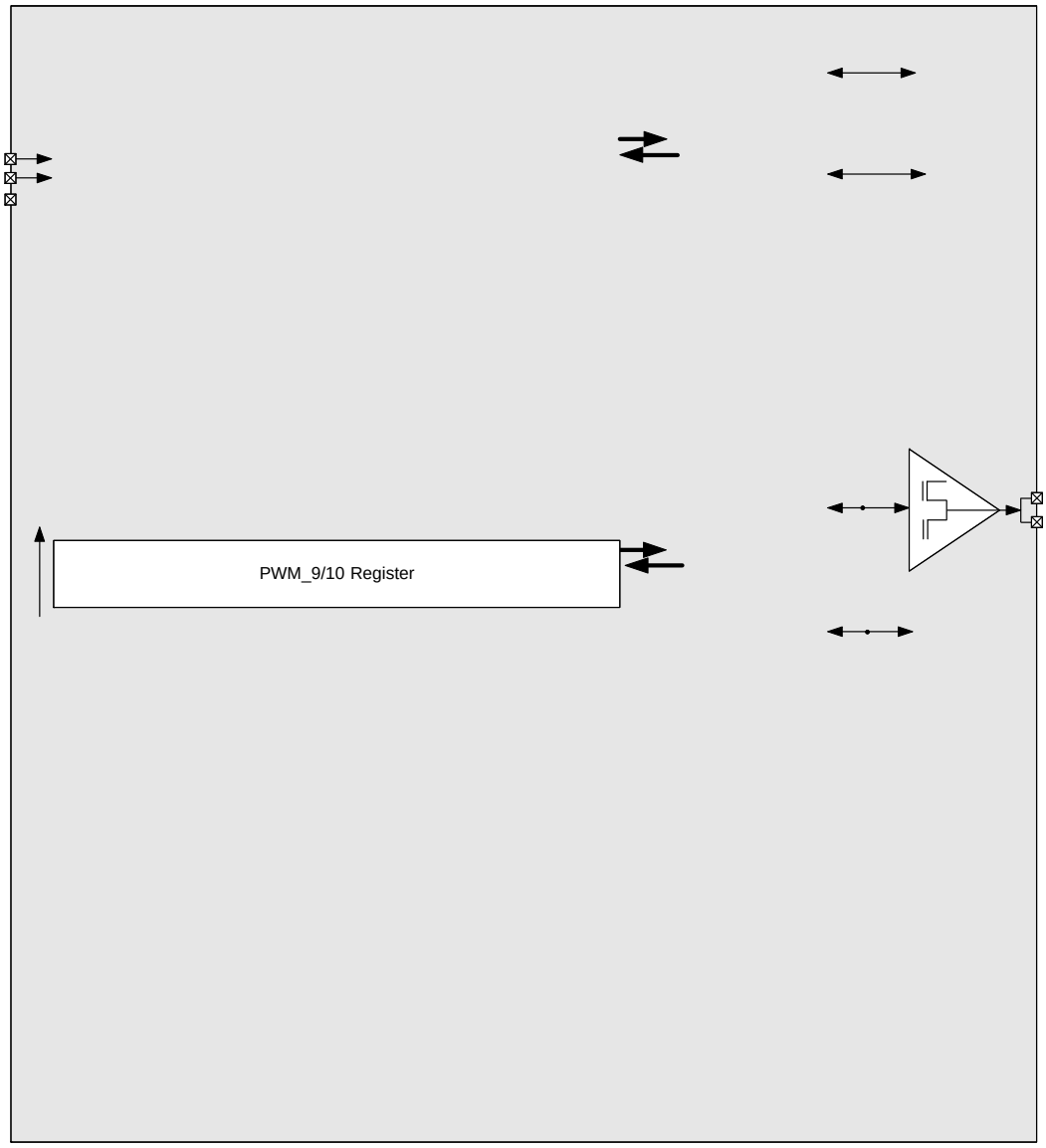
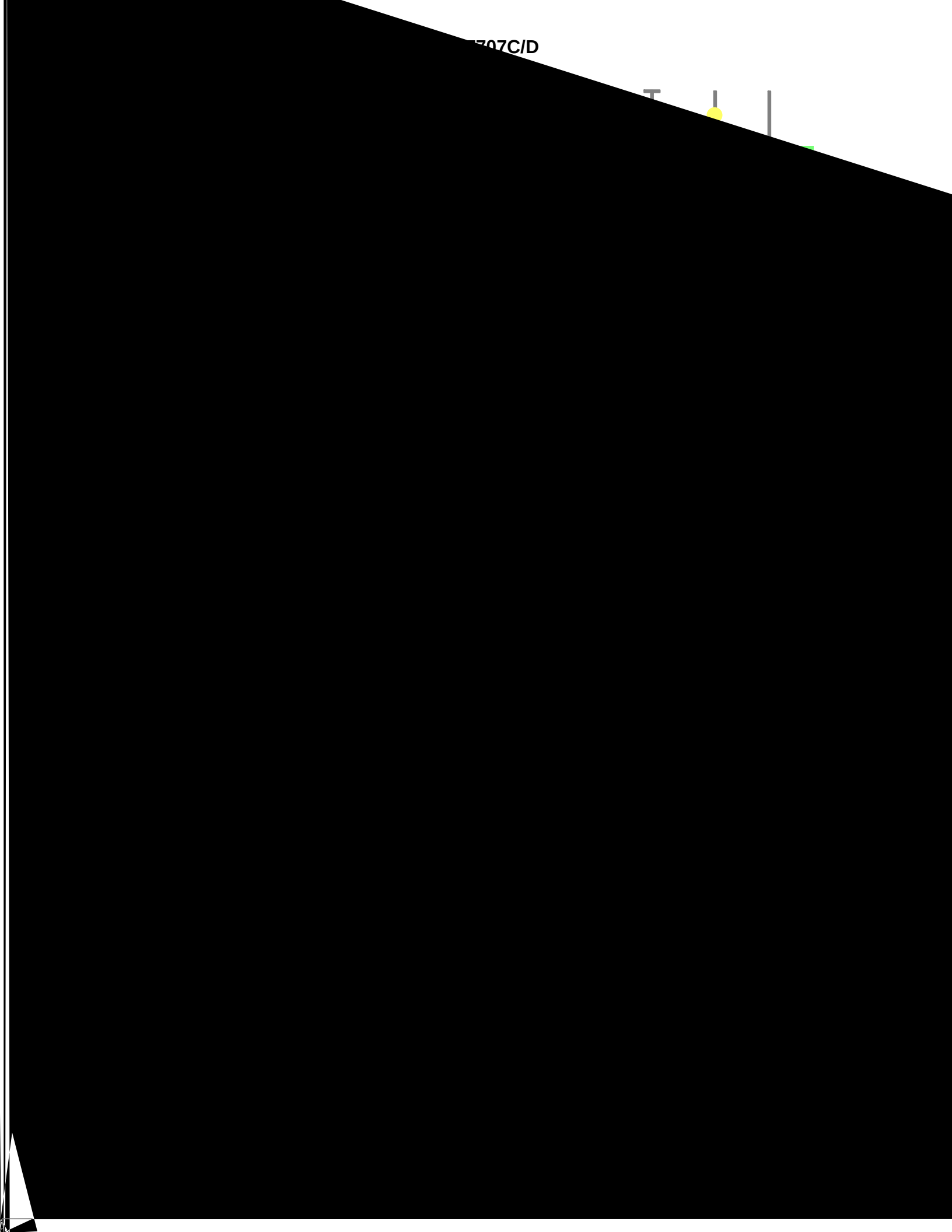

PWM_9/10 Register



ELECTRICAL CHARACTERISTICS (continued)
4.5 V < V_{CC} < 5.25 V, 8 V < Vs < 18 V, −40°C < T_J < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
MIRROR COMMON OUTPUT (X/Y, FOLD) OUT1						
Ron_out1	On−resistance HS or LS	T_J = 25°C, Iout1 = ±1.5 A		0.3		Ω
		T_J = 125°C, Iout1 = ±1.5 A			0.64	
Ioc1_hs	Overcurrent threshold HS		−5		−3.55	A
Ioc1_ls	Overcurrent threshold LS		3.55		5	A
Vlim1	Vds voltage limitation HS or LS		2		3	V
Iuld1_hs	Underload detection threshold HS		−80		−5	mA
Iuld1_ls	Underload detection threshold LS		10		80	mA
td_HS1(on)	Output delay time, HS Driver on	Time from CSB going high to V(OUT1) = 0.1·Vs / 0.9·Vs (on/off)		2.5	12	µs
td_HS1(off)	Output delay time, HS Driver off			3	12	µs
td_LS1(on)	Output delay time, LS Driver on	Time from CSB going low to V(OUT1) = 0.9·Vs / 0.1·Vs (on/off)		1	12	µs
td_LS1(off)	Output delay time, LS Driver off			1.5	12	µs
tdLH1	Cross conduction protection time, low−to−high transition including LS slew−rate			0.5	22	µs
tdHL1	Cross conduction protection time, high−to−low transition including HS slew−rate			5.5	22	µs
Ileak_act_hs1	Output HS leakage current, Active mode	V(OUT1) = 0 V	−40	−16		µA
Ileak_act_ls1	Output pull−down current, Active mode	V(OUT1) = VS		100	160	µA
Ileak_stdby_hs1	Output HS leakage current, Standby mode	V(OUT1) = 0 V	−5			µA
Ileak_stdby_ls1	Output pull−down current, Standby mode	V(OUT1) = VS, T_J ≥ 25°C V(OUT1) = VS, T_J < 25°C		80	120 175	µA
td_uld1	Underload blanking delay		430		610	µs
td_old1	Overload shutdown blanking delay		5		25	µs
frec1L	Recovery frequency, slow recovery mode	CONTROL_3.OCRF = 0	1.3		2.1	kHz
frec1H	Recovery frequency, fast recovery mode	CONTROL_3.OCRF = 1	2.6		4.2	kHz
dVout1	Slew rate of HS driver	Vs = 13.5 V, Rload = 16 Ω to GND	1	2	3	V/µs

ELECTRICAL CHARACTERISTICS (continued)
4.5 V < V_{CC} < 5.25 V, 8 V < Vs < 18 V, −40°C < T_J < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
MIRROR X/Y POSITIONING OUTPUTS OUT2, OUT3						
Ron_out2,3	On−resistance HS or LS	T_J = 25°C, Iout2,3 = ±0.5 A		1.6		Ω
		T_J = 125°C, Iout2,3 = ±0.5 A			3.4	Ω
Ioc2,3_hs	Overcurrent threshold HS		−1.25		−0.75	A
Ioc2,3_ls	Overcurrent threshold LS		0.75		1.25	A
Vlim2,3	Vds voTm2,3					

ELECTRICAL CHARACTERISTICS (continued)
4.5 V < V_{CC} < 5.25 V, 8 V < Vs < 18 V, −40°C < T_J < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DOOR LOCK OUTPUTS OUT4, OUT5						
Ron_out4,5	On−resistance HS or LS	T_J = 25°C, Iout4,5 = ±3 A		0.15		Ω
		T_J = 125°C, Iout4,5 = ±3 A			0.3	Ω
Ioc4,5_hs	Overcurrent threshold HS		−10		−6	A
Ioc4,5_ls	Overcurrent threshold LS		6		10	A
Vlim4,5	Vds voltage limitation HS or LS		2		3	V
Iuld4,5_hs	Underload detection threshold HS		−300		−60	mA
Iuld4,5_ls	Underload detection threshold LS		60		300	mA
td_HS4,5 (on)	Output delay time, HS Driver on	Time from CSB going high to V(OUT4,5) = 0.1·Vs / 0.9·Vs (on/off)		2.5	12	μs
td_HS4,5 (off)	Output delay time, HS Driver off			3	12	μs
td_LS4,5 (on)	Output delay time, LS Driver on	Time from CSB going low to V(OUT4,5) = 0.9·Vs / 0.1·Vs (on/off)		1	12	μs
td_LS4,5 (off)	Output delay time, LS Driver off			1.5	12	μs
tdLH4,5	Cross conduction protection time, low−to−high transition including LS slew−rate			0.5	22	μs
tdHL4,5	Cross conduction protection time, high−to−low transition including HS slew−rate			5.5	22	μs
Ileak_act_hs4,5	Output HS leakage current, Active mode					

ELECTRICAL CHARACTERISTICS (continued)
4.5 V < V_{CC} < 5.25 V, 8 V < Vs < 18 V, −40°C < T_J < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SAFE LOCK, MIRROR FOLD OUTPUT OUT6						
Ron_out6	On−resistance HS or LS	T_J = 25°C, Iout6 = ±1.5 A		0.3		Ω
		T_J = 125°C, Iout6 = ±1.5 A			0.63	
Ioc6_hs						

ELECTRICAL CHARACTERISTICS (continued)
4.5 V < V_{CC} < 5.25 V, 8 V < Vs < 18 V, −40°C < T_J < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BULB / LED DRIVER OUTPUTS OUT7, OUT8						
Ron_out7,8_ICB	On−resistance to supply, HS switch, Bulb mode	T_J = 25°C, Iout7,8 = −1 A		0.3		Ω
		T_J = 125°C, Iout7,8 = −1 A			0.68	
Ron_out7,8_LED	On−resistance to supply, HS switch, LED mode	T_J = 25°C, Iout7,8 = −0.2 A		1.4		Ω
		T_J = 125°C, Iout7,8 = −0.2 A				

ELECTRICAL CHARACTERISTICS (continued)
4.5 V < V_{CC} < 5.25 V, 8 V < Vs < 18 V, −40°C < T_J < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
LED DRIVER OUTPUTS OUT9, OUT10						
Ron_out9,10	On−resistance to supply, HS switch	T_J = 25°C, Iout9,10 = −0.2 A		1.4		Ω
		T_J = 125°C, Iout9,10 = −0.2 A			3	Ω
Ioc9,10	Overcurrent threshold		−0.63		−0.38	A
Iuld9,10	Underload detection threshold		−16		−4	mA
td_OUT(on)9,10	Output delay time, Driver on	Time from CSB going high to V(OUT9,10) = 0.1·Vs / 0.9·Vs (on/off)		18	48	µs
td_OUT(off)9,10	Output delay time, Driver off			23	48	
Ileak_act9,10	Output leakage current, Active mode	V(OUT9,10) = 0 V	−10			µA
Ileak_stdby9,10	Output leakage current, Standby mode	V(OUT9,10) = 0 V	−5			µA
Ileak_out_vs9,10	Output pull−down current	V(OUT9,10) = VS			1	mA
td_uld9,10	Underload blanking delay		250		610	µs
td_old_OUT9,10	Overload shutdown blanking delay		16		50	µs
frec9,10L	Recovery frequency, slow recovery mode	CONTROL_3.OCRF = 0	1.3		2.1	kHz
frec9,10H	Recovery frequency, fast recovery mode	CONTROL_3.OCRF = 1	2.6		4.2	kHz
dVout9,10	Slew rate	Vs = 13.5 V, Rload = 64 Ω		0.2		V/µs

ELECTRICAL CHARACTERISTICS (continued)
4.5 V < V_{CC} < 5.25 V, 8 V < Vs < 18 V, −40°

ELECTRICAL CHARACTERISTICS (continued)
4.5 V < V_{CC} < 5.25 V, 8 V < Vs < 18 V, −40°C < T_J < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
CURRENT SENSE MONITOR OUTPUT ISOUT/PWM2						
Vis	Current Sense output functional voltage range	V_{CC} = 5 V, Vs = 8−20 V	0		V_{CC} − 0.5	V
Kis (Note 7)	Current Sense output ratio OUT1/6 and 7/8 (low on−resistance bulb mode)	K = Iout / Iis, 0 V ≤ Vis ≤ 4.5 V, V_{CC} = 5 V		10000		
	Current Sense output ratio OUT4/5			10000		
	Current Sense output ratio OUT9/10 and 7/8 (high on−resistance LED mode)			2000		
	Current Sense output ratio OUT11			10000		
Iis,acc (Notes 8 and 9)	Current Sense output accuracy OUT1/6	0.3 V ≤ Vis ≤ 4.5 V, V_{CC} = 5 V Iout1/6 = 0.5−2.9 A	−10% − 2% FS		10% + 2% FS	
	Current Sense output accuracy OUT4/5	0.3 V ≤ Vis ≤ 4.5 V, V_{CC} = 5 V, Iout4/5 = 0.5−5.9 A	−10% − 2% FS		10% + 2% FS	
	Current Sense output accuracy OUT7/8 (low on−resistance bulb mode)	0.3 V ≤ Vis ≤ 4.5 V, V_{CC} = 5 V Iout7/8 = 0.5−1.3 A	−10%−1.5% FS		10% + 1.5% FS	
	Current Sense output accuracy OUT7/8 (high on−resistance LED mode)	0.3 V ≤ Vis ≤ 4.5 V, V_{CC} = 5 V Iout7/8 = 0.1−0.3 A				

ELECTRICAL CHARACTERISTICS (continued)
4.5 V < V_{CC} < 5.25 V, 8 V < Vs < 18 V, −40°C < T_J < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DIGITAL INPUTS CSB, SCLK, PWM1/2, SI						
Vinl	Input low level	V_{CC} = 5 V			0.3·V_{CC}	V
Vinh	Input high level		0.7·V_{CC}			V
Vin_hyst	Input hysteresis		500			mV
Rcsb_pu	CSB pull−up resistor	V_{CC} = 5 V_{CC} 0 V < Vcsb < 0.7·V_{CC}	30	120	250	kΩ
Rsclk_pd	SCLK pull−down resistor	V_{CC} = 5 V, Vsclk = 1.5 V	30	60	220	kΩ
Rsi_pd	SI pull−down resistor	V_{CC} = 5 V, Vsi = 1.5 V	30	60	220	kΩ
Rpwm1_pd	PWM1 pull−down resistor	V_{CC} = 5 V, Vpwm1 = 1.5 V	30	60	220	kΩ
Rpwm2_pd	PWM2 pull−down resistor	V_{CC} = 5 V, Vpwm2 = 1.5 V, current sense disabled	30	60	220	kΩ
Ileak_isout	Output leakage current	current sense enabled	−1		3.5	μA
Ccsb / sclk / pwm1/2	Pin capacitance	0 V < V_{CC} < 5.25 V (Note 10)			10	pF
DIGITAL INPUTS CSB, SCLK, SI; TIMING						
tsclk	Clock period	V_{CC} = 5 V		1000		ns
tsclk_h	Clock high time		115			ns
tsclk_l	Clock low time		115			ns
tset_csb	CSB setup time, CSB low before rising edge of SCLK		400			ns
tset_sclk	SCLK setup time, SCLK low before rising edge of CSB		400			ns
tset_si	SI setup time		200			ns
thold_si	SI hold time		200			ns
tr_in	Rise time of input signal SI, SCLK, CSB				100	ns
tf_in	Fall time of input signal SI, SCLK, CSB				100	ns
tcsb_hi_stdby	Minimum CSB high time, switching from Standby mode	Transfer of SPI−command to input register, valid before tsact mode transition delay expires		5	10	μs
tcsb_hi_min	Minimum CSB high time, Active mode			2	4	μs

10. Values based on design and/or characterization.

ELECTRICAL CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (continued)
4.5 V < V_{CC} < 5.25 V, 8 V < Vs < 18 V, −40°C < T_J < 150°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
THERMAL PROTECTION						
Tjtw_on	Temperature warning threshold	Junction temperature	140		160	°C
Tjtw_hys	Thermal warning hysteresis			5		°C
Tjsd_on	Thermal shutdown threshold, T_J increasing	Junction temperature	160		180	°C
Tjsd_off	Thermal shutdown threshold, T_J decreasing	Junction temperature	160			°C
Tjsd_hys	Thermal shutdown hysteresis			5		°C
Tjsdtw_delta	Temperature difference between warning and shutdown threshold			20		°C
td_tx	Filter time for thermal warning and shutdown	TW / TSD Global Status bits	10		100	µs
OPERATING MODES TIMING						
tact	Time delay for mode change from Unpowered mode into Standby mode	SPI communication ready after V_{CC} reached $V_{uv\_VCC(off)}$ threshold			30	µs
tsact	Time delay for mode change from Standby mode into Active mode	Time until output drivers are enabled after CSB going to high and CONTROL_0.MODE = 1		170	440	µs
tacts	Time delay for mode change from Active mode into Standby mode via SPI	Time until output drivers are disabled after CSB going to high and CONTROL_0.MODE = 0			300	µs
INTERNAL PWM CONTROL UNIT (OUT7 – OUT10)						
PWMlo	PWM frequency, low selection	CONTROL_2.PWMI = 1, PWMx.FSELx = 0	135	170	200	Hz
PWMhi	PWM frequency, high selection	CONTROL_2.PWMI = 1, PWMx.FSELx = 1	175	225	260	Hz

DETAILED OPERATING AND PIN DESCRIPTION

General

The NCV7707C/D provides six half−bridge drivers, five independent high−side outputs and a programmable PWM control unit for free configuration. Strict adherence to integrated circuit die temperature is necessary, with a static maximum die temperature of 150°C. This may limit the number of drivers enabled at one time. Output drive control and fault reporting are handled via the SPI (Serial Peripheral Interface) port. A SPI−controlled mode control provides a low quiescent sleep current mode when the device is not being utilized. A pull down is provided on the SI and SCLK inputs to ensure they default to a low state in the event of a severed input signal. A pull−up is provided on the CSB input disabling SPI communication in the event of an open CSB input.

Supply Concept

Power Supply Scheme − VS and VCC

The Vs power supply voltage is used to supply the half bridges and the high−side drivers. An all−internal chargepump is implemented to provide the gate−drive voltage for the n−channel type high−side transistors. The VCC voltage is used to supply the logic section of the IC, including the SPI interface.

Due to the independent logic supply voltage the control and status information will not be lost in case of a loss of Vs supply voltage. The device is designed to operate inside the specified parametric limits if the VCC supply voltage is within the specified voltage range (4.5 V to 5.25 V). Between the operational level and the VCC undervoltage threshold level (Vuv_VCC) it is guaranteed that the device remains in a safe functional state without any inadvertent change to logic information.

Device / Module Ground Concept

The high−side output stages OUT7−11 are designed to handle DC output voltage conditions down to −0.3 V and allow for short negative transient currents due to parasitic line inductances. Therefore the application has to take care that these ratings are not violated under abnormal operating conditions (module loss of GND, ground shift if load connected to external GND) by either implementing external bypass diodes connected to GND or a direct connection between load−GND and module−GND. Since these output stages are designed to drive resistive loads, restrictions on maximum inductance / clamping energy apply.

The heat slug is not hard−connected to internal GND rail. It has to be connected externally.

Power Up/Down Control

In order to prevent uncontrolled operation of the device during power/up down, an undervoltage lockout feature is implemented. Both supply voltages (V_{CC} and Vs) are monitored for undervoltage conditions supporting a safe power−up transition. When Vs drops below the undervoltage threshold Vuv_vs(off) (Vs undervoltage threshold) all output stages are switched to high−impedance state and the global status bit UOV_OC is set. This bit is a multi information bit in the Global Status Byte which is set in case of overcurrent, Vs over− and undervoltage. In case of undervoltage the status bit STATUS_2.VSUV is set, too.

Bit CONTROL_3.OVUVR (Vs under−/overvoltage recovery behavior) can be used to select the desired recovery behavior after a Vs under−voltage event. In case of OVUVR = 0, all output stages return to their programmed state as soon as Vs recovers back to its normal operating range. If OVUVR is set, the automatic recovery function is disabled thus the output stages will remain in high−impedance condition until the status bits have been cleared by the microcontroller. To avoid high current oscillations in case of output short to GND and low Vs voltage conditions, it is recommended to disable the Vs−auto−recovery by setting OVUVR = 1.

Chargepump

In Standby mode, the chargepump is disabled. After enabling the device by setting bit CONTROL_0.MODE to active (1), the internal oscillator is started and the voltage at the CHP output pin begins to increase. The output drivers are enabled after a delay of tsact once MODE was set to active.

Driver Outputs

Output PWM Control

For all half−bridge outputs as well as the high−side outputs the device features the possibility to logically combine the SPI−setting with a PWM signal that can be provided to the inputs PWM1 and ISOUT/PWM2, respectively. Each of the outputs has a fixed 12−bit base period and a

Table 1. PWM CONTROL SCHEME

Output	PWM Control Input	
	CONTROL_2.PWMI = 0	CONTROL_2.PWMI = 1
OUT1	PWM1	PWM1
OUT2	PWM1	PWM1
OUT3	PWM1	PWM1
OUT4	PWM1	PWM1
OUT5	ISOUT/PWM2	ISOUT/PWM2
OUT6	PWM1	PWM1
OUT7	PWM1	PWM_7/8.PW7[6:0]
OUT8	ISOUT/PWM2	PWM_7/8.PW8[6:0]
OUT9	PWM1	PWM_9/10.PW9[6:0]
OUT10	ISOUT/PWM2	PWM_9/10.PW10[6:0]
OUT11	PWM1	

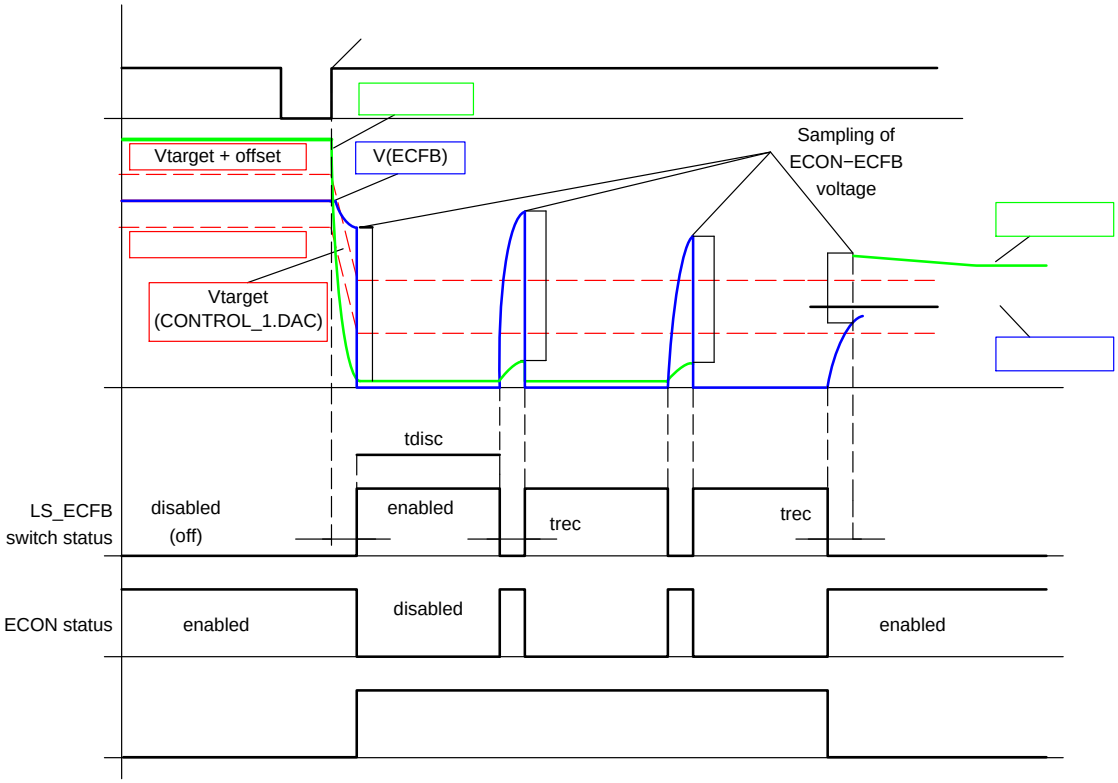


Figure 6. PWM Discharge Mode for ECFB

Diagnostic Functions

All diagnostic functions (overcurrent, underload, power supply monitoring, thermal warning and thermal shutdown) are internally filtered. The failure condition has to be valid for the minimum specified filtering time (td_old, td_uld, td_uvov and td_tx) before the corresponding status bit in the status register is set. The filter function is used to improve the noise immunity of the device. The undercurrent and temperature warning functions are intended for information purpose and do not affect the state of the output drivers. An overcurrent condition disables the corresponding output driver while a thermal shutdown event disables all outputs into high impedance state. Depending on the setting of the overcurrent recovery bits in the input register, the driver can

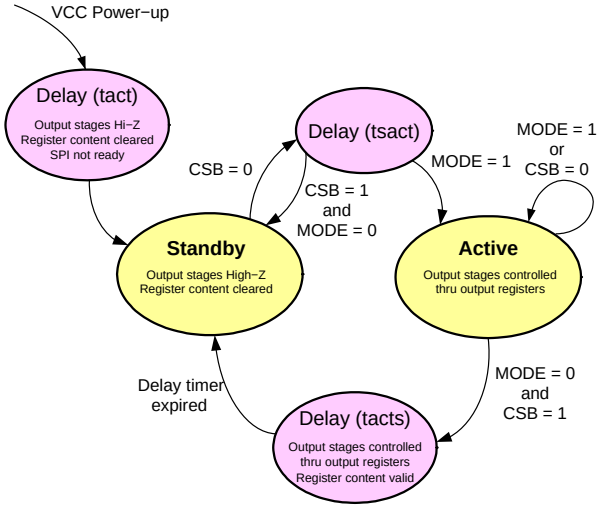


Figure 8. Mode Transitions Diagram

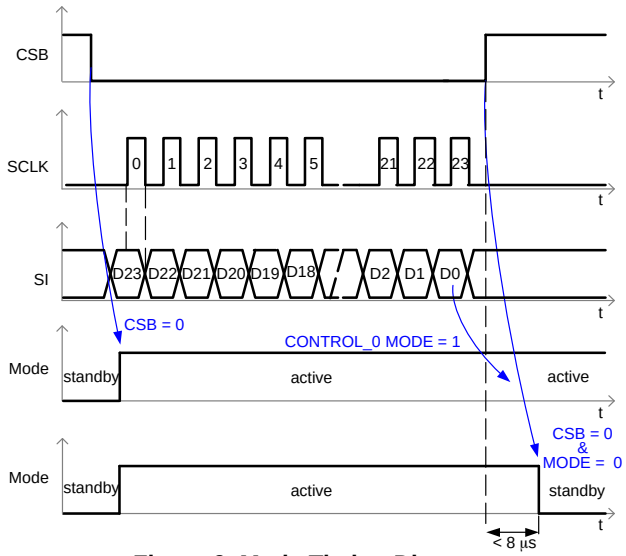


Figure 9. Mode Timing Diagram

SPI Control

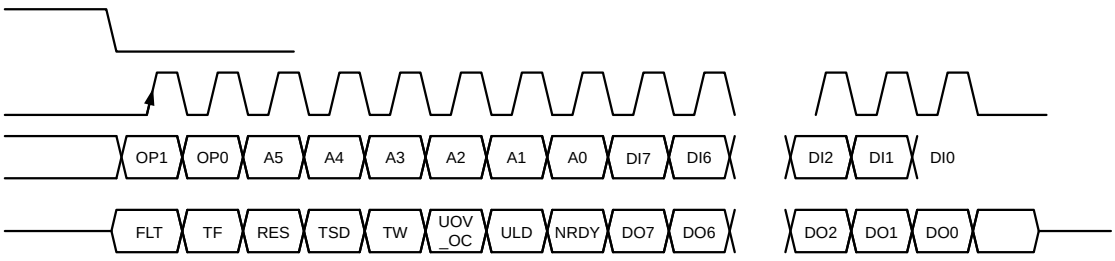
General Description

The 4−wire SPI interface establishes a full duplex synchronous serial communication link between the NCV7707C/D and the application's microcontroller. The NCV7707C/D always operates in slave mode whereas the controller provides the master function. A SPI access is performed by applying an active−low slave select signal at CSB. SI is the data input, SO the data output. The SPI master provides the clock to the NCV7707C/D via the SCLK input. The digital input data is sampled at the rising edge at SCLK. The data output SO is in high impedance state (tri−state) when CSB is high. To readout the global error flag without sending a complete SPI frame, SO indicates the corresponding value as soon as CSB is set to active. With the first rising edge at SCLK after the high−to−low transition of CSB, the content of the selected register is transferred into the output shift register.

The NCV7707C/D provides four control registers (CONTROL_0/1/2/3), two PWM configuration registers (PWM_7/8 and PWM_9/10), three status registers (STATUS_0/1/2) and one general configuration register (CONFIG). Each of these register contains 16−bit data, together with the 8−bit frame header (access type, register address), the SPI frame length is therefore 24 bits. In addition to the read/write accessible registers, the NCV7707C/D provides five 8−bit ID registers (ID_HEADER, ID_VERSION, ID_CODE1/2 and ID_SPI−FRAME) with 8−bit data length. The content of these registers can still be read out by a 24−bit access, the data is then transferred in the MSB section of the data frame.

SPI Frame Format

Figure 10 shows the general format of the NCV7707C/D SPI frame.



24−bit SPI Interface

Both 24−bit input and output data are MSB first. Each SPI−input frame consists of a command byte followed by two data bytes. The data returned on SO within the same frame always starts with the global status byte. It provides general status information about the device. It is then followed by 2 data bytes (in−frame response) which content depends on the information transmitted in the command byte. For write access cycles, the global status byte is followed by the previous content of the addressed register.

Chip Select Bar (CSB)

CSB is the SPI input pin which controls the data transfer of the device. When CSB is high, no data transfer is possible and the output pin SO is set to high impedance. If CSB goes low, the serial data transfer is allowed and can be started. The communication ends when CSB goes high again.

Serial Clock (SCLK)

If CSB is set to low, the communication starts with the rising edge of the SCLK input pin. At each rising edge of SCLK, the data at the input pin Serial IN (SI) is latched. The data is shifted out thru the data output pin SO after the falling edges of SCLK. The clock SCLK must be active only within the frame time, means when CSB is low. The correct transmission is monitored by counting the number of clock pulses during the communication frame. If the number of SCLK pulses does not correspond to the frame width indicated in the SPI−frame−ID (Chip ID Register, address 3Eh) the frame will be ignored and the communication failure bit “TF” in the global status byte will be set. Due to this safety functionality, daisy chaining the SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSB signal of the connected ICs is recommended.

Serial Data In (SI)

During the rising edges of SCLK (CSB is low), the data is transferred into the device thru the input pin SI in a serial way. The device features a stuck−at−one detection, thus upon detection of a command = FFFFFFh, the device will be forced into the Standby mode. All output drivers are switched off.

Serial Data Out (SO)

The SO data output driver is activated by a logical low level at the CSB input and will go from high impedance to a low or high level depending on the global status bit, FLT (Global Error Flag). The first rising edge of the SCLK input after a high to low transition of the CSB pin will transfer the content of the selected register into the data out shift register. Each subsequent falling edge of the SCLK will shift the next bit thru SO out of the device.

Command Byte / Global Status Byte

Each communication frame starts with a command byte (Table 2). It consists of an operation code (OP[1:0], Table 3) which specifies the type of operation (Read, Write, Read & Clear, Readout Device Information) and a six bit address (A[5:0], Table 4). If less than six address bits are required, the remaining bits are unused but are reserved. Both Write and Read mode allow access to the internal registers of the device. A “Read & Clear”−access is used to read a status register and subsequently clear its content. The “Read Device Information” allows to read out device related information such as ID−Header, Product Code, Silicon Version and Category and the SPI−frame ID. While receiving the command byte, the global status byte is transmitted to the microcontroller. It contains global fault information for the device, as shown in Table 6.

ID Register

Chip ID Information is stored in five special 8−bit ID registers (Table 5). The content can be read out at the beginning of the communication.

Table 2. COMMAND BYTE / GLOBAL STATUS BYTE STRUCTURE

Bit	Command Byte (IN) / Global Status Byte (OUT)							
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NCV7707C/D IN	OP1	OP0	A5	A4	A3	A2	A1	A0
NCV7707C/D OUT	FLT	TF	RESB	TSD	TW	UOV_OC	ULD	NRDY
Reset Value	1	0	0	0	0	0	0	1

Table 3. COMMAND BYTE, ACCESS MODE

OP1	OP0	Description
0	0	Write Access (W)
0	1	Read Access (R)
1	0	Read and Clear Access (RC)
1	1	Read Device ID (RDID)

Table 4. COMMAND BYTE, REGISTER ADDRESS

A[5:0]	Access	Description	Content
00h	R/W	Control Register CONTROL_0	Device mode control, Bridge outputs control
01h	R/W	Control Register CONTROL_1	High−side outputs control, ECM control
02h	R/W	Control Register CONTROL_2	Bridge outputs recovery control, PWM enable, ECM setup
03h	R/W	Control Register CONTROL_3	High−side outputs recovery control, PWM enable, Current Sense selection
08h	R/W	PWM Control Register PWM_7/8	PWM control register for OUT7,8
09h	R/W	PWM Control Register PWM_9/10	PWM control register for OUT9,10
10h	R/RC	Status Register STATUS_0	Bridge outputs Overcurrent diagnosis
11h	R/RC	Status Register STATUS_1	Bridge outputs Underload diagnosis
12h	R/RC	Status Register STATUS_2	HS outputs Overcurrent and Underload diagnosis, Vs Over− and Under-voltage, EC−mirror
3Fh	R/W	Configuration Register CONFIG	Mask bits for global fault bits

Table 5. CHIP ID INFORMATION

A[5:0]	Access	Description	Content
00h	RDID	ID header	4300h
01h	RDID	Version	0A00h
02h	RDID	Product Code 1	7700h
03h	RDID	Product Code 2	0700h
3Eh	RDID	SPI−Frame ID	0200h

Table 6. Global Status Byte Content

FLT	**Global Fault Bit**	
0	No fault Condition	Failures of the Global Status Byte, bits [6:0] are always linked to the Global Fault Bit FLT. This bit is generated by an OR combination of all failure bits of the device (RESB inverted). It is reflected via the SO pin while CSB is held low and NO clock signal is present (before first positive edge of SCLK). The flag will remain valid as long as CSB is held low. This operation does not cause the Transmission error Flag in the Global Status Byte to be set. Signals TW and ULD can be masked.
1	Fault Condition	
TF	**SPI Transmission Error**	
0	No Error	If the number of clock pulses within the previous frame was unequal 0 (FLT polling) or 24. The frame was ignored and this flag was set.
1	Error	
RESB	**Reset Bar (Active low)**	
0	Reset	Bit is set to ”0” after a Power−on−Reset or a stuck−at−1 fault at SI (SPI−input data = FFFFFFh) has been detected. All outputs are disabled.
1	Normal Operation	
TSD	**Overtemperature Shutdown**	
0	No Thermal Shutdown	Thermal Shutdown Status indication. In case of a Thermal Shutdown, all output drivers including the charge pump output are deactivated (high impedance). The TSD bit has to be cleared thru a SW reset to reactivate the output drivers and the chargepump output.
1	Thermal Shutdown	
TW	**Thermal Warning**	
0	No Thermal Warning	This bit indicates a pre−warning level of the junction temperature. It is maskable by the Configuration Register (CONFIG.NO_TW).
1	Thermal Warning	
UOV_OC	**VS Monitoring, Overcurrent Status**	
0	No Fault	This bit represents a logical OR combination of under−/overvoltage signals (VS) and overcurrent signals.
1	Fault	
ULD	**Underload**	
0	No Underload	This bit represents a logical OR combination of all underload signals. It is maskable by the Configuration Register (CONFIG.NO_ULDx). It is also possible to deactivate this flag for HS1 or LS1, only (CONFIG.NO_ULD_HS1/LS1).
1	Underload	
NRDY		

SPI REGISTERS CONTENT

CONTROL_0 Register

Address: 00h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	−	−	−	RW
Bit name	HS1	LS1	HS2	LS2	HS3	LS3	HS4	LS4	HS5	LS5	HS6	LS6	0	0	0	MODE
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	HSx	LSx		Description	Remark
HS/LS Outputs OUT1−6 Driver Control	0	0	default	OUTx High impedance	If a driver is enabled by the control register AND the corresponding PWM enable bit is set in CONTROL_2 register, the output is only activated if PWM1 (PWM2) input signal is high. Since OUT1..OUT6 are half−bridge outputs, activating both HS and LS at the same time is prevented by internal logic.
	0	1		LSx enabled	
	1	0		HSx enabled	
	1	1		OUTx High impedance	

	MODE		Description	Remark
Mode Control	0	default	Standby	If MODE is set, the device is switched to Active mode. Resetting MODE forces the device to transition into Standby mode, all internal memory is cleared and all output stages are switched into their default state (off). Delay of tacts should be respected before the Active mode is requested again.
	1		Active	

CONTROL_1 Register
Address: 01h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	−
Bit name	HS7.1	HS7.0	HS8.1	HS8.0	HS9	HS10	HS11	LS ECFB	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0	ECEN	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	HSx.1	HSx.0		Description	Remark
	0	0	default	OUTx High impedance	
HS Outputs OUT7,8 Control					If a driver is enabled by the sn750704 re8o0 0 8 5 ref251.036 628.498 95

CONTROL_2 Register

Address: 02h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Bit name	OCR1	OCR2	OCR3	OCR4	OCR5	OCR6	OCR ECFB	PWMI	OUT1 PWM1	OUT2 PWM1	OUT3 PWM1	OUT4 PWM1	OUT5 PWM2	OUT6 PWM1	ECFB PWM1	FSR
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	OCRx		Description	Remark
Overcurrent Recovery	0	default	Overcurrent Recovery disabled	During an overcurrent event the overcurrent status bit STATUS_0/2.OCx is set and the dedicated output is switched off. (The global multi bit UOV_OC is set, also). When the overcurrent recovery bit is enabled, the output will be reactivated automatically after a programmable delay time (CONTROL_3.OCRF).
	1		Overcurrent Recovery enabled	

	PWMI		Description	Remark
PWM Unit	0	default	Internal PWM unit disabled	The device has three different PWM sources: external pins PWM1, PWM2 and the internal PWM unit which can be used to control the lamp drivers in an additional way. PWMI selects the internal PWM unit.
	1		Internal PWM unit enabled	

	OUTx PWM		Description	Remark
PWM1/2 Selection	0	default	PWMx not selected	For each half−bridge output it is possible to select the PWM input pins PWM1 or PWM2. In this case the dedicated output (selected in CONTROL_0 register) is on if the PWM input signal is high. OUT5 is controlled by PWM2, all other half−bridges are controlled by PWM1.
	1		PWMx selected	

	FSR		Description	Remark
DAC Full−scale Range Control	0	default	Vout = 1.5 / 2^6 ·	

CONTROL_3 Register

Address: 03h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access Type																

	IS3	IS2	IS1	IS0	Description	Remark
Current Sensing Selection	0	0	0	0	OUT1	The current in all high−side power stages (except of OUT2/3) can be monitored at the bidirectional multifunctional pin ISOUT/PWM2. This pin is a multifunctional pin and can be activated as output by setting the current selection bits IS[3:0]. The selected high−side output will be multiplexed to the output ISOUT.
	0	0	0	1	current sensing deactivated	
	0	0	1	0	current sensing deactivated	
	0	0	1	1	OUT4	
	0	1	0	0	OUT5	
	0	1	0	1	OUT6	
	0	1	1	0	OUT7	
	0	1	1	1	OUT8	
	1	0	0	0	OUT9	
	1	0	0	1	OUT10	
	1	0	1	0	OUT11	
	1	0	1	1	current sensing deactivated	
	1	1	0	0	current sensing deactivated	
	1	1	0	1	current sensing deactivated	
	1	1	1	0	current sensing deactivated	
	1	1	1	1	current sensing deactivated	

PWM_7/8 Register
Address: 08h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access Type	RW	RW	RW	RW	RW											

PWM_9/10 Register
Address: 09h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	FSEL9	PW9.6	PW9.5	PW9.4	PW9.3	PW9.2	PW9.1	PW9.0	FSEL 10	PW10.6	PW10.5	PW10.4	PW10.3	PW10.2	PW10.1	PW10.0
Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	PW9[6:0]
PWM Duty Cycle selector for OUT9	

STATUS_0 Register
Address: 10h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access Type	R/RC	R/RC	R/RC	R/RC	R/RC	R/RC	R/RC	R/RC	R/RC	R/RC	R/RC	R/RC	−	−	−	−
Bit Name	OC															

STATUS_2 Register

Address: 12h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access type	R/RC	R/RC	R/RC	R/RC	R/RC	R/RC	R/RC	R/RC	R/RC	R/RC	R/RC	R/RC	R/RC	R/RC	R/RC	R/RC
Bit name	OC HS7	ULD HS7	OC HS8	ULD HS8	OC HS9	ULD HS9	OC HS10	ULD HS10	OC HS11	ULD HS11	OC ECFB	ULD ECFB	VSUV	VSOV	ECLO	ECHI
Reset value																

CONFIG Register

Address: 3Fh

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Access Type	–	–	–	–	–	–	–	–	RW	–	RW	RW	RW	–	RW	–
Bit Name	0	0	0	0	0	0	0	0	ECM LSPWM	0	NO_ULD HS1	NO_ULD LS1	NO_ TW	0	NO_ULD OUTn	0
Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	NO_ULD HS1	NO_ULD LS1		Description	Remark
Global Underload Flag HS1/LS1	0	0	default	Global underload flag at HS1/LS1 active	For ULD_HS1 and ULD_LS1 it is possible to deactivate the global ULD failure bit by setting the configuration bits CONFIG.NO_ULD_HS1/LS1.With setting CONFIG.NO_ULD_OUTn the global ULD failure bit is deactivated in general.
	0	1		No global underload flag at LS1	
	1	0		No global underload flag at HS1	
	1	1		No global underload flag at HS1/LS1	

	NO_TW		Description	Remark
No Thermal Warning Flag	0	default	Thermal warning flag active	The global thermal warning bit TW can be deactivated.
	1		No thermal warning flag active	

	NO_ULD_OUTn		Description	Remark
Global Undeload Flag OUTn	0	default	Global underload flag active	By setting CONFIG.NO_ULD_OUTn the global ULD failure bit is deactivated in general.
	1		No global underload flag active	

	ECM_LSPWM		Description	Remark
ECM PWM Discharge	0	default	LS PWM feature disabled	If this bit is set, automatic PWM discharge on the ECM output is enabled. In case of PWM discharge the Overcurrent recovery feature is disabled, regardless of the setting of CONTROL_2.OC_ECFB.
	1		LS PWM feature enabled	

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