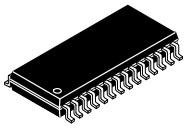
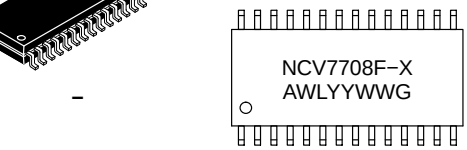
C 7708

The NCV7708F is a fully protected Hex Half Bridge Driver designed specifically for automotive and industrial motion control applications. The six low and high side drivers are freely configurable and can be controlled separately. This allows for high side, low side, and H−Bridge control. H−Bridge control provides forward, reverse, brake, and high impedance states. The drivers are controlled via a standard SPI interface.

- Ultra Low Quiescent Current Sleep Mode
- Six Independent High−Side and Six independent Low−Side Drivers
- Integrated Freewheeling Protection (LS and HS)
- Internal Upper and Lower Clamp Diodes
- Configurable as H−Bridge Drivers
- $R_{DS(on)}$ = 0.6 Ω (typ)
- 5 MHz SPI Control
- SPI Valid Frame Detection
- Compliance with 5 V and 3.3 V Systems
- Overvoltage Lockout
- Undervoltage Lockout
- Fault Reporting
- Current Limit
- Overtemperature Protection
- Internally Fused Lead in SOIC−28
- SSOP−24 NB EPAD
- These are Pb−Free Devices

- Automotive
- Industrial
- DC Motor Management



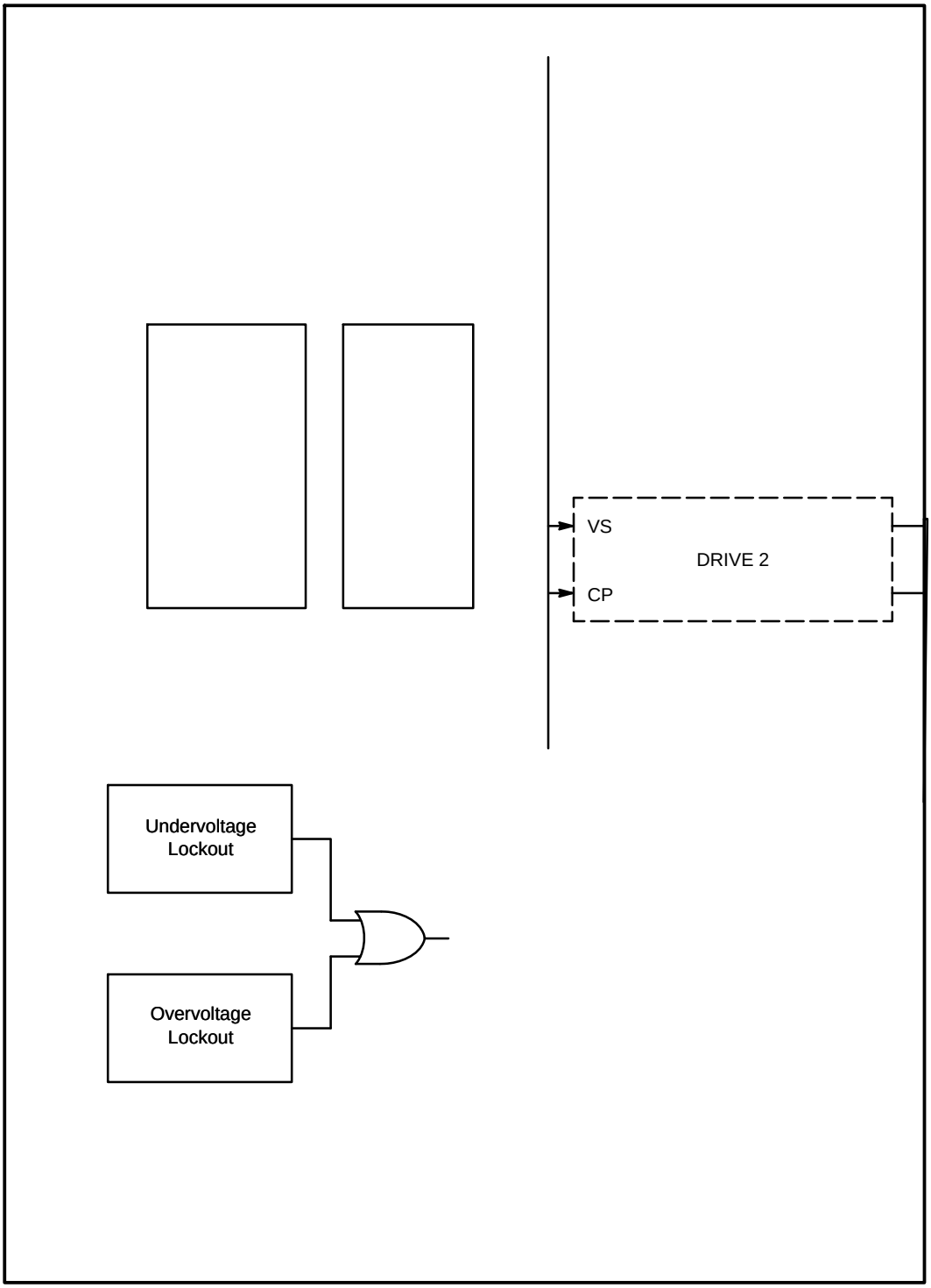


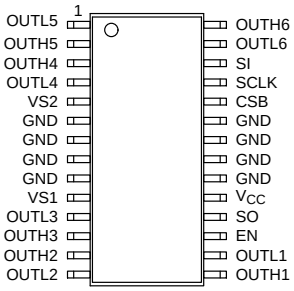
X	= Optional Wafer Fab Indicator
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

		†
NCV7708FDWR2G*	SOIC−28W (Pb−Free)	1000 / Tape & Reel

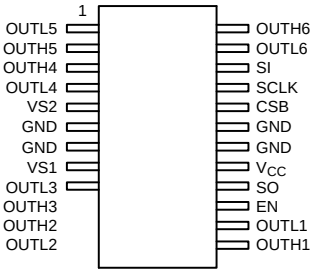
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Publication Order Number:


VS
DRIVE 2
CP
Undervoltage
Lockout
Overvoltage
Lockout



SOIC−28



SSOP−24

Power Supply Voltage (VS1, VS2) (DC) (AC), t < 500 ms, Ivsx > −2 A	 −0.3 to 40 −1.0	V
Output Pin OUTHx (DC) (AC – inductive clamping)	 −0.3 to 40 −8.0	V
Output Pin OUTLx (DC) (AC), t < 500 ms, IOUTLx > −2 A (AC Inductive Clamping)	 −0.3 to 36 −1.0 45	V
Pin Voltage (Logic Input pins, SI, SCLK, CSB, SO, EN, V_{CC})	−0.3 to 5.5	V
Output Current (OUTL1, OUTL2, OUTL3, OUTL4, OUTL5, OUTL6, OUTH1, OUTH2, OUTH3, OUTH4, OUTH5, OUTH6) (DC) Vds = 12 V (DC) Vds = 20 V (DC) Vds = 40 V (AC) Vds = 12 V, (50 ms pulse, 1 s period) (AC) Vds = 20 V, (50 ms pulse, 1 s period) (AC) Vds = 40 V, (50 ms pulse, 1 s period)	 −1.5 to 1.5 −0.7 to 0.7 −0.25 to 0.25 −2.0 to 2.0 −0.9 to 0.9 −0.3 to 0.3	A
Electrostatic Discharge, Human Body Model, VS1, VS2, OUTx (Note 1)		

Digital Supply Input Voltage (V_{CC})	V_{CCmax}	3.15	5.25	V
Battery Supply Input Voltage (V_S)	V_{Smax}	5.5	28	V
DC Output Current (I(OUTLx), I(OUTHx))	DC_{max}	−	0.5	A
Junction Temperature	T_J	−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

(−40°C < T_J < 150°

(−40°C < T_J < 150°C, 5.5 V < VSx < 40 V, 3.15 V < V_{CC} < 5.25 V, EN = V_{CC}, unless otherwise specified)

Sink Leakage Current	I_{snk}	OUTL(1−6) = 34 V, V_{CC} = 5 V OUTL(1−6) = 34 V, V_{CC} = 5 V, T = 25°C	− −	− −	5.0 1.0	μA
Power Transistor Body Diode Forward Voltage	V_{bd_fwd}	I_F = 500 mA	−	0.9	1.3	V
High−Side Clamping Voltage (Note 7)	V_{clp_hs}	$I_{(OUTHx)}$ =				

(−40°C < T_J < 150°C, 5.5 V < VSx < 40 V, 3.15 V < V_{CC} < 5.25 V, EN = V_{CC}, unless otherwise specified)

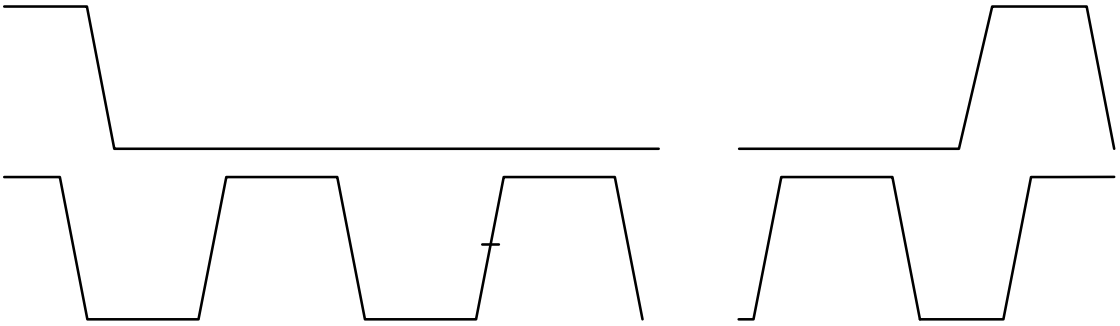
Low Side Turn Off Time	t_{lsoff}	Vs = 13.2 V, R_{load} = 25 Ω	−	2.0	5.0	μs
High Side Rise Time	t_{hsr}	Vs = 13.2 V, R_{load} = 25 Ω	−	4.0	8.0	μs
High Side Fall Time	t_{hsf}	Vs = 13.2 V, R_{load} = 25 Ω	−	2.0	3.0	μs
Low Side Rise Time	t_{lsr}	Vs = 13.2 V, R_{load} = 25 Ω	−	1.0	2.0	μs
Low Side Fall Time	t_{lsf}	Vs = 13.2 V, R_{load} = 25 Ω	−	1.0	3.0	μs
Non−Overlap Time	$t_{hsOfflsOn}$	High Side Turn Off To Low Side Turn On	1.5	−	−	μs
Non−Overlap Time	$t_{lsOffhsOn}$	Low Side Turn Off To High Side Turn On	1.5	−	−	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. For temperatures above 85°C, refer to graphs for VSx and V_{CC} Sleep Current vs. Temperature on page 17.
6. Thermal characteristics are not subject to production test.
7. Refer to “Typical High−Side Negative Clamp Voltage” graph on page 17.
8. Current limit is active with and without overcurrent detection.
9. Not production tested.

(−40°C < T_J < 150°C, 5.5 V < VSx < 40 V, EN = V_{CC} = 5 V, unless otherwise specified)

(V_{CC} = 5 V)						
SCLK Frequency		f_{SCLK}	−	−	5.0	MHz
SCLK Clock Period	V_{CC} = 5 V V_{CC} = 3.3 V	t_{SCLK}	200 500	− −	− −	ns
SCLK High Time		t_{CLKH}	85	−	−	ns
SCLK Low Time		t_{CLKL}	85	−	−	ns
SCLK Setup Time		t_{CLKSU1} t_{CLKSU2}	85 85	− −	− −	ns

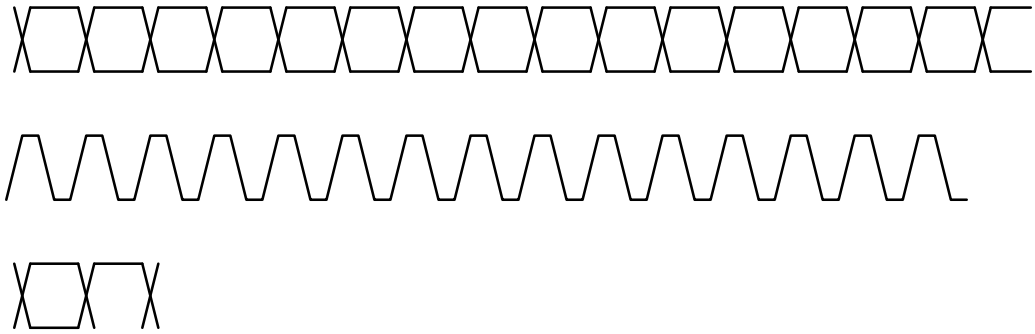


Standard 16−bit communication has been implemented for the communication of this IC to turn drivers on and off, and to report faults. (Reference the SPI Communication Frame Format Diagram). The LSB (Least Significant Bit) is clocked in first.

For SPI communication, the device must first be enabled (EN = high). The SPI inputs are TTL compatible and the SO output high level is defined by the applied VCC. The active-low CSB input has a pull−up resistor. SPI communication is active when CSB is low. Providing a pull-up resistor insures the communication bus is not active should the communication link between the microcontroller and NCV7708F become open. SCLK and SI have pull−down resistors. This provides known states when the SPI is not active.

Communication is implemented as follows:

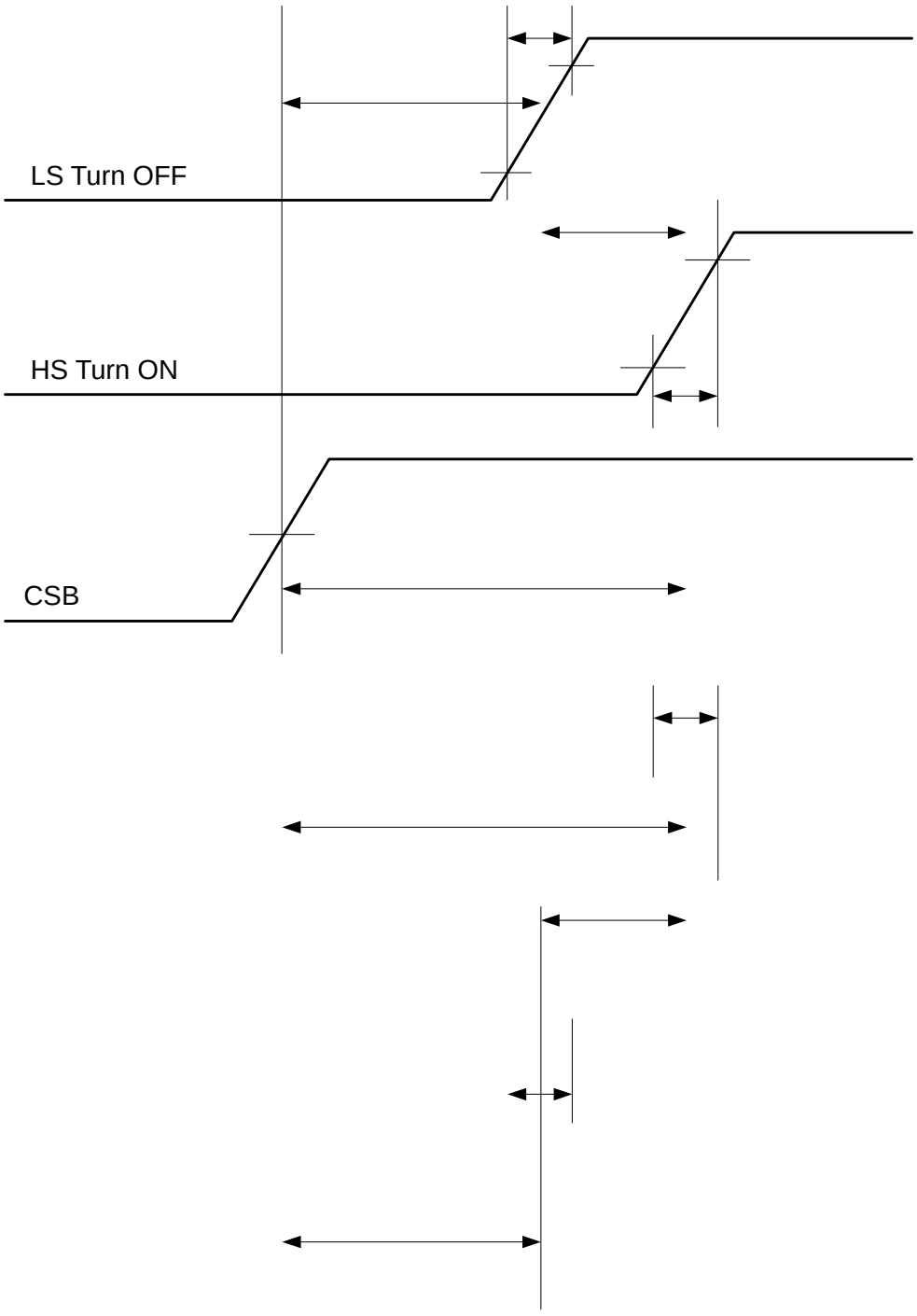
1. CSB goes low to allow serial data transfer.
2. A 16 bit word is clocked (SCLK) into the SI (serial input) pin. The SI input signal is latched on the falling edge of SCLK.
3. Current SO data is simultaneously shifted out on every rising edge of SCLK starting with the LSB (TW).
4. CSB goes high to transfer the clocked in information to the data registers.
   (Note: SO is tristate when CSB is high.)
5. The SI data will be accepted when a valid SPI frame is detected. A valid SPI frame consists of the above conditions and a complete set of multiples of 16 bit words. Invalid frames are ignored with previous input data intact.



The table below defines the programming bits and diagnostic bits. Fault information is sequentially clocked out the SO pin of the NCV7708F as programming information is clocked into the SI pin of the device. Daisy chain communication between SPI compatible IC's is possible by connection of the serial output pin (SO) to the input of the sequential IC (SI).

15	Overvoltage Lock Out Control (OVLO)	0 = Disable 1 = Enable
14	Under Load Detection Shut Down Control (ULD)	0 = Disable 1 = Enable
13	Overcurrent Detection Shut Down Control (OCD)	0 = 200 μsec 1 = 25 μsec
12	OUTH6	0 = Off 1 = On
11	OUTL6	0 = Off 1 = On
10	OUTH5	0 = Off 1 = On
9	OUTL5	0 = Off 1 = On
8	OUTH4	0 = Off 1 = On
7	OUTL4	0 = Off 1 = On
6	OUTH3	0 = Off 1 = On
5	OUTL3	0 = Off 1 = On
4	OUTH2	0 = Off 1 = On
3	OUTL2	0 = Off 1 = On
2	OUTH1	0 = Off 1 = On
1	OUTL1	0 = Off 1 = On
0	Status Register Reset (SRR)	0 = No Reset 1 = Reset

15	Power Supply Fail Signal (OVLO or UVLO = PSF)	0 = No Fault 1 = Fault
14	Under Load Detect Signal (ULD)	0 = No Fault 1 = Fault
13	Over Load Detect Signal (OLD)	0 = No Fault 1 = Fault
12	OUTH6*	0 = Off 1 = On
11	OUTL6*	0 = Off 1 = On
10	OUTH5*	0 = Off 1 = On
9	OUTL5*	0 = Off 1 = On
8	OUTH4*	0 = Off 1 = On
7	OUTL4*	0 = Off 1 = On
6	OUTH3*	0 = Off 1 = On
5	OUTL3*	0 = Off 1 = On
4	OUTH2*	0 = Off


LS Turn OFF
HS Turn ON
CSB

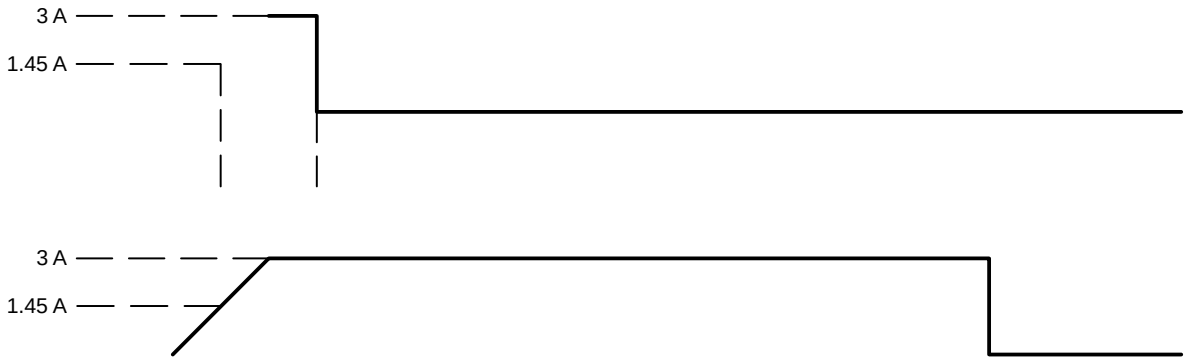
There are two protection mechanisms for output current, overcurrent and current limit.

1. Current limit − Always active with a typical threshold of 3 A.
2. Overcurrent Detection − Selectable shutdown time via Bit 13 with a typical threshold of 1.45 A.

Figure 6 shows the typical performance of a part which has exceeded the 1.45 A Overcurrent Detection threshold and started the shutdown control timer. When Bit 13 = 1, the shutdown time is 25 μsec. When Bit 13 = 0, the shutdown time is 200 μsec.

Once an Overcurrent Shutdown Delay Time event has been detected by the NCV7708F, the timer setting cannot be interrupted by an attempted change via a SPI command of Bit 13.

0	200 μsec
1	25 μsec

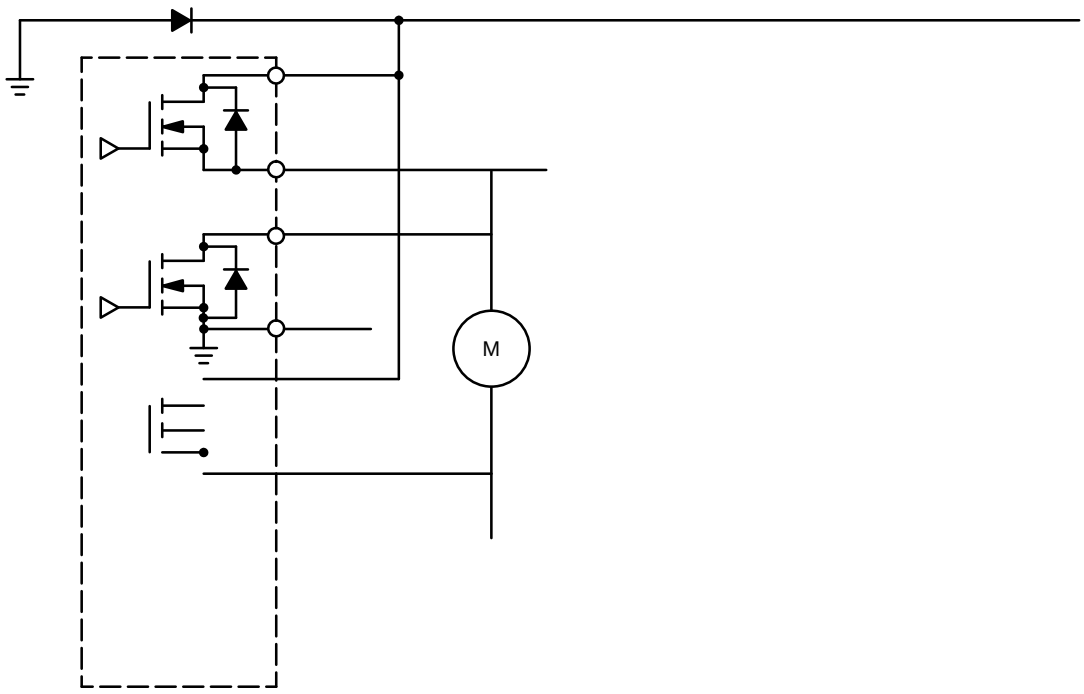


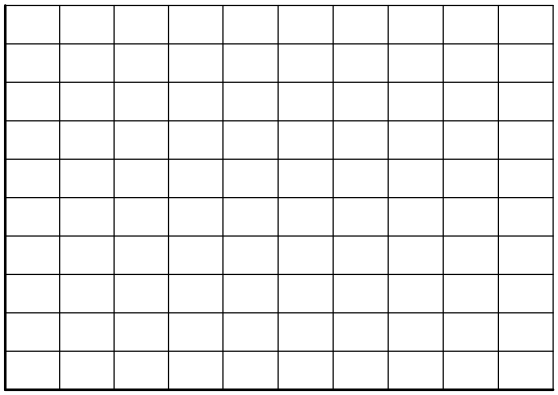
The under−load detection is accomplished by monitoring the current from each output driver. A minimum load current (this is the maximum detection threshold) is required when the drivers are turned on. If the under−load circuit detection

Six independent thermal shutdown circuits are featured (one common sensor for each HS and LS transistor pair). Each sensor has two levels, one to give a Thermal Warning (TW) and a higher one, Thermal Shutdown, which will shut the drivers off. When the part reaches the temperature point of Thermal Warning, the output data bit 0 (TW) will be set

The applications drawing below displays the range with which this part can drive a multitude of loads.

1. H−Bridge Driver configuration
2. Low Side Driver
3. High Side Driver





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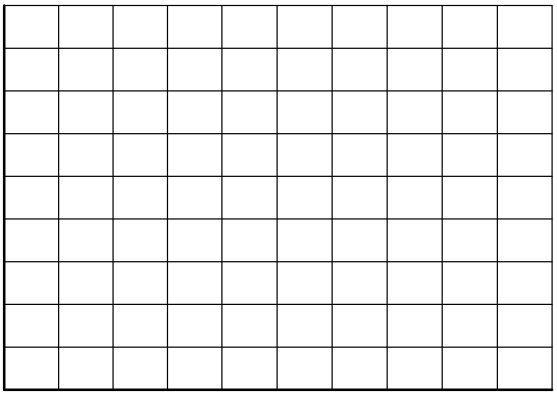
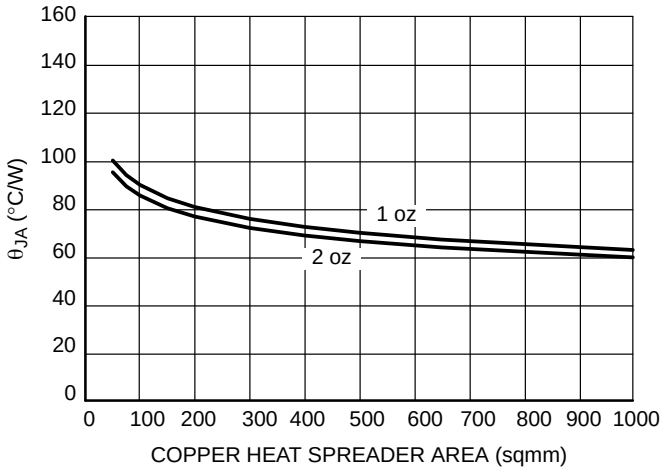
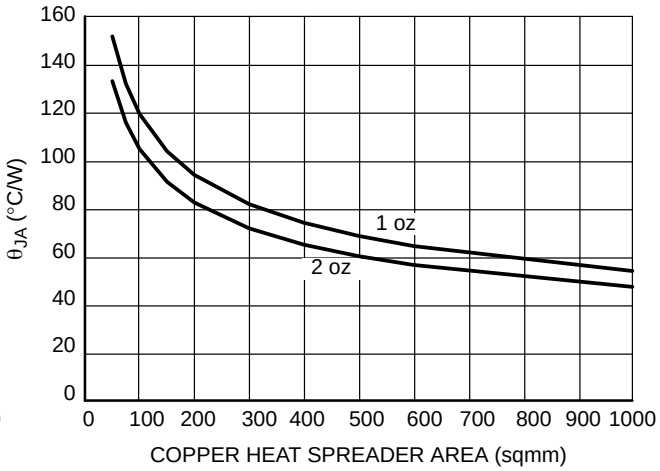
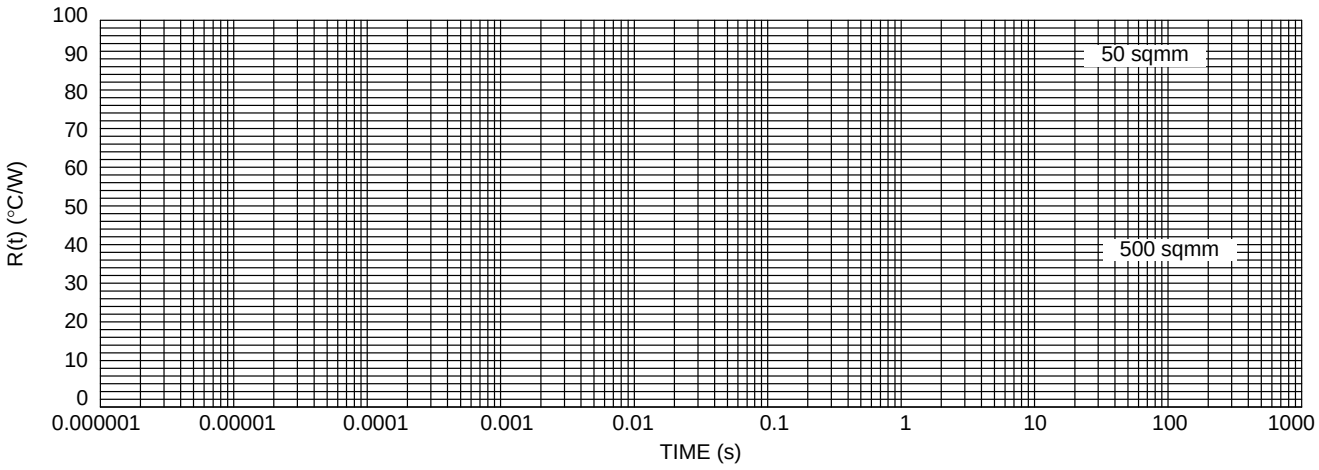



160
140
120
100
80
60
40
20
0
θJA (°C/W)
1 oz
2 oz
0 100 200 300 400 500 600 700 800 900 1000
COPPER HEAT SPREADER AREA (sqmm)

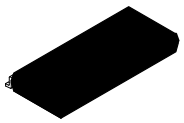
– θ


160
140
120
100
80
60
40
20
0
θJA (°C/W)
1 oz
2 oz
0 100 200 300 400 500 600 700 800 900 1000
COPPER HEAT SPREADER AREA (sqmm)

θ


100
90
80
70
60
50
40
30
20
10
0
R(t) (°C/W)
50 sqmm
500 sqmm
0.000001 0.00001 0.0001 0.001 0.01 0.1 1 10 100 1000
TIME (s)

–

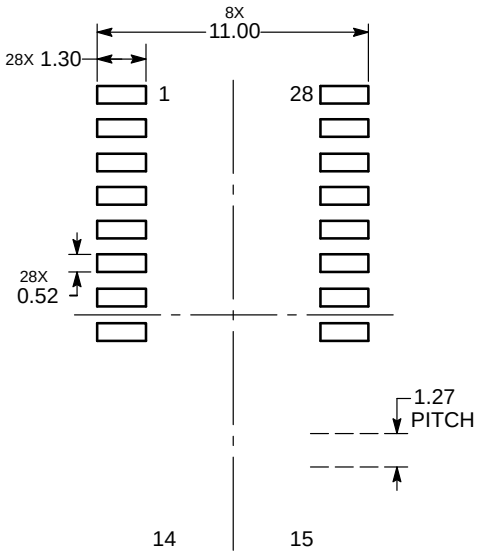


SCA E 1:1

SOIC−28 WB
CASE 751F
ISSUE J

DATE 23 SEP 2015

SOLDERING FOOTPRINT*

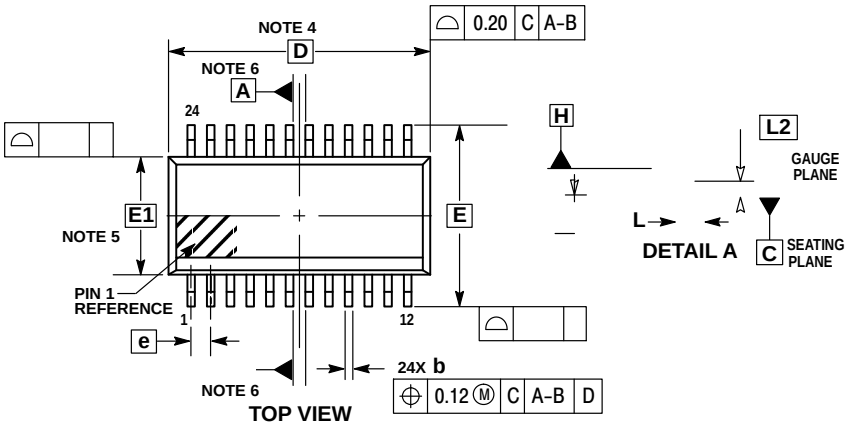


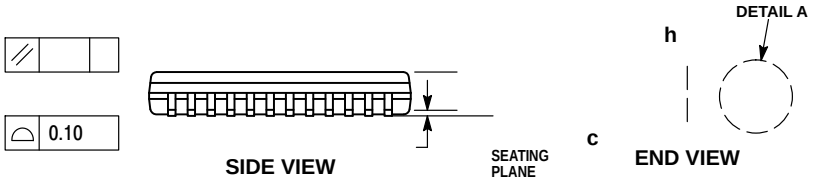
DIMENSIONS: MILLIMETERS

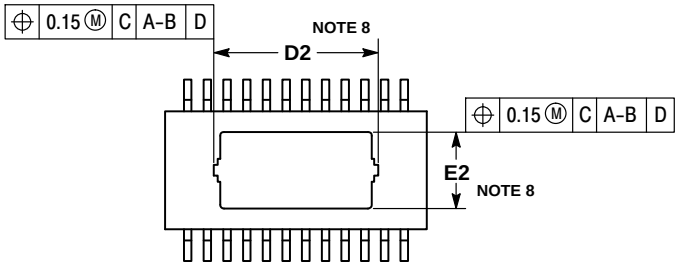
SSOP24 NB EP
CASE 940AK
ISSUE O

SCALE 1:1

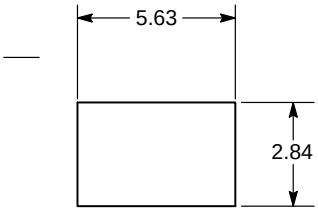
DATE 24 APR 2012







SOLDERING FOOTPRINT



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.10 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. DIMENSION b APPLIES TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D IS DETERMINED AT DATUM PLANE H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM PLANE H.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. CONTOURS OF THE THERMAL PAD ARE UNCONTROLLED WITHIN THE REGION DEFINED BY DIMENSIONS D2 AND E2.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.70
A1	0.00	0.10
b	0.19	0.30
c	0.09	0.20

D2	5.28	5.58

E1	3.90 BSC	
E2	2.44	2.64
e	0.65 BSC	
h	0.25	0.50
L	0.40	0.85
L1	1.00 REF	
L2	0.25 BSC	
M	0°	8°