NCV7718B, NCV7718C

Hex Half-Bridge Driver

The NCV7718B/C is a Hex Half Bridge Driver with protection features designed specifically for automotive and industrial motion control applications. The NCV7718B/C has independent controls and diagnostics. The device can be operated in forward, reverse, brake, and high impedance states. The drivers are controlled via a 16 bit SPI interface and are daisy chain compatible.

Features

- Low Quiescent Current Sleep Mode
- High Side and Low Side Drivers Connected in a Half Bridge Configuration
- Integrated Freewheeling Protection (LS and HS)
- 0.55 A Peak Current
- $R_{DS(on)}$ = 1 Ω (typ)
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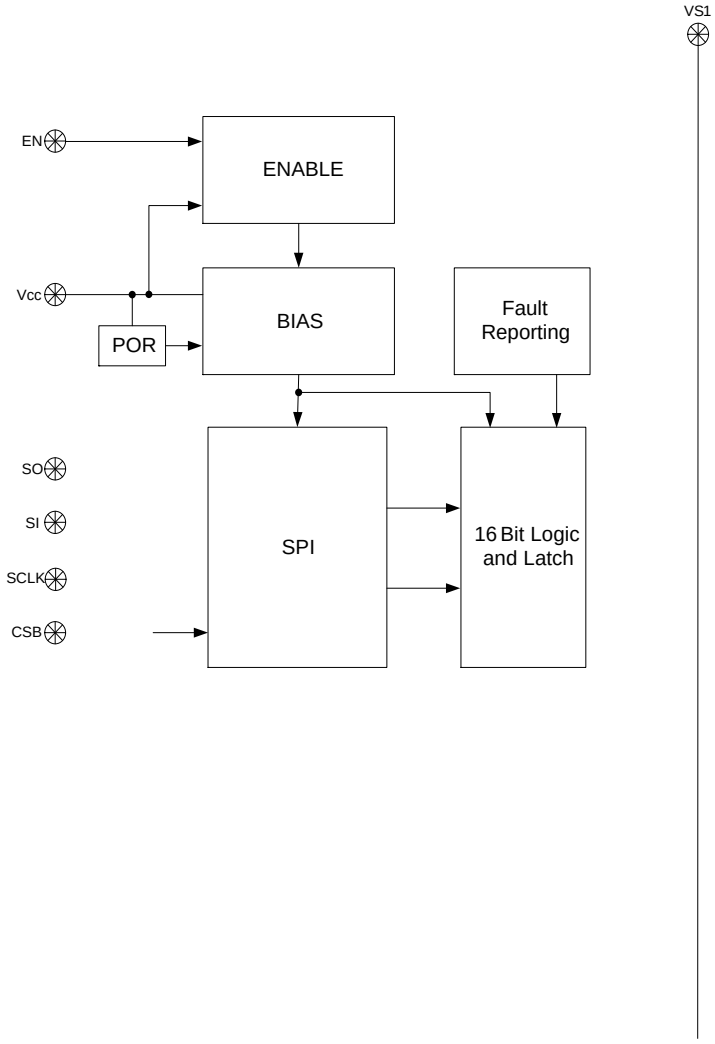
SSOP−24
DP
CASE


VS1
EN
ENABLE
Vcc
BIAS
Fault Reporting
POR
SO
SI
SCLK
CSB
SPI
16 Bit Logic and Latch

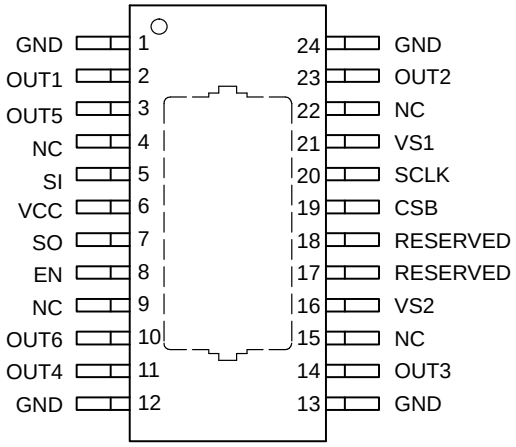


Figure 3. Pinout − SSOP24 NB and SSOP24 NB EP (Top View)

PACKAGE PIN DESCRIPTION: SSOP24 NB, SSOP24 NB EP

Pin #	Symbol	Description
1	GND	Ground. Shorted to pin 24 internally.
2	OUT1	Half Bridge Output 1
3	OUT5	Half Bridge Output 5
4	NC	

MAXIMUM RATINGS

ELECTRICAL CHARACTERISTICS

(−40°C < T_J < 150°C, 5.5 V < VSx < 40 V, 3.15 V < V_{CC} < 5.25 V, EN = V_{CC}, unless otherwise specified)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
GENERAL						
Supply Current (VS1 + VS2) Sleep Mode	IqVsx85	VS1 = VS2 = 13.2 V, V_{CC} = 0 V −40°C to 85°C No Load	–	1.0	2.5	μA
Supply Current (VS1 + VS2) Active Mode	IvsOp	EN = V_{CC}, 5.5 V ≤ VSx < 28 V No Load				

ELECTRICAL CHARACTERISTICS

(−40°C < T_J < 150°C, 5.5 V < VSx < 40 V, 3.15 V < V_{CC} < 5.25 V, EN = V_{CC}, unless otherwise specified)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
BODY DIODE						
Power Transistor Body Diode Forward Voltage	VbdFwd	If = 500 mA	–	0.9	1.3	V
LOGIC INPUTS (EN, SI, SCLK, CSB)						
Input Threshold High Low	VthInH VthInL		 2.0 –	 – –	 – 0.6	V
Input Hysteresis (SI, SCLK, CSB)	VthInHys		50	150	300	mV
Enable Hysteresis	VthENHys		150	400	800	mV
Input Pull−down Resistance (EN, SI, SCLK)	Rpdx	EN = SI = SCLK = V_{CC}	50	125	200	kΩ
Input Pull−up Resistance (CSB)	RpuCSB	CSB = 0 V	50	125	250	kΩ
Input Capacitance	Cinx	Not ATE tested	–	––	15	pF
LOGIC OUTPUT (SO)						
Output High	VsoH	I_{SOURCE} = −1 mA	V_{CC} – 0.6	–	–	V
Output Low	VsoL	I_{SINK} = 1.6 mA	–	–	0.4	V
Tri−state Leakage	ItriStLkg	CSB = 5 V	−5	–	5	μA
Tri−state Output Capacitance	ItriStCout	CSB = V_{CC}, 0 V < V_{CC} < 5.25 V Not ATE tested	–	–	15	pF

ELECTRICAL CHARACTERISTICS (−40°C < TJ < 150°C, 5.5 V < VSx < 40 V, 3.15 < Vcc < 5.25 V, EN= Vcc, unless otherwise specified)

Characteristic	Symbol	Conditions	Timing Chart	Min	Typ	Max	Unit
DRIVER OUTPUT TIMING SPECIFICATIONS							
High Side Turn On Time	ThsOn	VSx = 13.2 V, R_{load} = 39 Ω		–	7.5	13	μs
High Side Turn Off Time	ThsOff	VSx = 13.2 V, R_{load} = 39 Ω		–	3.0	6.0	μs
Low Side Turn On Time							

ELECTRICAL CHARACTERISTIC TIMING DIAGRAMS

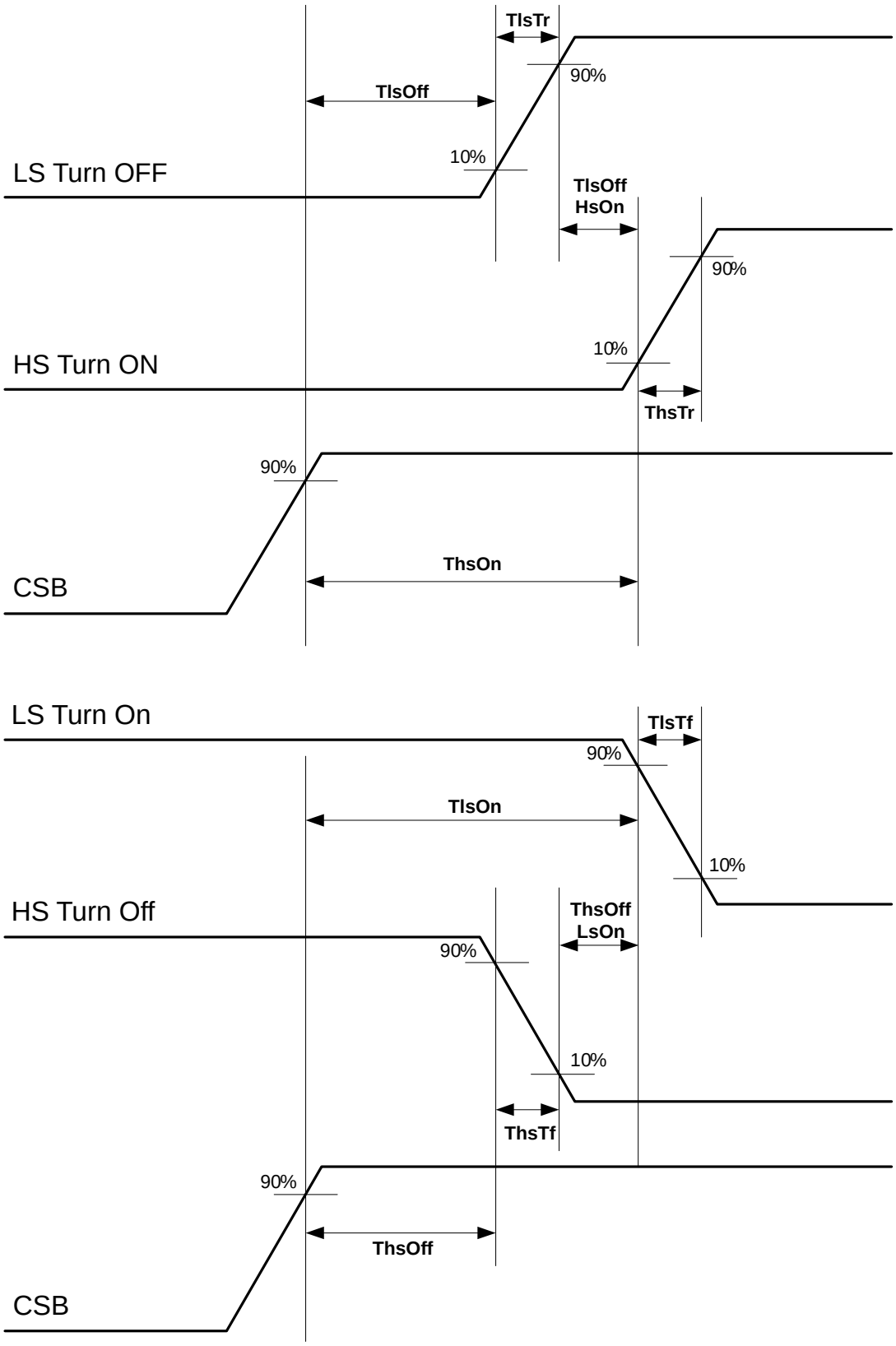
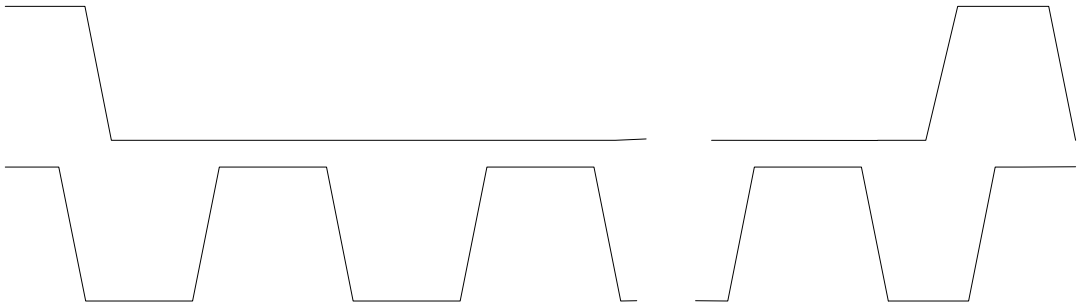


Figure 4. Detailed Driver Timing



TYPICAL PERFORMANCE GRAPHS

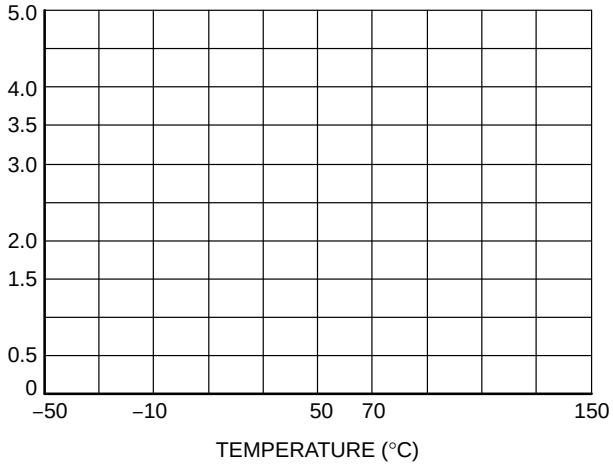


Figure 6. IqTot vs. Temperature

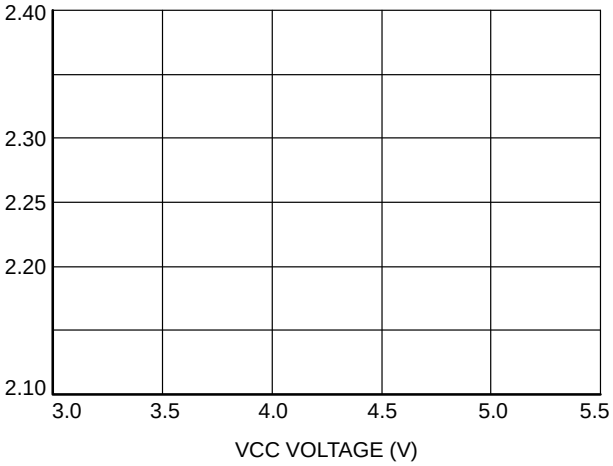


Figure 7. I(V_{CC}) Active Mode vs. V(V_{CC})

TEMPERATURE (°C)

Figure 8. $R_{DS(on)}$ vs. Temperature

TEMPERATURE (°C)

Figure 9. $R_{DS(on)}$ vs. Temperature

TEMPERATURE (°C)

Figure 10. Body Diode vs. Temperature

TEMPERATURE (°C)

Figure 11. Overcurrent vs. Temperature

TYPICAL PERFORMANCE GRAPHS

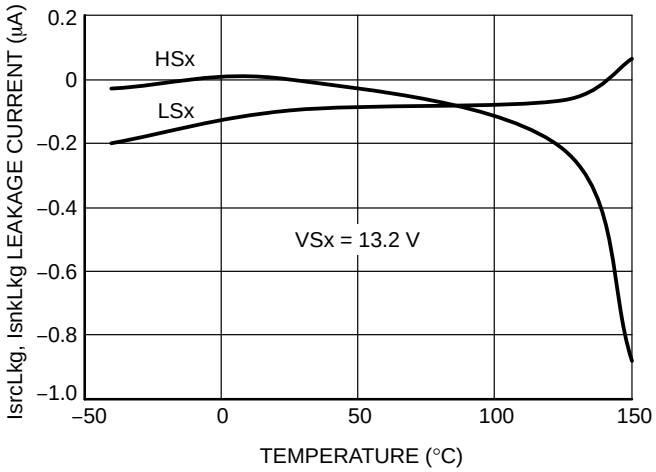


Figure 12. Source−Sink Leakage vs. Temperature

OPERATING DESCRIPTION

General Overview

The NCV7718B/C is comprised of twelve DMOS power drivers (six PMOS High Side Driver and six NMOS Low Side Driver) configured as six half bridges that enables three independent Full Bridge operations. Each output drive is characterized for a max 550 mA DC load and has a typical 2 A surge capability (at VSx =13.2 V). Strict adherence to integrated circuit die temperature is necessary. Maximum die temperature is 150°C. This may limit the number of drivers enabled at one time. Output drive control and fault reporting is handled via the SPI (Serial Peripheral Interface) port.

An Enable function (EN) provides a low quiescent sleep current mode when the device is not being utilized. No data is stored when the device is in sleep mode. An internal pull down resistor is provided on the EN input to ensure the device is off if the input signal is lost. De asserting the EN signal clears all the registers and resets the driver. When the EN signal is asserted the IC will proceed with the V_{CC} POR cycle and brings the drivers into normal operation.

SPI Communication

16 bit full duplex SPI communication has been implemented for the communication of this IC for device configurations, driver controls and reading the diagnostic data. In addition to the 16 bit diagnostic data, a pseudo bit (PRE_15) can also be retrieved from the SO register. The part is required to be enabled (EN active high) for SPI communication. The inputs for the SPI are TTL logic compatible and are specified by the VthInH and VthInL thresholds. The active low CSB input has a pull up resistor and the remaining SPI inputs have pull down resistors to bias them to a known state when SPI is not active.

Reference the SPI communication frame format diagram in Figure 13 for the 16 bit SPI implementation. Tables 1 and 2 define the programming bits and diagnostic bits shown in Figure 13.

SPI COMMUNICATION FRAME FORMAT

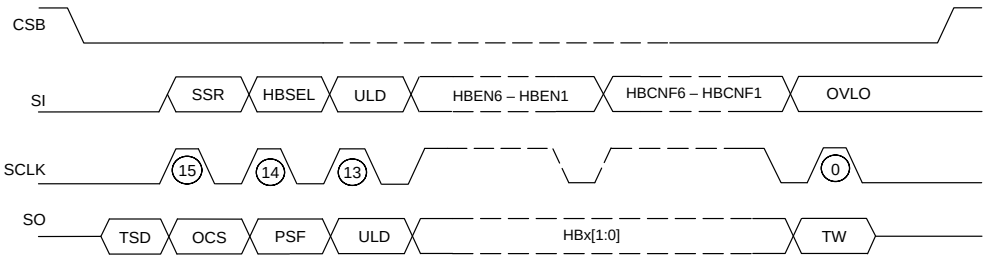


Figure 13. SPI Communication Frame Format

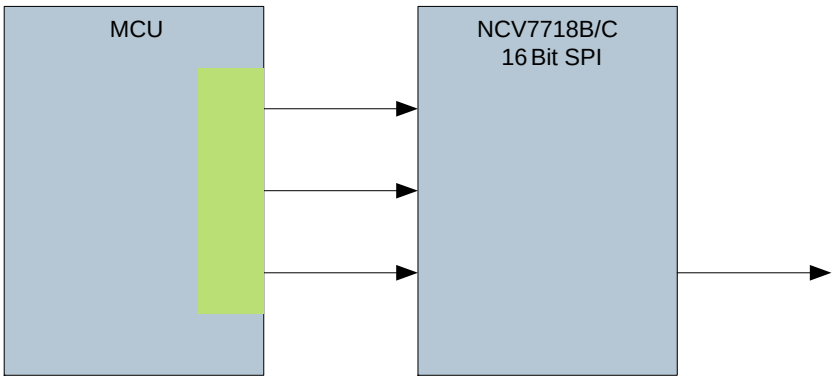
Communication is implemented as follows and is also illustrated in Figure 16:

1. SI and SCLK are set to low before the CSB cycle.
2. CSB goes low to allow serial data transfer.
3. SI data starting with the Most Significant bit (MSB) is shifted in first.
4. SI data is recognized on every falling edge of the clock.
5. Simultaneously, SO data from the previous frame starting with the MSB bit is shifted out on every rising edge of the clock.
6. The input data is compared to a 16 bit counter for the initial 16 bits shifted into SI for frame detection error scheme.
7. The sequential input bits are compared to a *n* x 8 (*n* can take on the value of any integer) bit counter for daisy chain operations and are monitored by the frame detection error scheme.
8. CSB goes high and the most recent 16 bits clocked into SI are transferred to the data register given that there is no frame detection error. Otherwise the entire frame is ignored.
9. SO is tri state when CSB is high.

Table 1. SPI INPUT DATA FRAME

Input Data			
Bit Number	**Bit Name**	**Bit Description**	**Bit Status**
15	SRR	Status Reset Register When Asserted All Latched Faults are Cleared (TSD, OCS & ULD)	0 = No Reset
			1 = Reset
14	HBSEL (Note 8)	Half Bridge Selection	Reserved
13	ULDSC	Under Load Detection Shutdown Control Global Enable; Per Half Bridge Operation	0 = Disable
			1 = Enable
12	HBEN6	Half Bridge 6 Enable	0 = High Z
			1 = Enabled
11	HBEN5	Half Bridge 5 Enable	0 = High Z
			1 = Enabled
10	HBEN4	Half Bridge 4 Enable	0 = High Z
			1 = Enabled
9	HBEN3	Half Bridge 3 Enable	0 = High Z
			1 = Enabled
8	HBEN2	Half Bridge 2 Enable	0 = High Z
			1 = Enabled
7	HBEN1	Half Bridge 1 Enable	0 = High Z
			1 = Enabled
6	HBCNF6	Half Bridge 6 Configuration Control	0 = LS6 ON & HS6 OFF
			1 = LS6 OFF & HS6 ON
5	HBCNF5	Half Bridge 5 Configuration Control	0 = LS5 ON & HS5 OFF
			1 = LS5 OFF & HS5 ON
4	HBCNF4	Half Bridge 4 Configuration Control	0 = LS4 ON & HS4 OFF
			1 = LS4 OFF & HS4 ON
3	HBCNF3	Half Bridge 3 Configuration Control	0 = LS3 ON & HS3 OFF
			1 = LS3 OFF & HS3 ON
2	HBCNF2	Half Bridge 2 Configuration Control	0 = LS2 ON & HS2 OFF
			1 = LS2 OFF & HS2 ON
1	HBCNF1	Half Bridge 1 Configuration Control	0 = LS1 ON & HS1 OFF
			1 = LS1 OFF & HS1 ON
0	OVLO	Over Voltage Lock Out Global Effect	0 = Disable
			1 = Enable

8. HBSEL enables bridge selection for the NCV7719 and NCV7720 devices. In the NCV7718B/C it is recommended to set the HBSEL to zero.


MCU
NCV7718B/C
16 Bit SPI

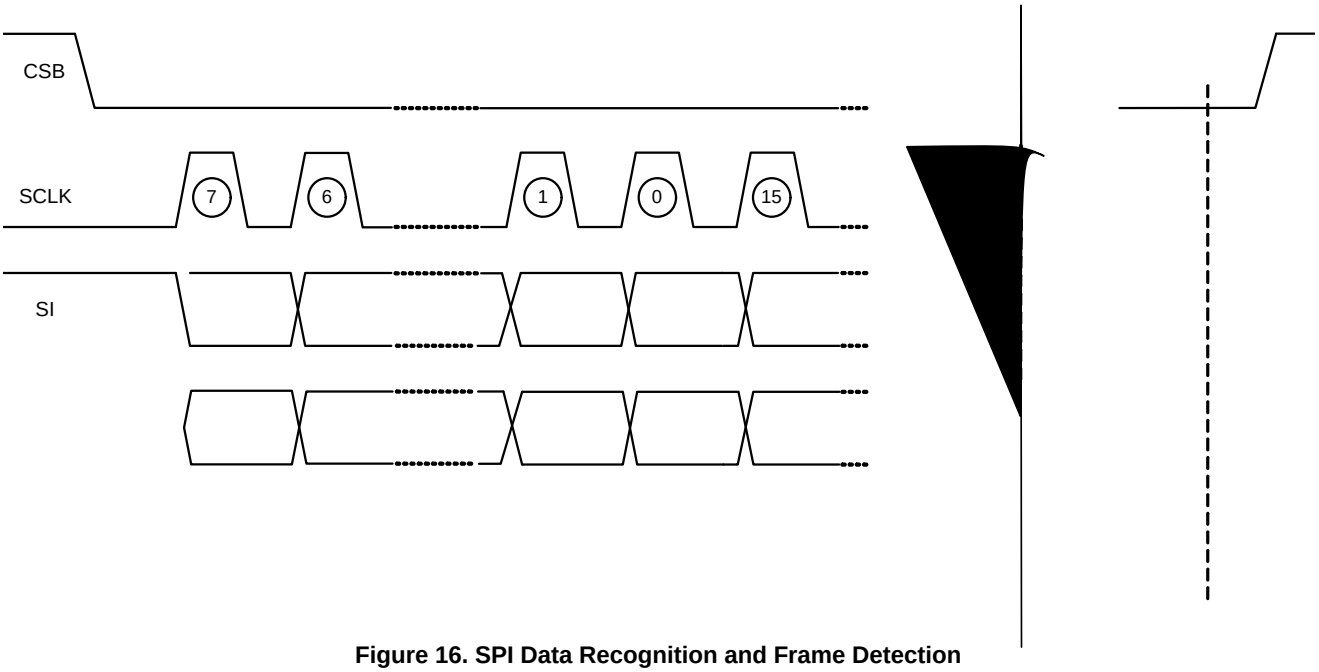


Figure 16. SPI Data Recognition and Frame Detection

Over Voltage Shutdown

Over voltage shutdown circuitry monitors the voltage on the VS1 and VS2 pins, which permits a 40 V maximum. When the Over voltage Threshold level has been breached on the VS1or VS2 supply input, the output bit 14 (PSF) will be set. Additionally, if the input bit 0 (OVLO) is asserted, all outputs will turn off. During an Over Voltage Lockout condition the turn on/off status is maintained in the logic circuitry. When proper input voltage levels are re established, the programmed outputs will turn back on. Over voltage shutdown can be disabled by using the SPI input bit 0 (OVLO = 0) to run through a load dump situation. It is highly recommended to operate the part with OVLO bit asserted to ensure that the drivers remain off during a load dump scenario.

The table below describes the driver status when enabling/disabling the over voltage lock out feature during normal and overvoltage situations.

Table 3. OVER−VOLTAGE LOCK OUT (OVLO)

OVLO Input Bit	VSx OVLO Condition	Output Data Bit 14 Power Supply Fail (PSF) Status	OUTx Status
0	0	'0'	Not in Overvoltage Outputs Unchanged
0	1	'1'	

Over Current Detection and Shutdown

The NCV7718B/C offers over current shutdown protection on the OUTx pins by monitoring the current on the high side and low side drivers. If the over current threshold is breached, the corresponding output is latched off (HS and LS driver is latched off) after the specified shutdown time, TdOc. Upon over current shutdown, the serial output bit OCS will be set and the corresponding

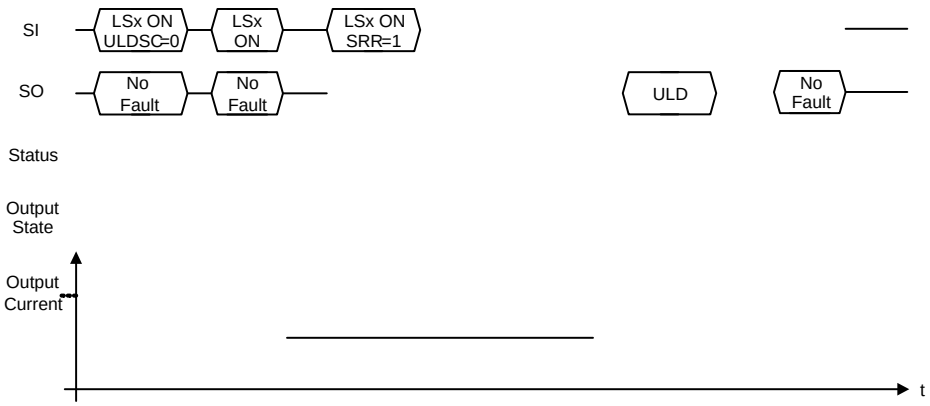


Figure 23. LS Under−load Timing Diagram

Fault Handling

At an event of a driver latched off fault, the offending half bridge driver is disabled and the half bridge configuration is defaulted to zero (HBENx =0, HBCNFx = 0). The user is required to clear the output register fault and to resend the proper SPI frame to turn on the drivers. A driver that is locked out during a fault conditions auto recovers to the previous programmed state when the fault is resolved. A latched fault flag on the serial output doesn't always translate an output latched off fault.

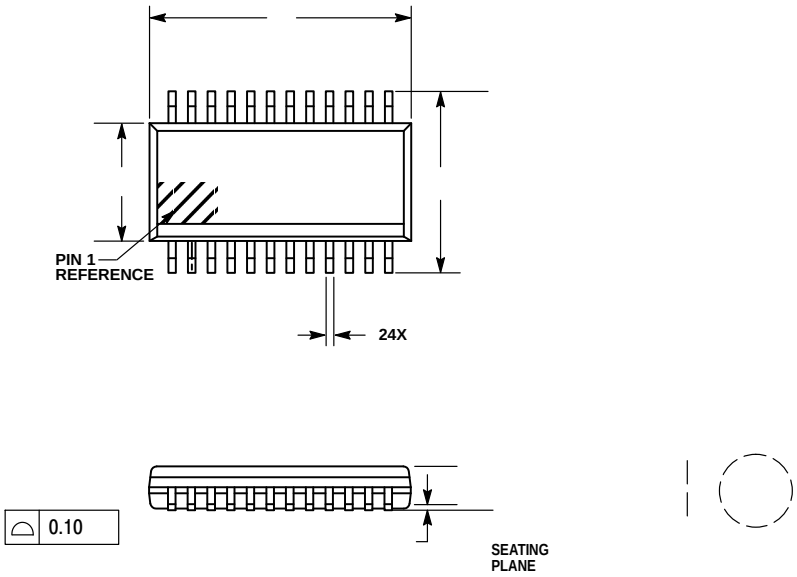
The summary of all fault conditions, the driver status and the clear requirements are provided in Table 5.

Table 5. FAULT SUMMARY

Fault	Fault Memory Serial Output Bit	Driver Condition During Fault	Driver Condition after Parameters Within Specified Limits	Output Register Clear Requirement
Under Load (ULDSC = 0)	Latched	Outputs Unchanged. Allowed to turn/ remain on	Allowed to turn/remain on	Valid SPI frame with SRR set to 1
Under Load (ULDSC = 1)	Latched (Note 9)	Offending Half−Bridge is Latched Off (LS and HS)	Offending Half−Bridge is Latched Off (LS and HS)	Valid SPI frame with SRR set to 1
Over Current	Latched (Note 9)	Offending Output is Latched Off (LS and HS)	Offending Output is Latched Off (LS and HS)	Valid SPI frame with SRR set to 1
Thermal Warning	Non−Latched	Outputs Unchanged. Allowed to turn/ remain on provided that device is not in thermal shutdown	Allowed to turn/remain on	Temp below (thermal warning temp – hysteresis)
Thermal Shutdown	Latched (Note 9)	Offending Half−Bridge Drivers are Latched Off (LS and HS)	Offending Half−Bridge is Latched Off (LS and HS)	Valid SPI frame with SRR set to 1. Temperature blow (thermal shutdown – hysteresis)
VS Power Supply Fail (Over−Voltage: OVLO = 0)	Non−Latched	Outputs Unchanged. Allowed to turn/ remain on	Allowed to turn/remain on	VS below (Over Voltage Threshold – hysteresis)
VS Power Supply Fail (Over−Voltage: OVLO = 1)				

PACKAGE DIMENSIONS

SSOP24 NB EP
CASE 940AK
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.10 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. DIMENSION b APPLIES TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D IS DETERMINED AT DATUM PLANE H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM PLANE H.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. CONTOURS OF THE THERMAL PAD ARE UNCONTROLLED WITHIN THE REGION DEFINED BY DIMENSIONS D2 AND E2.

	MILLIMETERS	
DIM	MIN	MAX
A		1.70
A1	0.00	0.10
b	0.19	0.30
c	0.09	0.20
e	0.65 BSC	
h	0.25	0.50
L	0.40	0.85
L2	0.25 BSC	
M	0°	8°

PACKAGE DIMENSIONS