NCV7719

Octal Half-Bridge Driver

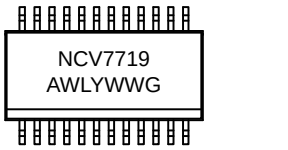
The NCV7719 Octal is an eight channel half-bridge driver with protection features designed specifically for automotive and industrial motion control applications. The product has independent controls and diagnostics, and the drivers can be operated in forward, reverse, brake, and high impedance states. The device is controlled via a 16 bit SPI interface and is daisy chain compatible.

Features

- Low Quiescent Current Sleep Mode
- High−Side and Low−Side Drivers Connected in Half−Bridge Configurations
- Integrated Freewheeling Protection (LS and HS)
- 0.55 A Peak Current
- $R_{DS(on)}$ = 1.0 □ (typ)
- 5 MHz SPI Communication
- 16 Bit Frame Error Detection
- Daisy Chain Compatible with Multiple of 8 bit Devices
- Compliance with 3.3 V and 5 V Systems
- Undervoltage and Overvoltage Lockout
- Discriminated Fault Reporting
- Over Current Protection
- Over−temperature Protection
- Underload Detection
- Exposed Pad Package
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This is a Pb−Free Device

Typical Applications

- Automotive
- Industrial
- DC Motor Management for HVAC Application



NCV7719 or NCV7719A = Specific Device Code

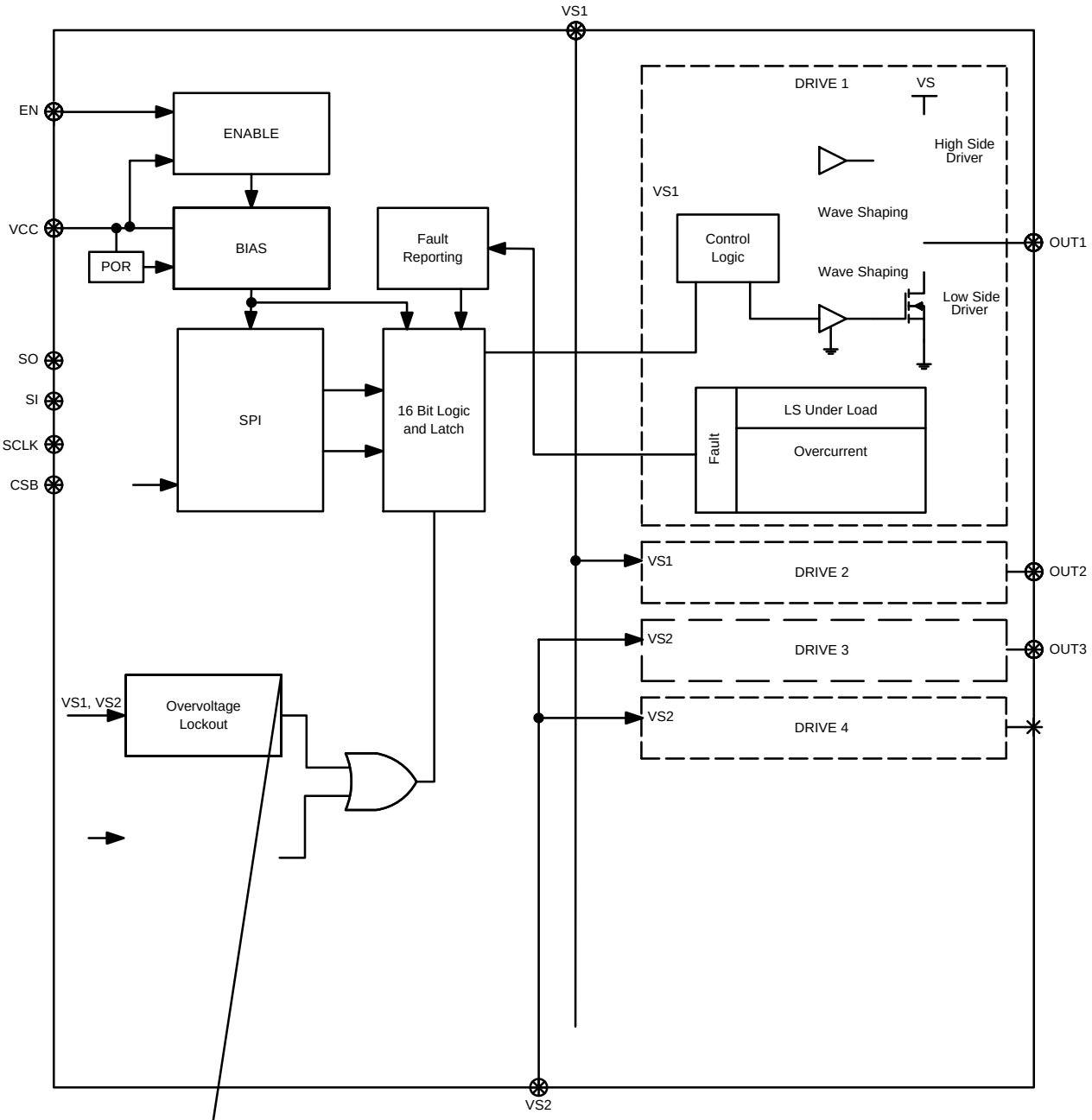


Figure 2. Block Diagram

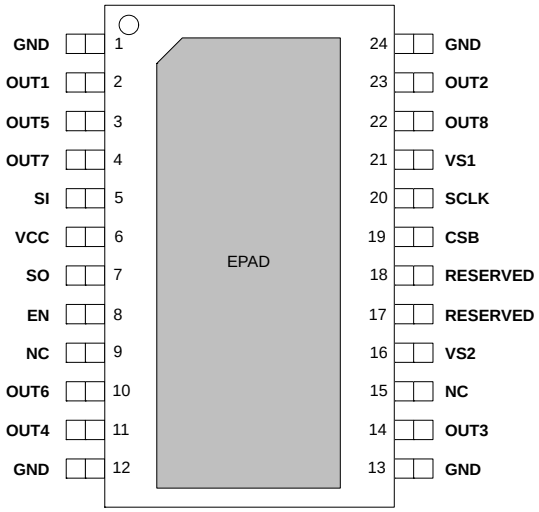


Figure 3. Pinout – SSOP24

PTION The pin−out for the Deca Half−Bridge in SSOP24 package is shown in the ta

	Description
	Ground
	Half−bridge output 1
	Half−bridge output 5
	Half−bridge output 7
	16 bit serial communication input. 3.3V/5V (TTL) Compatible − internally pulled down.

MAXIMUM RATINGS (Voltages are with respect to GND)

Rating		Symbol	Value	Unit
VSx Pin Voltage	(VS1, VS2) (DC) (AC), t < 500 ms, Ivsx > −2 A	 VSxdcMax VSxac	 −0.3 to 40 −1.0	V
I/O Pin Voltage	(Vcc, SI, SCLK, CSB, SO, EN)	VioMax	−0.3 to 5.5	V
OUTx Pin Voltage	 (DC) (AC) (AC), t< 500 ms, IOUTx > −1.1 A (AC), t< 500 ms, IOUTx < 1 A	 VoutxDc VoutxAc	 −0.3 to 40 −0.3 to 40 −1.0 1.0	V
OUTx Pin Current	(OUT1, ..., OUT8)	IoutxImax	−2.0 to 2.0	A
Junction Temperature Range		T_J	−40 to 150	°C
Storage Temperature Range		Tstr	−55 to 150	°C
Peak Reflow Soldering Temperature: Pb−free 60 to 150 seconds at 217°C		(Note 1)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality

ELECTRICAL CHARACTERISTICS

(−40°C ≤ T_J ≤ 150°C, 5.5 V ≤ VSx ≤ 40 V, 3.15 V ≤ V_{CC} ≤ 5.25 V, EN = V_{CC}, unless otherwise specified.)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
POWER SUPPLIES						
Supply Current (VS1 + VS2) Sleep Mode	IqVSx85	VS1 = VS2 = 13.2V, V_{CC} = 0 V −40°C to 85°C	−	1.0	2.5	□A
Supply Current (VS1 + VS2) Active Mode	IvsOp	EN = V_{CC}, 5.5V < VSx < 28 V No Load	−	2.5	5.0	mA
Supply Current (Vcc) Sleep Mode Active Mode	 IqV_{CC} $IV_{CC}Op$	CSB = V_{CC}, EN = SI = SCLK = 0 V −40°C to 85°C EN = CSB = V_{CC}, SI = SCLK = 0V No Load	 − −	 1.0 1.5	 2.5 3.0	 □A mA
Total Sleep Mode Current I(VS1) + I(VS2) + I(VCC)	IqTot	Sleep Mode, −40°C to 85°C VS1 = VS2 = 13.2 V, No Load	−	2.0	5.0	□A
VCC Power−on Reset Threshold	V_{CC}por	V_{CC} increasing	−	2.55	2.90	V
VSx Undervoltage Detection Threshold	VSxuv	VSx decreasing	3.5	4.1	4.5	V
VSx Undervoltage Detection Hysteresis	VSxuHys		100	−	450	mV
VSx Overvoltage Detection Threshold	VsXov	VSx increasing	30	36	40	V
VSx Overvoltage Detection Hysteresis	VSxoHys		1	2.5	4	V
DRIVER OUTPUT CHARACTERISTICS						
Output High $R_{DS(on)}$ (source)	R_{DSon}HS	Iout = −500 mA, Vs = 13.2 V V_{CC} = 3.15 V	−	1.0	2.25	□
Output Low $R_{DS(on)}$ (sink)	R_{DSon}LS	Iout = 500 mA, Vs =13.2 V V_{CC} = 3.15 V	−	1.0	2.25	□
Output Path $R_{DS(HSx+LSx)}$	RDSonPath	I_{out} = |500| mA, T_J ≤ 125°C	−	−	4.0	□
Source Leakage Current IsrcLkg13.2 IsrcLkg28	 	V_{CC} = 5 V, OUT(1−8) = 0 V, −40°C to 85°C; V_{Sx} = 13.2 V V_{Sx} = 28 V	 −1.0 −2.0	 − −	 − −	□A
Sink Leakage Current IsnkLkg13.2 IsnkLkg28	 	V_{CC} = 5 V; OUT(1−8) = V_{Sx} = 13.2 V OUT(1−8) = V_{Sx} = 28 V	 − −	 − −	 1.0 2.0	□A
Overcurrent Shutdown Threshold (Source)	IsdSrc	V_{CC} = 5 V, VSx = 13.2 V	−2.0	−1.2	−0.8	A
Overcurrent Shutdown Threshold (Sink)	IsdSnk	V_{CC} = 5 V, VSx = 13.2 V	0.8	1.2	2.0	A
Over Current Delay Timer	TdOc		10	25	50	□s
Underload Detection Threshold (Low Side)	IuldLS	V_{CC} = 5 V, VSx = 13.2 V	2.0	11	20	mA
Underload Detection Delay Time	TdUld	V_{CC} = 5 V, VSx = 13.2 V	200	350	600	□s
Body Diode Forward Voltage	IbdFwd	If = 500 mA	−	0.9	1.3	V
DRIVER OUTPUT SWITCHING CHARACTERISTICS						
High Side Turn On Time	ThsOn	Vs = 13.2 V, R_{load} = 39 □	−	7.5	13	□s
High Side Turn Off Time	ThsOff	Vs = 13.2 V, R_{load} = 39 □	−	3.0	6.0	□s
Low Side Turn On Time	TlsOn	Vs = 13.2 V, R_{load} = 39 □	−	6.5	13	□s
Low Side Turn Off Time	TlsOff	Vs = 13.2 V, R_{load} = 39 □	−	2.0	5.0	□s

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product

ELECTRICAL CHARACTERISTICS

(−40°C ≤ T_J ≤ 150°C, 5.5 V ≤ VSx ≤ 40 V, 3.15 V ≤ V_{CC} ≤ 5.25 V, EN = V_{CC}, unless otherwise specified.)

SERIAL PERIPHERAL INTERFACE

Characteristic	Symbol	Conditions	Timing Charts #	Min	Typ	Max	Unit
CSB Setup Time	TcsbSup		5, 6	100	−	−	ns
CSB High Time	TcsbH	(Note 5)	7	5.0	−	−	□s
SO enable after CSB falling edge	TenSo		8	−	−	200	ns
SO disable after CSB rising edge	TdisSo		9	−	−		

CHARACTERISTIC TIMING DIAGRAMS

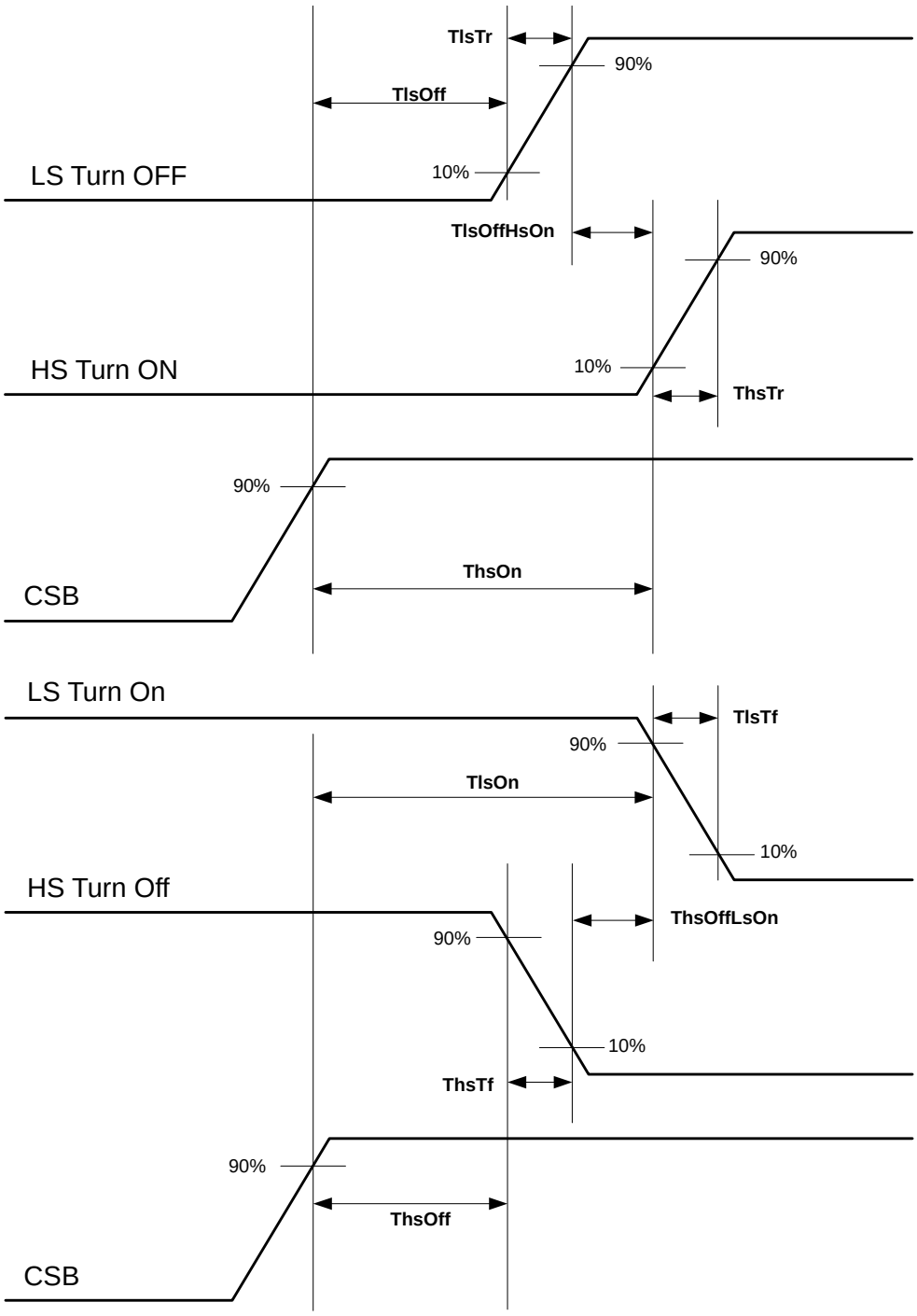
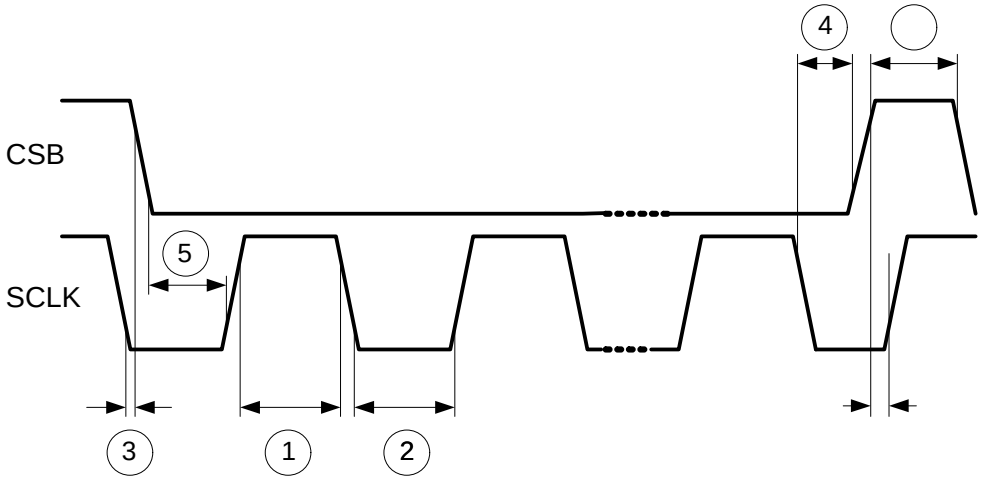
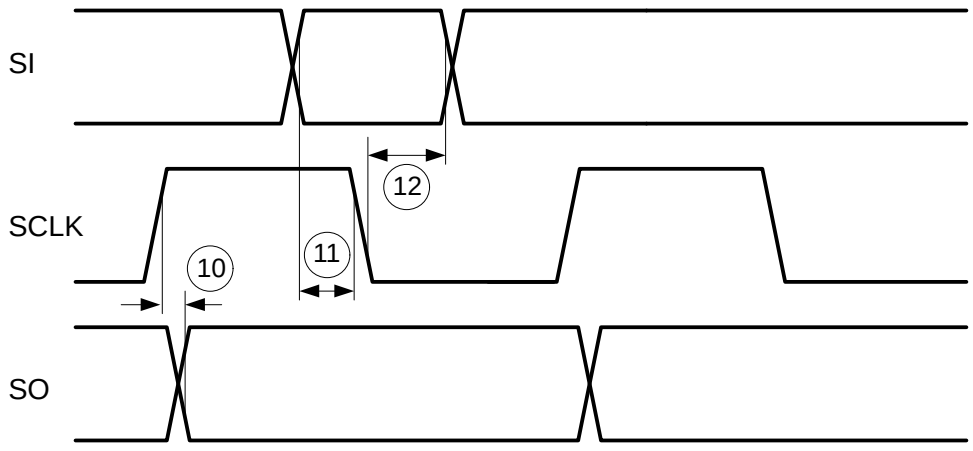


Figure 4. Detailed Driver Timing


CSB
SCLK
4
5
3
1
2


SI
SCLK
SO
12
11
10

TYPICAL PERFORMANCE CURVES

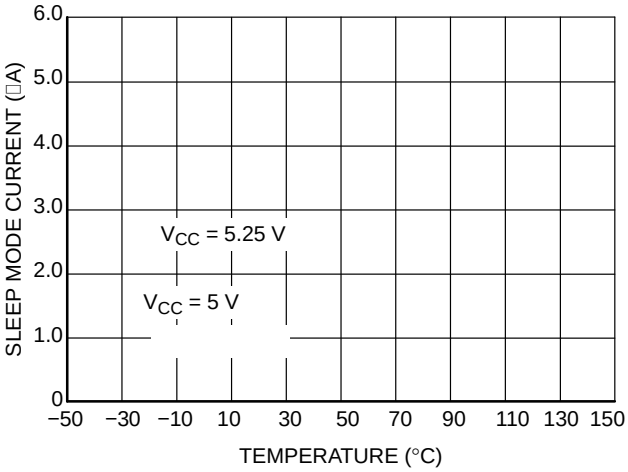


Figure 6. IqTot vs. Temperature

Table 1. SPI COMMAND INPUT DEFINITIONS

Channels 8 – 7 (Input Bit # 14 = 1)				
Bit#	**Name**	**Function**	**Status***	**Scope**
15	SRR	Status Register Reset**	1 = Reset	Status Reset per **HBSEL**
14	**HBSEL**	Channel Group Select	**1 = HB [8:7]**	1 = HB [8:7] | 0 = HB [6:1]
13	ULDSC	Underload Shutdown	1 = Enabled	Enabled per **HBSEL**; Per Half−Bridge Operation
12	X	Not Used	–	–
11				
10				
9				
8	HBEN8	Enable Half−Bridge 8	0 = Hi−Z 1 = Enabled	Per Half−Bridge
7	HBEN7	Enable Half−Bridge 7		
6	X	Not Used	–	–
5				
4				
3				
2	HBCNF8	Configure Half−Bridge 8	0 = LS On, HS Off 1 = LS Off, HS On	Per Half−Bridge
1	HBCNF7	Configure Half−Bridge 7		
0	OVLO	VSx Overvoltage Lockout	1 = Enabled	Global Lockout
Channels 6 – 1 (Input Bit # 14 = 0)				
Bit#	**Name**	**Function**	**Status***	**Scope**
15	SRR	Status Register Reset**	1 = Reset	Status Reset per **HBSEL**
14	**HBSEL**	Channel Group Select	**0 = HB [6:1]**	1 = HB [8:7] | 0 = HB [6:1]
13	ULDSC	Underload Shutdown	1 = Enabled	Enabled per **HBSEL**; Per Half−Bridge Operation
12	HBEN6	Enable Half−Bridge 6	0 = Hi−Z 1 = Enabled	Per Half−Bridge
11	HBEN5	Enable Half−Bridge 5		
10	HBEN4	Enable Half−Bridge 4		
9	HBEN3	Enable Half−Bridge 3		
8	HBEN2	Enable Half−Bridge 2		
7	HBEN1	Enable Half−Bridge 1		
6	HBCNF6	Configure Half−Bridge 6	0 = LS On, HS Off 1 = LS Off, HS On	Per Half−Bridge
5	HBCNF5	Configure Half−Bridge 5		
4	HBCNF4	Configure Half−Bridge 4		
3	HBCNF3	Configure Half−Bridge 3		
2	HBCNF2	Configure Half−Bridge 2		
1	HBCNF1	Configure Half−Bridge 1		
0	OVLO	VSx Overvoltage Lockout	1 = Enabled	Global Lockout

*All command input bits are set to 0 at V_{CC} power−on reset.
**Latched faults are cleared and outputs can be re−programmed if no fault exists after SRR asserted.

Table 2. SPI STATUS OUTPUT DEFINITIONS

Channels 8 – 7 (Input Bit # 14 = 1)				
Bit#	**Name**	**Function**	**Status***	**Scope**
PRE_15	TSD	Latched Thermal Shutdown	1 = Fault	Global Notification; Per Half−Bridge Operation
15	OCS	Latched Overcurrent Shutdown	1 = Fault	Notification per **HBSEL**; Per Half−Bridge Operation
14	PSF	VS1 and/or VS2 Undervoltage or Overvoltage	1 = Fault	Global Notification and Global Operation
13	ULD	Underload Detect	1 = Fault	Notification per **HBSEL**; Per Half−Bridge Operation
12	X	Not Used	(Hard coded to zero)	−
11				
10				
9				
8	HBST8	Half−Bridge 8 Output Status	0 = Hi−Z 1 = Enabled	Per Half−Bridge
7	HBST7	Half−Bridge 7 Output Status		
6	X	Not Used	(Hard coded to zero)	−
5				
4				
3				
2	HBCR8	Half−Bridge 8 Config Status	0 = LS On, HS Off 1 = LS Off, HS On**	Per Half−Bridge
1	HBCR7	Half−Bridge 7 Config Status		
0	TW	Thermal Warning	1 = Fault	Global Notification; Per Half−Bridge Operation

*All status output bits are set to 0 at Vcc power−on reset (POR).
**HBCRx is forced to 0 when HBSTx = 0 via POR, SPI, or fault.

ATUS OUTPUT DEFINITIONS

Channels 6 – 1 (If Previous Input Bit # 14 = 0)			
Name	**Function**	**Status***	**Scope**
TSD	Latched Thermal Shutdown	1 = Fault	Global Notification; Per Half−Bridge Operation

1 = Fault

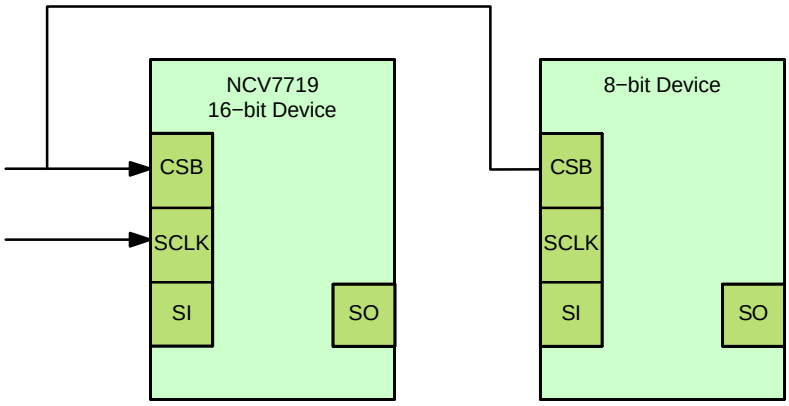


Figure 13. Daisy Chain Configuration

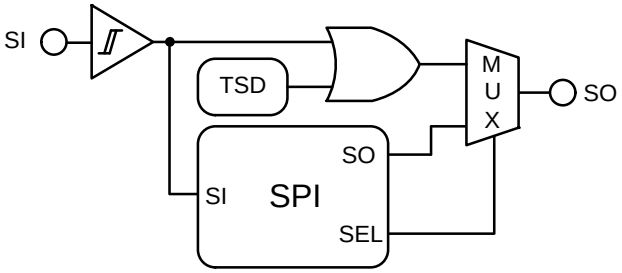


Figure 15. TSD SPI Link

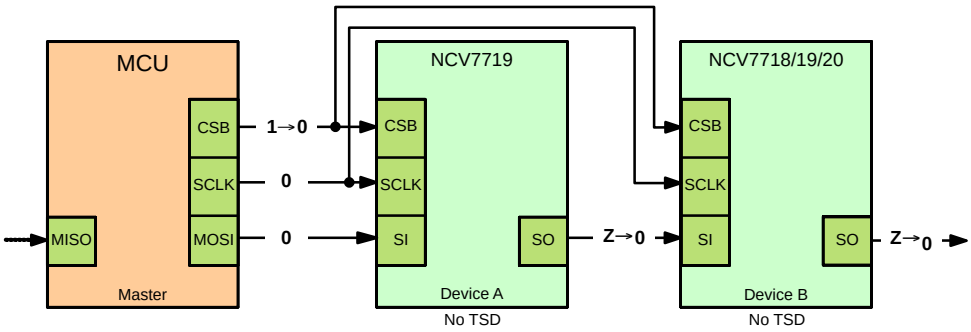
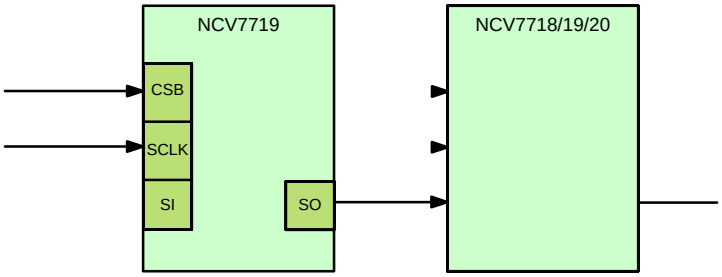


Figure 16. Daisy Chain Without TSD Fault



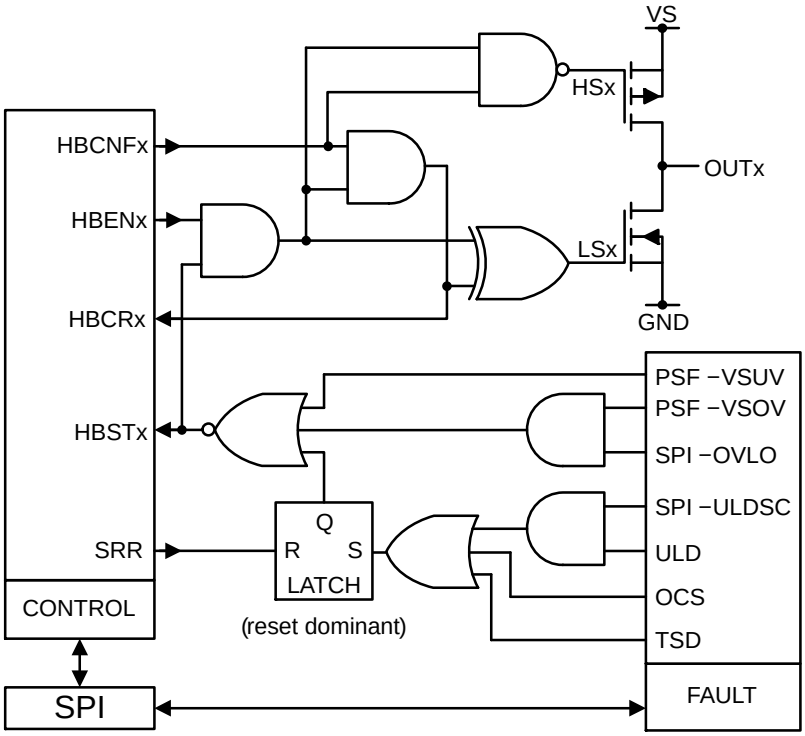


Figure 18. Simplified Half−Bridge Control Logic

Table 3. OUTPUT STATE VS. COMMAND AND STATUS

Command		Status		
HBENx	**HBCNFx**	**HBSTx**	**HBCRx**	**OUTx**
X	X	0	0	Z
0	X	0	0	Z
1	0	1	0	GND
1	1	1	1	VS

DIAGNOSTICS, PROTECTIONS, STATUS REPORTING AND RESET

Overview

The NCV7719 employs diagnostics designed to prevent destructive overstress during a fault condition. Diagnostics are classified as either supervisory or protection functions (Table 4). Supervisory functions provide status information about device conditions. Protection functions provide status information and activate fault management behaviors.

Diagnostics resulting in output shutdown and latched status may depend on a qualifier and may require user intervention for output recovery and status memory clear. Diagnostics resulting in output lockout and non−latched status (VSOV or VSUV) may recover and clear automatically. Output configurations can be changed during output lockout. Outputs assume the new configurations or resume the previous configurations when an auto−recover fault is resolved. Table 5 shows output states during faults and output recovery modes, and Table 6 shows the status memory and memory clear modes.

Table 4. Diagnostic Classes and Functions

Name	Class	Function
TSD	Protection	Thermal Shutdown
OCS	Protection	Overcurrent Shutdown
PSF	Supervisory	Under/overvoltage Lockout
ULD	Protection	Underload Shutdown
HBSTX	Supervisory	Half−Bridge X Output Status
HBCRX	Supervisory	Half−Bridge X Config Status
TW	Supervisory	Thermal Warning

Status Information Retrieval

Current status information as selected by HBSEL is retrieved during each SPI frame. To preserve device configuration and output states, the previous SI data pattern must be sent during the status retrieval frame.

Status information is prevented from being updated during a SPI frame but new status becomes available after CSB goes high at the end of the frame provided the frame did not contain an SRR request. For certain device faults, it may not be possible to determine which channel (or channels) has a particular fault (or faults) since notification may be via a single global status bit. The complete status data from all channels may need to be examined to determine where a fault may exist.

Status Register Reset − SRR

Sending SRR = 1 clears status memory and re−activates faulted outputs for channels as selected by HBSEL. The previous SI data pattern must be sent with SRR to preserve device configuration and output states. SRR takes effect at the rising edge of CSB and a timer (Tsrr) is started. Tsrr is the minimum time the user must wait between consecutive SRR requests. If a fault is still present when SRR is sent, protection can be re−engaged and shutdown can recur. The device can also be reset by toggling the EN pin or by VCC power−on reset.

Diagnostics Details

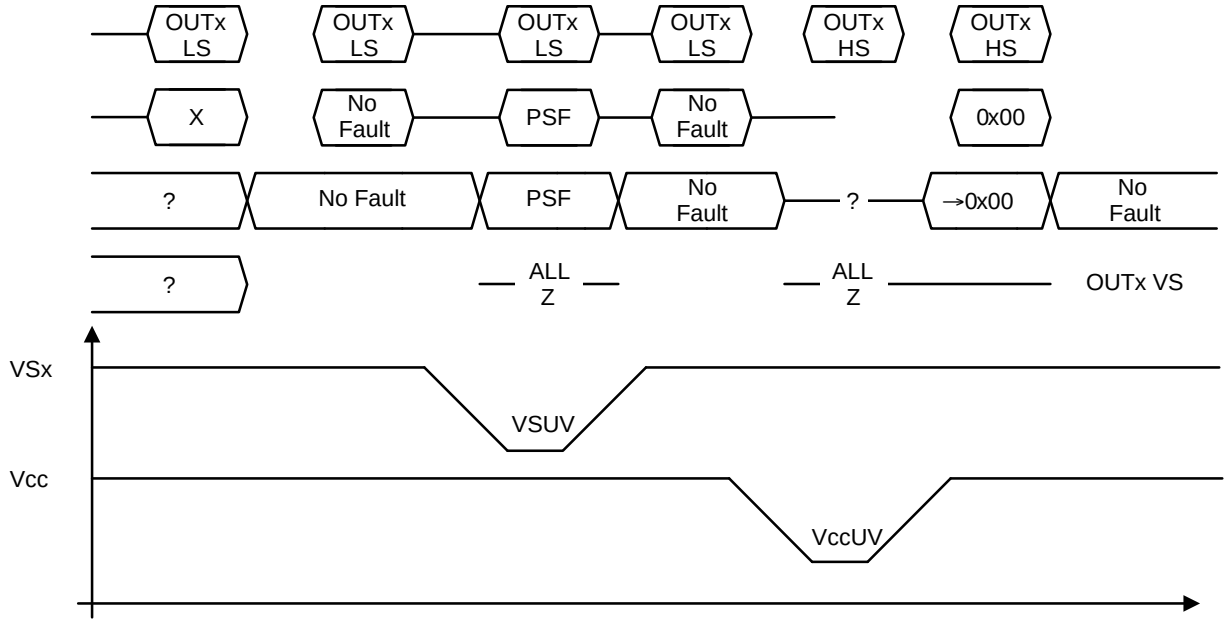
The following sections describe the individual diagnostics and some behaviors. In each description and illustration, a SPI frame is assumed to always be valid and the SI data pattern sent for HBCNFx and HBENx is the same as the previous frame. Actual results can depend on asynchronous fault events and SPI clock frequency and frame rate.

Undervoltage Lockout

Global Notification, Global Operation

Undervoltage detection and lockout control is provided by monitoring the VS1, VS2 and V_{CC} supply inputs. Undervoltage hysteresis is provided to ensure clean detection transitions. Undervoltage timing is shown in Figure 19.

Undervoltage at either VSx input turns off all outputs and sets the power supply fail (PSF) status bit. The outputs return to their previously programmed state and the PSF status bit is cleared when VSx rises above the hysteresis voltage level. SPI is available and programmed output enable and configuration states are maintained if proper V_{CC} is present during VSx undervoltage. V_{CC} undervoltage turns all outputs off and clears the command input and status output registers.



Overvoltage Lockout

Global Notification, Global Operation

Overvoltage detection and lockout control is provided by monitoring the VS1 and VS2 supply inputs. Overvoltage hysteresis is provided to ensure clean detection transitions. Overvoltage timing is shown in Figure 20.

Overvoltage at either VSx input turns off all outputs if the overvoltage lockout input bit is set (OVLO = 1, HBSEL = X), and sets the power supply fail (PSF) status bit (see Tables 5 and 6). The outputs return to their previously programmed state and the PSF status bit is cleared when VSx falls below the hysteresis voltage level.

To reduce stress, it is recommended to operate the device with OVLO bit asserted to ensure that the drivers turn off during a load dump scenario.

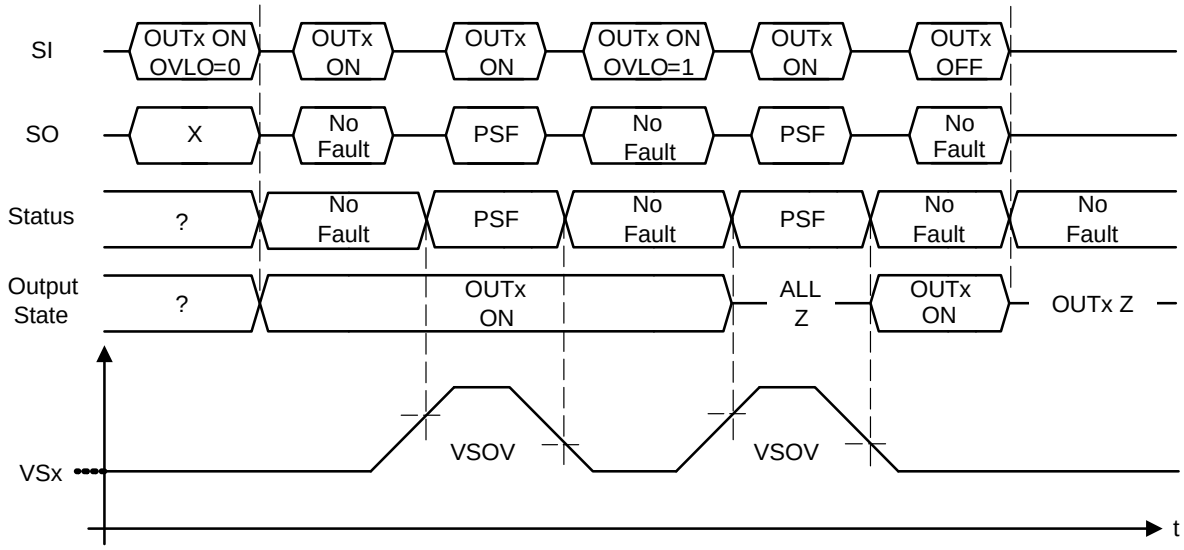


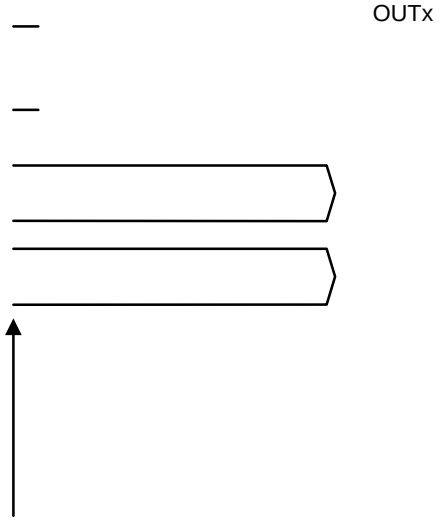
Figure 20. Overvoltage Timing

Overcurrent Shutdown

Notification per HBSEL, Per Half−Bridge Operation

Overcurrent detection and shutdown control is provided by monitoring each HS and LS driver. Overcurrent timing is shown in Figure 21. Overcurrent in either driver starts a channel's overcurrent delay timer. If overcurrent exists after the delay, both drivers are latched off and the overcurrent (OCS) status bit is set. The OCS bit is cleared and channels are re−activated by sending SRR = 1. The channel group select (HBSEL) input bit determines which channels are affected by SRR.

A persistent overcurrent cause should be resolved prior to re−activation to avoid repetitive stress on the drivers. Extended exposure to stress may affect device reliability.



Underload Shutdown

Notification per HBSEL, Shutdown per HBSEL

Underload detection and shutdown control is provided by monitoring each LS driver. Underload timing is shown in Figure 22. Underload at a LS driver starts the global underload delay timer. If underload occurs in another channel after the global timer has been started, the delay for any subsequent underload will be the remainder of the timer. The timer runs continuously with a persistent underload condition.

If underload exists after the delay and if the underload shutdown (ULDSC) command bit is set, both HS and LS drivers are latched off and the underload (ULD) status bit is set; otherwise the drivers remain on and the ULD bit is set (see Table 5 and 6). The ULD bit is cleared and channels are re−activated by sending SRR = 1. The channel group select (HBSEL) input bit determines which channels are affected by SRR and also determines which half−bridges are latched off via the ULDSC command bit (see Table 1).

Underload may result from a fault (e.g. open−load) condition or normal circuit behavior (e.g. L/R tau). In motor applications it is often desirable to actively brake the motor by turning on both HS or LS drivers in two half−bridge channels. If the configuration is two LS drivers (LS brake), an underload will result as the motor current decays normally. Utilizing HS brake instead will avoid underload notification.

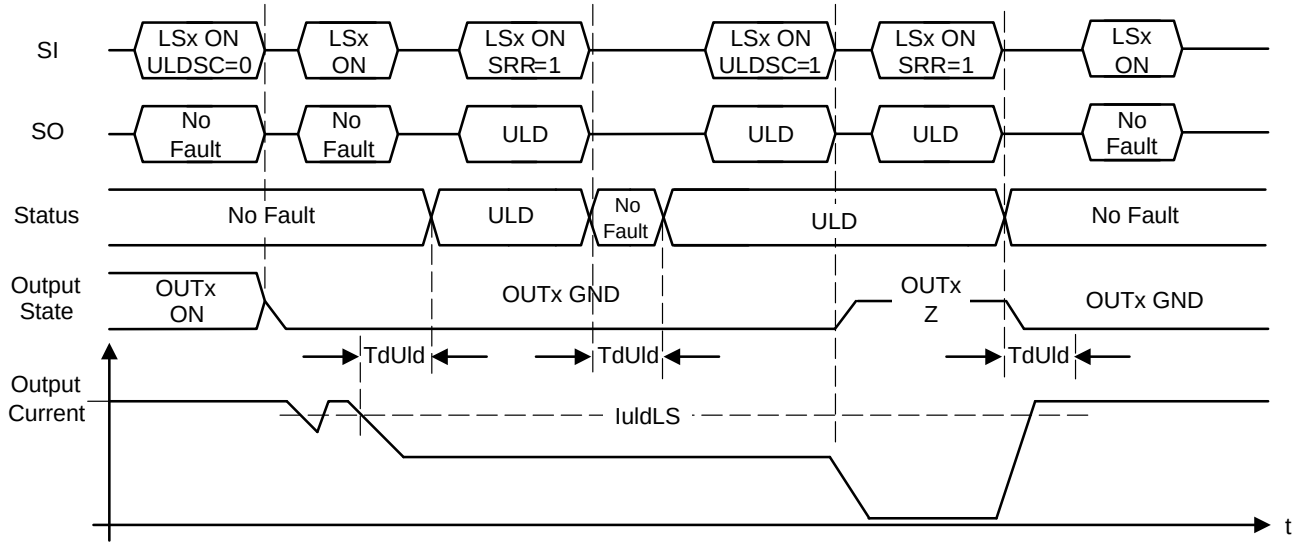


Figure 22. Underload Timing

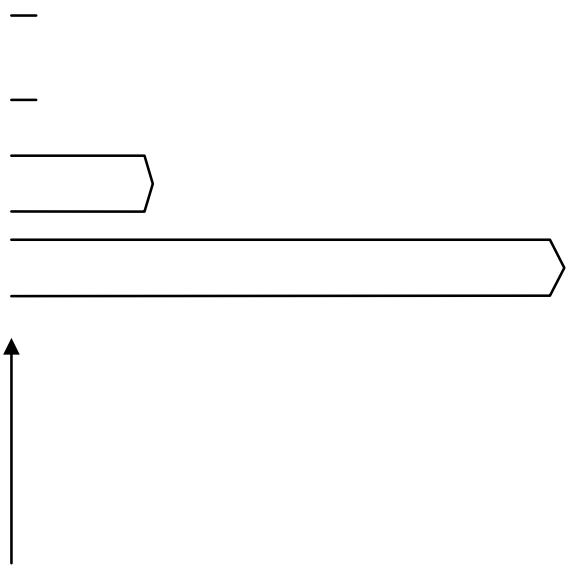
Thermal Warning and Thermal Shutdown

Global Notification, Per Half−Bridge Operation

Thermal warning (TW) and thermal shutdown (TSD) detection and control are provided for each half−bridge by monitoring the driver pair's thermal sensor. Thermal hysteresis is provided for each of the warning and shutdown functions to ensure clean detection transitions. Since TW notification precedes TSD, software polling of the TW bit enables avoidance of thermal shutdown. Thermal warning and shutdown timing is shown in Figure 23.

The TW status bit is set when a half−bridge's sensor temperature exceeds the warning level (T_J > Twr), and the bit is automatically cleared when sensor temperature falls below the warning hysteresis level (T_J < TwHy). A channel's output state is unaffected by TW.

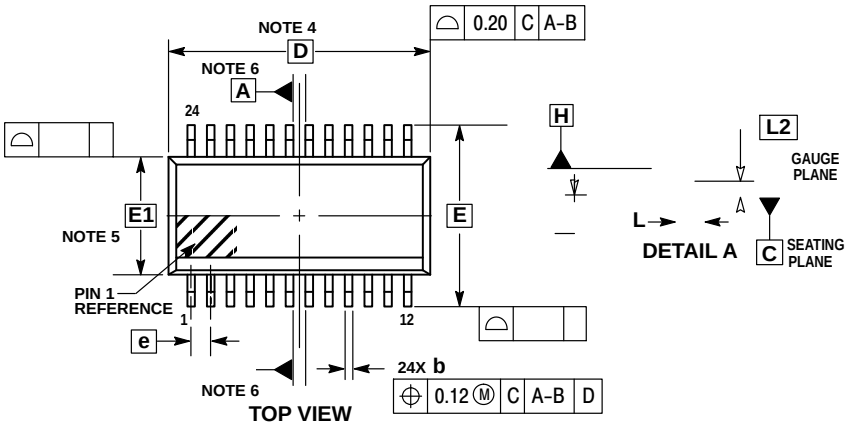
When sensor temperature exceeds the shutdown level (T_J > Tsd), the channel's HS and LS drivers are latched off, the TW bit is/remains set, and the TSD (PRE_15) bit is set. The TSD bit is cleared and all affected channels in a group are re−activated (T_J < TsdHy) by sending SRR = 1. The channel group select (HBSEL) input bit determines which channels are affected by SRR.

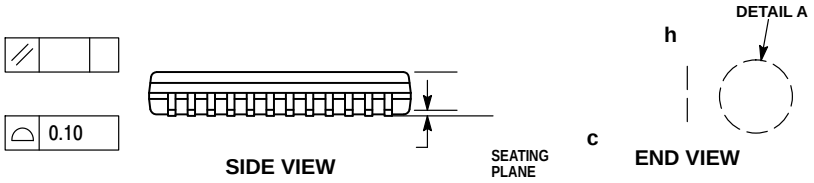


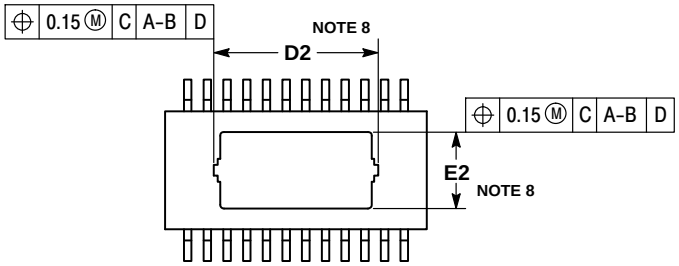
SSOP24 NB EP
CASE 940AK
ISSUE O

SCALE 1:1

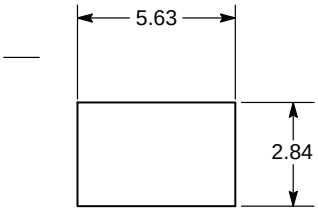
DATE 24 APR 2012







SOLDERING FOOTPRINT



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.10 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. DIMENSION b APPLIES TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D IS DETERMINED AT DATUM PLANE H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM PLANE H.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. CONTOURS OF THE THERMAL PAD ARE UNCONTROLLED WITHIN THE REGION DEFINED BY DIMENSIONS D2 AND E2.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.70
A1	0.00	0.10
b	0.19	0.30
c	0.09	0.20

D2	5.28	5.58

E1	3.90 BSC	
E2	2.44	2.64
e	0.65 BSC	
h	0.25	0.50
L	0.40	0.85
L1	1.00 REF	
L2	0.25 BSC	
M	0°	8°