# Hex Half-Bridge Driver

# NCV7723B

The NCV7723B is a six channel half−bridge driver with protection features designed specifically for automotive and industrial motion control applications. The product has independent controls and diagnostics, and the drivers can be operated in forward, reverse, brake, and high impedance states. The device is controlled via a 16 bit SPI interface and is daisy chain compatible. Outputs 1 and 2 can be controlled through an external PWM signal.

### Features

- Low Quiescent Current Sleep Mode
- High−Side and Low−Side Outputs

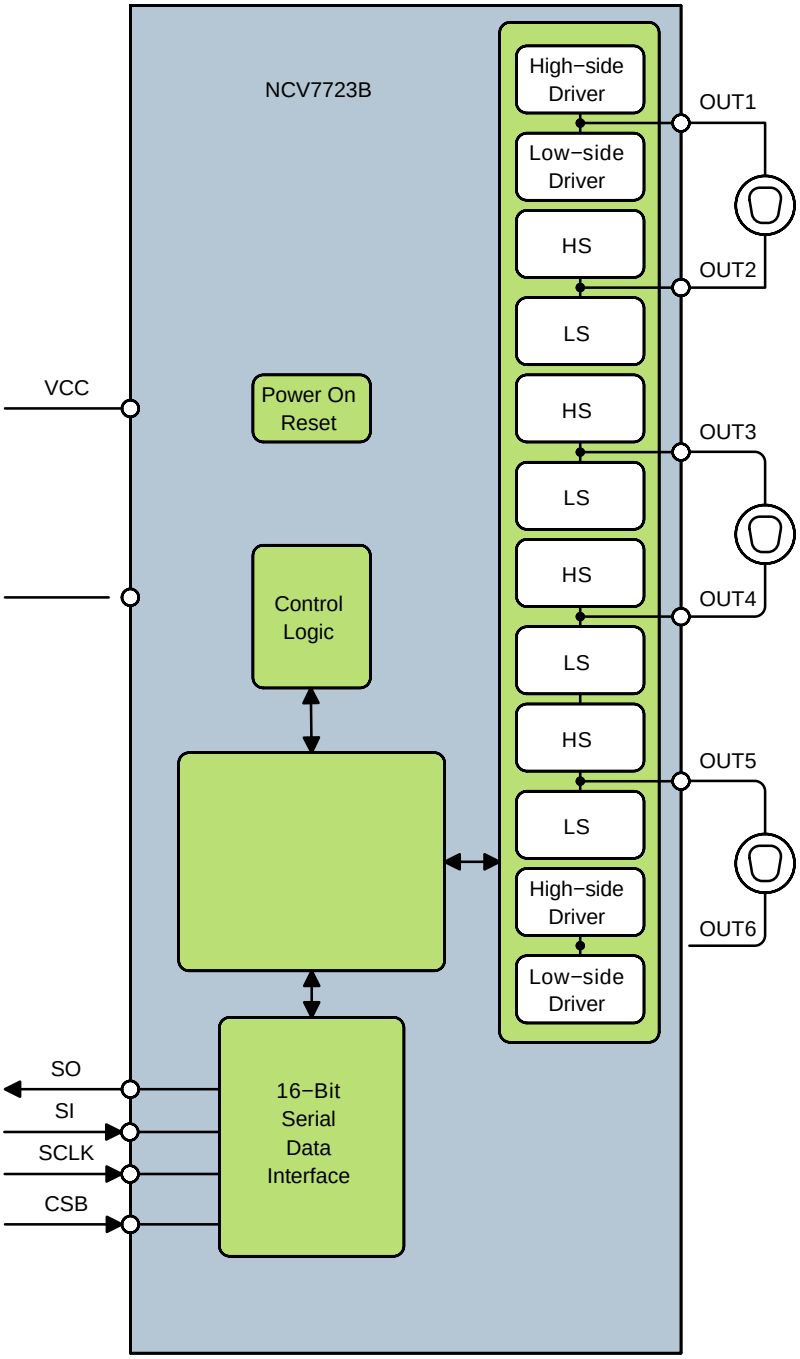
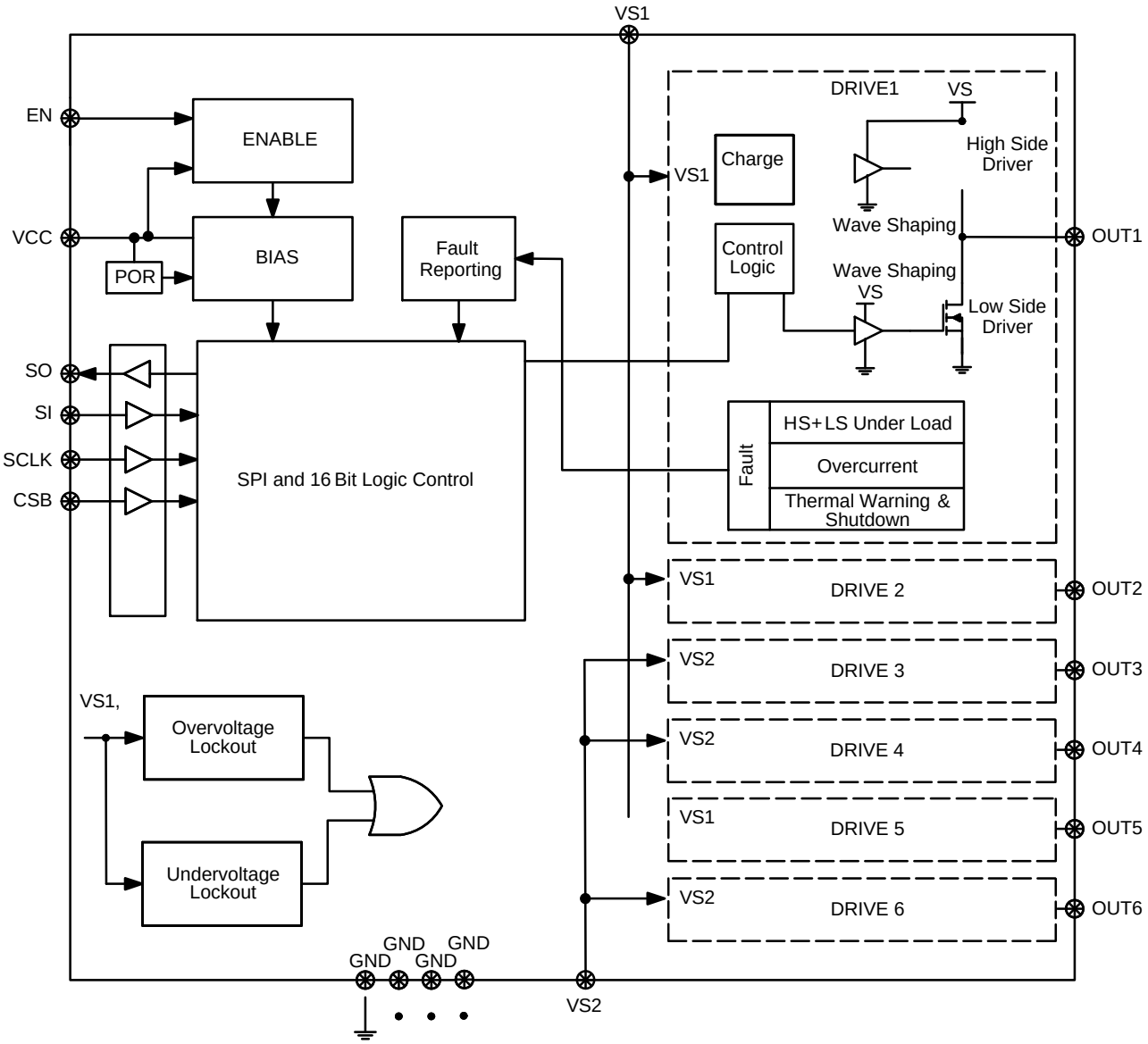



**Figure 1. Typical Application**


VS1
EN
ENABLE
VCC
BIAS
POR
Fault Reporting
SO
SI
SCLK
CSB
SPI and 16 Bit Logic Control
DRIVE1
VS
High Side Driver
VS1
Charge
Wave Shaping
OUT1
Control Logic
Wave Shaping
VS
Low Side Driver
Fault
HS+LS Under Load
Overcurrent
Thermal Warning & Shutdown
VS1
DRIVE 2
OUT2
VS2
DRIVE 3
OUT3
VS2
DRIVE 4
OUT4
VS1
DRIVE 5
OUT5
VS2
DRIVE 6
OUT6
VS1,
Overvoltage Lockout
Undervoltage Lockout
GND
GND
GND
GND
VS2

## ATTRIBUTES

| Characteristic | | Symbol | Value | Unit |
|---|---|---|---|---|
| Short Circuit Reliability Characterization | | AECQ10x | Grade A | |
| ESD Capability<br>Human Body Model per AEC−Q100−002<br><br>Charged Device Model per AEC−Q100−011 | <br>VSx, OUTx<br>All Other Pins<br> | <br>Vesd4k<br>Vesd2k<br>Vesd750 | <br>≥ ±4.0 kV<br>≥ ±2.0 kV<br>≥ ±750 V | |
| Moisture Sensitivity Level | | MSL | MSL2 | |
| Package Thermal Resistance – Still−air<br>Junction–to–Ambient<br>Junction–to–Board | <br>(Note 2)<br>(Note 2) | <br>$R_{\theta JA}$<br>$R_{\theta JBOARD}$ | <br>32.1<br>21.8 | <br>°C/W<br>°C/W |

2. Based on JESD51−7, 1.6 mm thick FR4, 2S2P PCB with 600 $mm^2$ 2 oz. copper and 18 thermal vias to 80x80 mm 1 oz. internal spreader planes. Simulated with each channel dissipating 0.2 W.

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Digital Supply Input Voltage | VCCOp | 3.15 | 5.25 | V |
| Battery Supply Input Voltage (VS1 = VS2) | VSxOp | 5.5 | 32 | V |
| DC Output Current | IxOp | − | 0.5 | A |
| Junction Temperature | TjOp | −40 | 125 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(−40°C ≤ $T_J$ ≤ 150°C, 5.5 V ≤ VSx ≤ 40 V, 3.15 V ≤ $V_{CC}$ ≤ 5.25 V, EN = $V_{CC}$, unless otherwise specified.)

| Characteristic | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **POWER SUPPLIES** | | | | | | |
| Supply Current (VS1 + VS2)<br>Sleep Mode | | | | | | |

**ELECTRICAL CHARACTERISTICS**
(−40°C ≤ $T_J$ ≤ 150°C, 5.5 V ≤ VSx ≤ 40 V, 3.15 V ≤ $V_{CC}$ ≤ 5.25 V, EN = $V_{CC}$, unless otherwise specified.) (continued)

| Characteristic | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DRIVER OUTPUT CHARACTERISTICS** | | | | | | |
| Sink Leakage Current | IsnkLkg13.2<br>IsnkLkg28 | $V_{CC}$ = 5 V, EN = 0/5 V<br>OUT (1−6) = VSx = 13.2 V<br>OUT (1−6) = VSx = 28 V | −<br>− | −<br>− | 1.0<br>2.0 | □A<br>□A |
| Overcurrent Shutdown Threshold (Source) | IsdSrc | $V_{CC}$ = 5 V, VSx = 13.2 V | −2.0 | −1.5 | −1.1 | A |
| Overcurrent Shutdown Threshold (Sink) | IsdSnk | $V_{CC}$ = 5 V, VSx = 13.2 V | 1.1 | 1.5 | 2.0 | A |

## ELECTRICAL CHARACTERISTICS

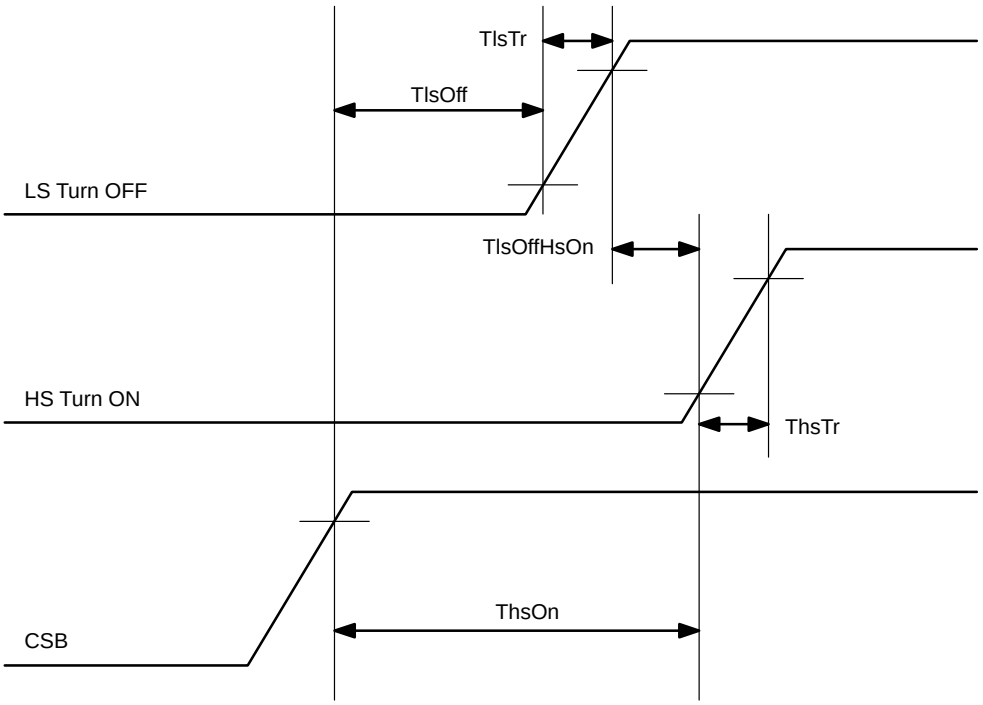
(−40°C ≤ $T_J$ ≤ 150°C, 5.5 V ≤ VSx ≤ 40 V, 3.15 V ≤ $V_{CC}$ ≤ 5.25 V, EN = $V_{CC}$, unless otherwise specified.) (continued)

| Characteristic | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **LOGIC OUTPUT SO** | | | | | | |
| Output High | VsoH | ISOURCE = −1 mA | $V_{CC}$ − 0.6 | − | − | V |
| Output Low | VsoL | ISINK = 1.6 mA | − | − | 0.4 | V |
| Tri−state Leakage | ItriStLkg | CSB = 5 V | −5 | − | 5 | □A |
| Tri−state Output Capacitance | ItriStCout | CSB = $V_{CC}$, 0 V < $V_{CC}$ < 5.25 V (Note 3) | − | − | 15 | pF |
| **SERIAL PERIPHERAL INTERFACE** | | | | | | |
| SCLK Frequency | Fclk | | − | − | − | 5.0 | MHz |
| SCLK Clock Period | TpClk | $V_{CC}$ = 5 V<br>$V_{CC}$ = 3.3 V | <br>− | 200<br>500 | −<br>− | −<br>− | ns |
| SCLK High Time | TclkH | | 1 | 85 | − | − | ns |
| SCLK Low Time | TclkL | | 2 | 85 | − | − | ns |
| SCLK Setup Time | TclkSup | | 3, 4 | 85 | − | − | ns |
| SI Setup Time | TsiSup | | 11 | 50 | − | − | ns |
| SI Hold Time | TsiH | | 12 | 50 | − | − | ns |
| CSB Setup Time | TcsbSup | | 5, 6 | 100 | − | − | ns |
| CSB High Time | TcsbH | (Note 4) | 7 | 5.0 | − | − | □s |
| SO enable after CSB falling edge | TenSo | | 8 | – | − | 200 | ns |
| SO disable after CSB rising edge | TdisSo | | 9 | – | − | 200 | ns |
| SO Rise/Fall Time | TsoR/F | Cload = 40 pF (Note 3) | − | − | 10 | 25 | ns |
| SO Valid Time | TsoV | Cload = 40 pF (Note 3)<br>SCLK ↑ to SO 50% | 10 | – | 50 | 100 | ns |
| EN Low Valid Time | TenL | $V_{CC}$ = 5 V; EN H → L 50% to OUTx turning off 50% | − | 10 | − | − | □s |
| EN High to SPI Valid | TenHspiV | | − | – | − | 100 | □s |
| SRR Delay Between Consecutive Frames | Tsrr | (Note 5) | − | 150 | − | − | □s |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Not production tested.
4. This is the minimum time the user must wait between SPI commands.
5. This is the minimum time the user must wait between consecutive SRR requests.

## CHARACTERISTIC TIMING DIAGRAMS



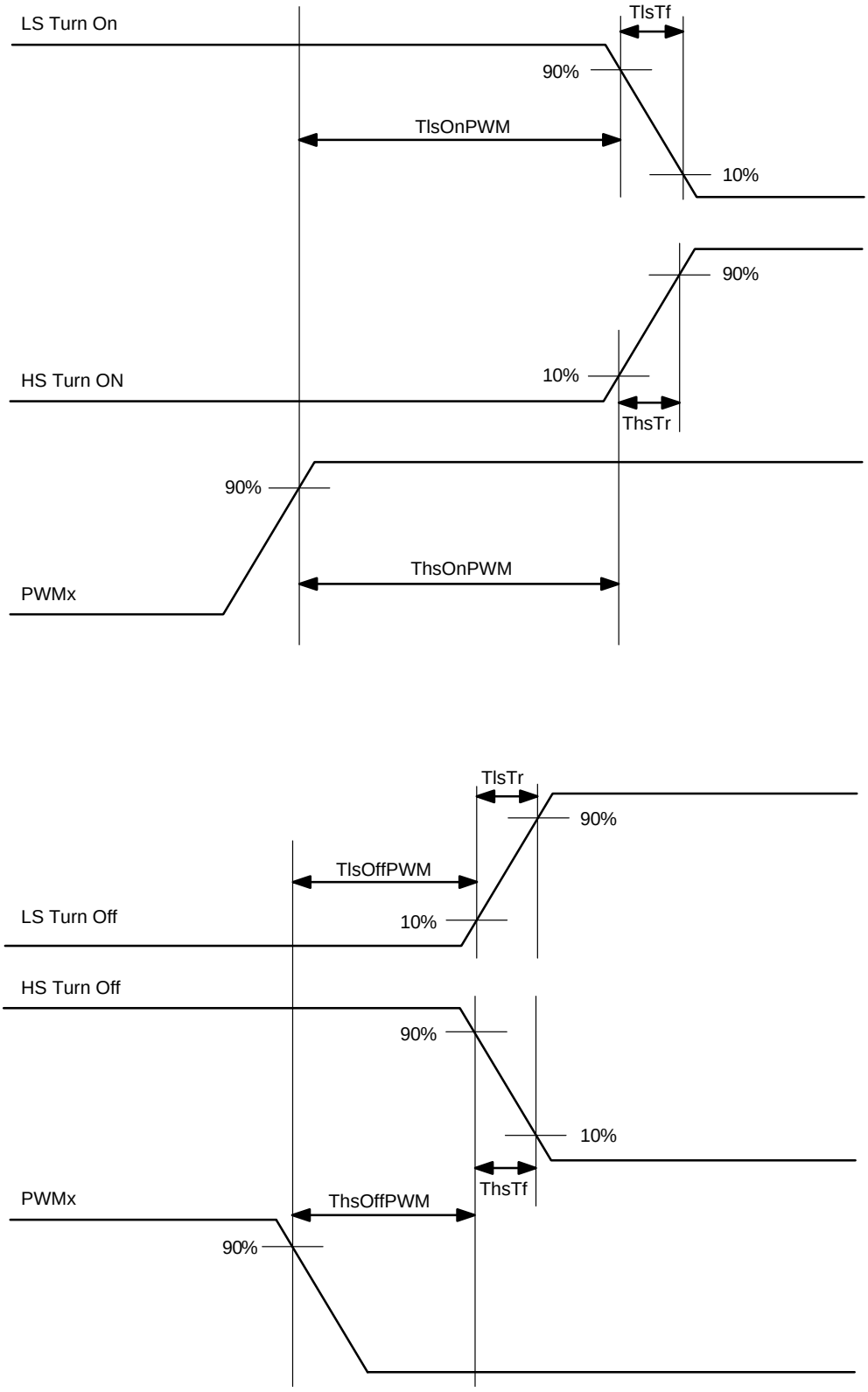
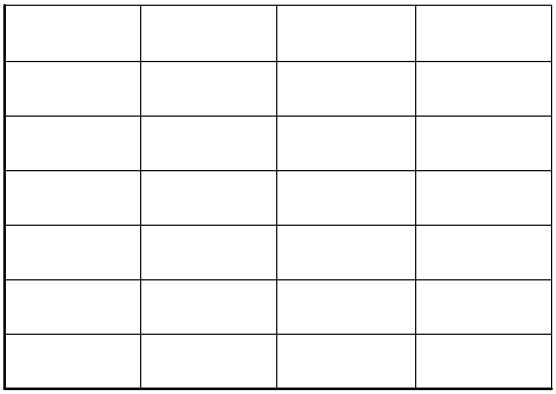



**Figure 5. Detailed Driver Timing (OUT1 / OUT2 PWM)**

## TYPICAL PERFORMANCE GRAPHS



TEMPERATURE (°

**Figure 7. IqTot vs. Temperature**

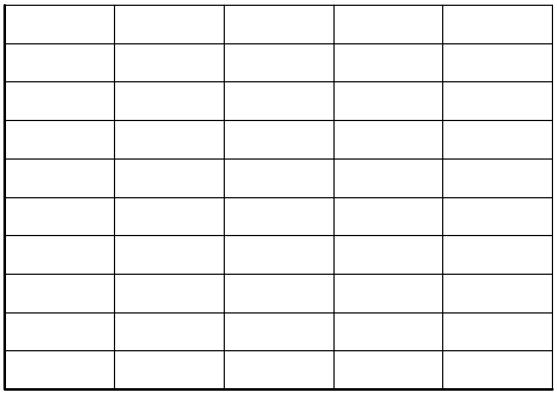


**Figure 8. I($V_{CC}$) Active Mode vs. V($V_{CC}$)**

## DETAILED OPERATING DESCRIPTION

### General Overview

The NCV7723B is comprised of twelve NMOS power drivers. The drivers are arranged as six half−bridge output channels, allowing for three independent full−bridge configured loads. Output control and status reporting is handled via the SPI (Serial Peripheral Interface) communications port. OUT1 and OUT2 can be controlled with an external PWM signal.

Each output is characterized for a typical 0.5 A DC load and has a maximum 2.0 A surge capability (at VSx = 13.2 V). Maximum allowable junction temperature is 150°C and may constrain the maximum load current and/or limit the number of drivers active at once.

An active−high enable function (EN) allows global control of the outputs and provides a low quiescent current sleep mode when the device is not being utilized. An internal pull−down resistor is provided on the input to ensure the device enters sleep mode if the input signal is lost.

After EN transitions from low to high, the $V_{CC}$ POR cycle will proceed and bring the device into normal operation. The device configuration registers can then be programmed via SPI. Bringing EN low clears all registers (no configuration

**Table 1. SPI COMMAND INPUT DEFINITIONS**

| Channels 6 – 1 | | | | |
|---|---|---|---|---|
| **Bit#** | **Name** | **Function** | **Status*** | **Scope** |
| 15 | SRR | Status Register Reset** | 1 = Reset | Global Status Reset |
| 14 | HBSEL*** | Half Bridge Selection | Reserved | – |
| 13 | ULDSC | Underload Shutdown Control | 1 = Enabled | Per Half−Bridge Operation |
| 12 | HBEN6 | Enable Half−Bridge 6 | 0 = Hi−Z<br>1 = Enabled | Per Half−Bridge |
| 11 | HBEN5 | Enable Half−Bridge 5 | | |
| 10 | HBEN4 | Enable Half−Bridge 4 | | |
| 9 | HBEN3 | Enable Half−Bridge 3 | | |
| 8 | HBEN2 | Enable Half−Bridge 2 | | |
| 7 | HBEN1 | Enable Half−Bridge 1 | | |
| 6 | HBCNF6 | Configure Half−Bridge 6 | 0 = LS On, HS Off<br>1 = LS Off, HS On | Per Half−Bridge |
| 5 | HBCNF5 | Configure Half−Bridge 5 | | |
| 4 | HBCNF4 | Configure Half−Bridge 4 | | |
| 3 | HBCNF3 | Configure Half−Bridge 3 | | |
| 2 | HBCNF2 | Configure Half−Bridge 2 | | |
| 1 | HBCNF1 | Configure Half−Bridge 1 | | |

**Table 2. SPI STATUS OUTPUT DEFINITIONS**

| Channels 6 – 1 | | | | |
|---|---|---|---|---|
| **Bit#** | **Name** | **Function** | **Status*** | **Scope** |
| PRE_15 | TSD | Latched Thermal Shutdown | 1 = Fault | Global Notification; Per Half−Bridge Operation |
| 15 | OCS | Latched Overcurrent Shutdown | 1 = Fault | Global Notification; Per Half−Bridge Operation |
| 14 | PSF | VS1 and/or VS2 Undervoltage or Overvoltage | 1 = Fault | Global Notification; Global Operation |
| 13 | | | | |

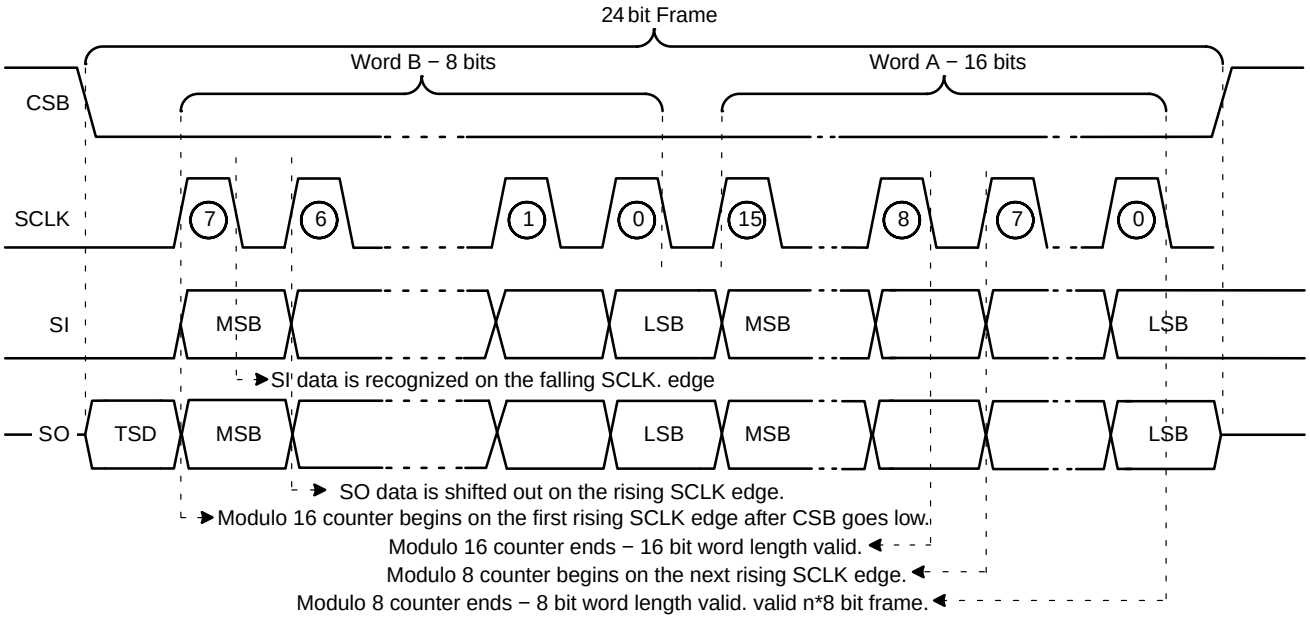



**Figure 16. Daisy Chain – 24 bit Frame Format**

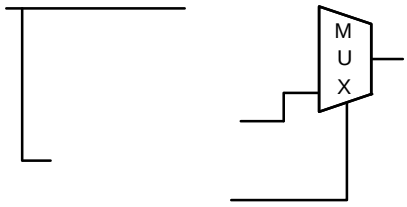
**TSD Bit in Daisy Chain Operation**

The SO frame is designed to allow TSD status retrieval in a daisy chain configuration using NCV7723B or other devices with identical SPI functionality. The TSD status bit is OR'd with SI and then multiplexed with the device's usual status data (Figure 17).

CSB is held high and SI and SCLK are held low by the master before the start of the SPI frame. TSD status is immediately available as bit PRE_15 at SO (SO = TSD) when CSB goes low to begin the frame. The usual status data (SO = STA) becomes available after the first rising SCLK edge.

The TSD status automatically propagates through the chain from the SO output of the previous device to the SI input of the next. This is shown in Figures 18 and 19, first without a TSD fault in either device (Figure 18), and then subsequently with a latched TSD fault (TSD = 1) in device "A" propagating through to device "B" (Figure 19).

Since the TSD status of any device propagates automatically through the entire chain, it is not possible to determine which device (or devices) has a fault (TSD = 1). The usual status data from each device will need to be examined to determine where a fault (or faults) may exist.



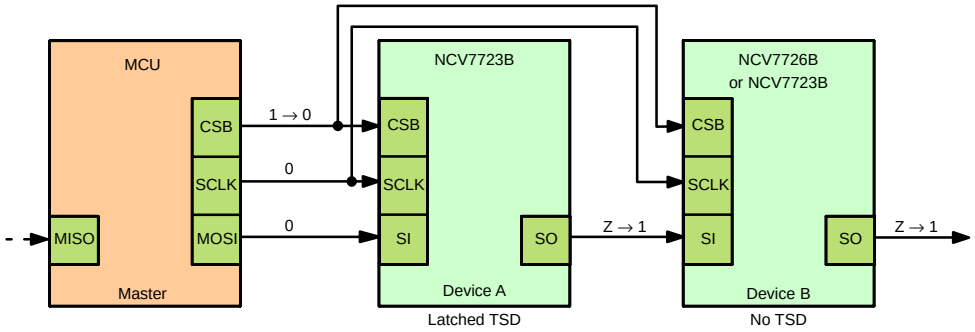



**Figure 19. Daisy Chain With TSD Fault**

### Power Up/Down Control

The $V_{CC}$ supply input powers the device's logic core. A $V_{CC}$ power−on reset (POR) function provides controlled power−up/down. $V_{CC}$ POR initializes the command input and status output registers to their default states (0x00), and ensures that the bridge output and SO drivers maintain Hi−Z as power is applied. SPI communication and normal device operation can proceed once $V_{CC}$ rises above the POR threshold and EN remains high.

The VS1 and VS2 supply inputs power their respective output drivers (refer to Figure 2 and the PIN FUNCTION DESCRIPTION). The VSx inputs are monitored to ensure that the supply stays within the recommended operating range. If the VSx supply moves into either of the VS undervoltage or overvoltage regions, the output drivers are switched to Hi−Z but command and status data is preserved. Output drivers will remain on if OVLO = 0 during an overvoltage condition.

### Driver Control

The NCV7723B has the flexibility to control each half−bridge driver channel via SPI. Actual driver output state is determined by the command input and the current fault status bits.

High−side (HSx) and low−side (LSx) drivers of the same channel cannot be active at the same time, and non−overlap delays are imposed when switching between HSx and LSx drivers in the same channel, preventing current shoot−through.

After the device has powered up and the drivers are allowed to turn on, the drivers remain on until commanded off via SPI or until a fault condition occurs.

### PWM Control

Outputs 1 and 2 can be controlled in two ways: through normal SPI control (see Table 1) or from an external PWM

## DIAGNOSTICS, PROTECTIONS, STATUS REPORTING AND RESET

### Overview

The NCV7723B employs diagnostics designed to prevent destructive overstress during a fault condition. Diagnostics are classified as either supervisory or protection functions (Table 3). Supervisory functions provide status information about device conditions. Protection functions provide status information and activate fault management behaviors. Diagnostics resulting in output shutdown and latched status may depend on a qualifier and may require user intervention for output recovery and status memory clear. Diagnostics resulting in output lockout and non−latched status (VSOV or VSUV) may recover and clear automatically. Output configurations can be changed during output lockout. Outputs assume the new configurations or resume the previous configurations when an auto−recover fault is resolved. Table 4 shows output states during faults and output recovery modes, and Table 5 shows the status memory and memory clear modes.

**Table 3. DIAGNOSTIC CLASSES AND FUNCTIONS**

| Name | Class | Function |
|---|---|---|
| TSD | Protection | Thermal Shutdown |
| OCS | Protection | Overcurrent Shutdown |
| PSF | Protection | Under/overvoltage Lockout (OVLO = 1) |
| ULD | Protection | Underload Shutdown |
| HBSTx[1:0] | Supervisory | Half−Bridge X Output Status |
| TW | Supervisory | Thermal Warning |

**Table 4. OUTPUT STATE VS. FAULT AND OUTPUT RECOVERY**

| Fault | Qualifier | OUTx State | OUTx Recovery | OUTx Recovery Scope |
|---|---|---|---|---|
| TSD | − | → Z | Send SRR | All Outputs |
| OCS | − | → Z | Send SRR | All Outputs |
| PSF – VSOV | OVLO = 1 | → Z → $Y_n$ \| $Y_{n+1}$ | Auto* | All Outputs |
| | OVLO = 0 | Unaffected | − | − |
| PSF – VSUV | − | → Z → $Y_n$ \| $Y_{n+1}$ | Auto* | All Outputs |
| ULD | ULDSC = 1 | → Z | Send SRR | All Outputs |
| | ULDSC = 0 | Unaffected | − | − |
| TW | − | Unaffected | − | − |

*OUTx returns to its previous state ($Y_n$) or new state (Yn+1) if fault is removed.

**Table 5. STATUS MEMORY VS. FAULT AND MEMORY CLEAR**

| Fault | Qualifier | Status Memory | Memory Clear | Memory Clear Scope |
|---|---|---|---|---|
| TSD | − | Latched | Send SRR | Global |
| OCS | − | Latched | Send SRR | Global |
| PSF – VSOV | OVLO = X | Non−Latched | Auto* | Global |
| PSF – VSUV | – | Non−Latched | Auto* | Global |
| ULD | ULDSC = X | Latched | Send SRR | Global |
| TW | − | Non−Latched | Auto* | Global |

*Status memory returns to its no−fault state if fault is removed.

### Status Information Retrieval

Current status information is retrieved during each SPI frame. To preserve device configuration and output states, the previous SI data pattern must be sent during the status retrieval frame.

Status information is prevented from being updated during a SPI frame but new status becomes available after CSB goes high at the end of the frame provided the frame did not contain an SRR request. Status information includes both global and per channel fault notification. To determine the channel(s) affected after detecting a global fault, examine driver output status and input configuration.

### Status Register Reset SRR

Sending SRR = 1 clears status memory and re−activates faulted outputs for all channels. The previous SI data pattern must be sent with SRR to preserve device configuration and output states.

At the rising edge of CSB, the SRR function is activated and an internal timer (Tsrr) is started. Tsrr is the minimum time the user must wait between consecutive SRR requests. If a fault is still present when SRR is sent, protection will be re−engaged and shutdown will recur. The status registers can also be reset by toggling the EN pin or by VCC power−on reset.

**Diagnostics Details**

The following sections describe individual diagnostics

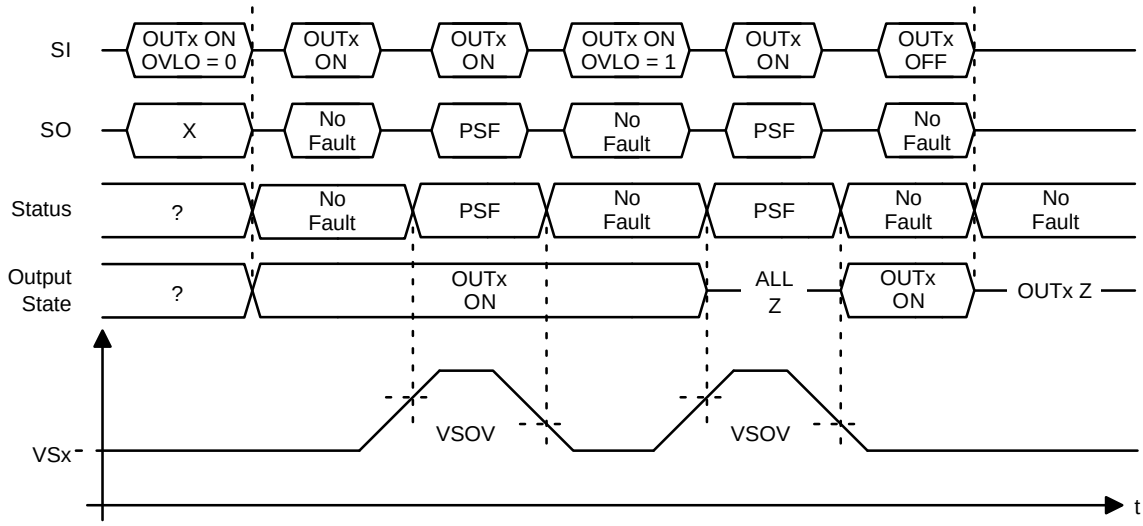



**Figure 22. Overvoltage Timing**

### Overcurrent Shutdown

*Global and per Channel Notification*
*Per Half−Bridge Operation*

Overcurrent detection and shutdown control is provided by monitoring each HS and LS driver. Overcurrent timing is shown in Figure 23. Overcurrent in either driver starts a channel's overcurrent delay timer (TdOc). If overcurrent exists after the delay, both drivers are latched off and the global overcurrent (OCS) status bit is set. The channel's corresponding HBSTx[1:0] bits are also set to "01" to indicate an OCS fault. Note that OCS fault reporting has priority over other faults as shown in Figure 14. The global OCS bit and individual channel bits are cleared and channels are re−activated by sending SRR = 1.

A persistent overcurrent cause should be resolved prior to re−activation to avoid repetitive stress on the drivers.

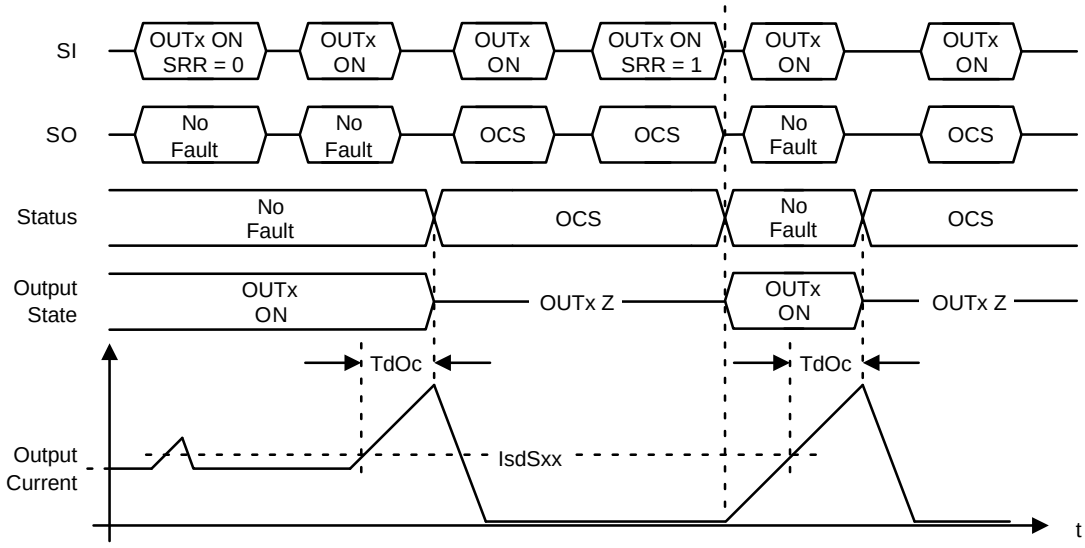



**Figure 23. Overcurrent Timing**

### Underload Shutdown

*Global and per Channel Notification*
*Global Shutdown Control, Per Half ĭ Bridge Operation*

Underload detection and shutdown control is provided by monitoring each half bridge driver. Underload timing is shown in Figure 24. Underload at any driver starts the global underload delay timer. If underload occurs in another channel after the global timer has been started, the delay for any subsequent underload will be the remainder of the timer.

If underload exists after the global delay timer and if the

### Thermal Warning and Thermal Shutdown

*Global Notification, Per Half ĭ Bridge Operation*

Thermal warning (TW) and thermal shutdown (TSD)

## THERMAL PERFORMANCE ESTIMATES

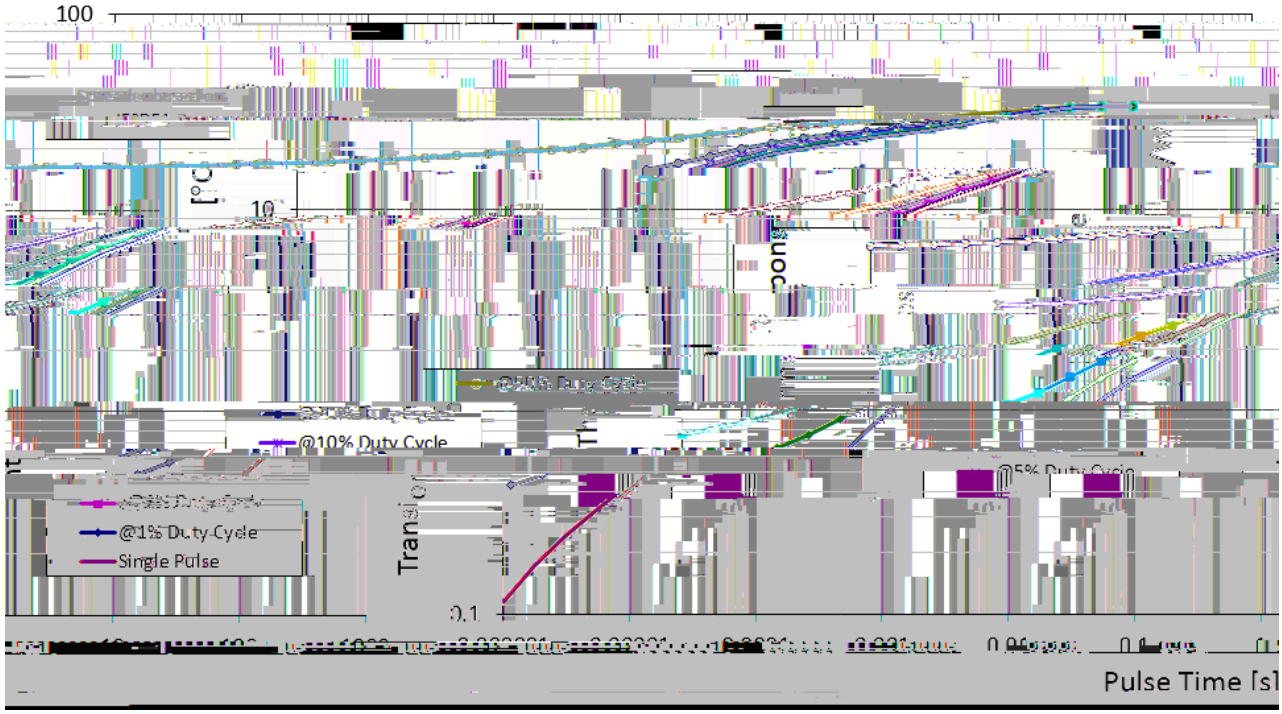
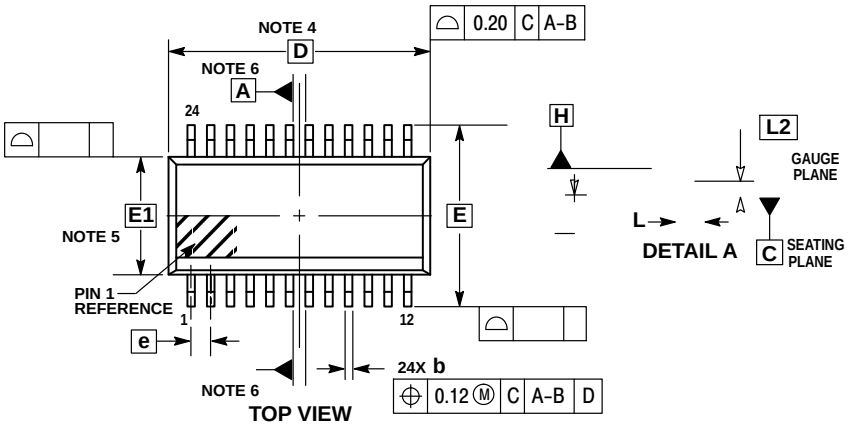


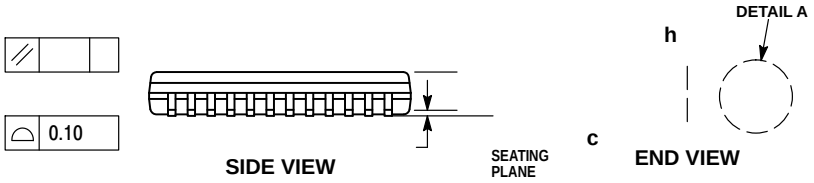

**Figure 26. Transient R(t) vs. Pulse Time for 2 oz Spreader**

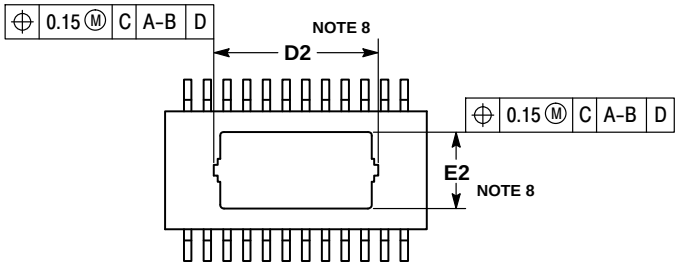
**SSOP24 NB EP**
CASE 940AK
ISSUE O

**SCALE 1:1**

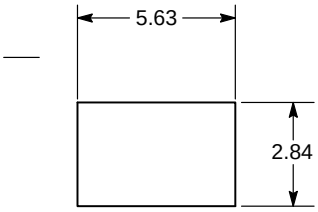
DATE 24 APR 2012




**SOLDERING FOOTPRINT**




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.10 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. DIMENSION b APPLIES TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D IS DETERMINED AT DATUM PLANE H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM PLANE H.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. CONTOURS OF THE THERMAL PAD ARE UNCONTROLLED WITHIN THE REGION DEFINED BY DIMENSIONS D2 AND E2.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | --- | 1.70 |
| A1 | 0.00 | 0.10 |
| | | |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |

| | | |
|---|---|---|
| D2 | 5.28 | 5.58 |

| | | |
|---|---|---|
| E1 | 3.90 BSC | |
| E2 | 2.44 | 2.64 |
| e | 0.65 BSC | |
| h | 0.25 | 0.50 |
| L | 0.40 | 0.85 |
| L1 | 1.00 REF | |
| L2 | 0.25 BSC | |
| M | 0° | 8° |