DATA SHEET

8 Channel Half-Bridge Driver

NCV7724B

The NCV7724B is an eight channel half-bridge driver with protection features designed specifically for automotive and industrial motion control applications. The product has independent controls and diagnostics, and the drivers can be operated in forward, reverse, brake, and high impedance states. The device is controlled via a 16 bit SPI interface and is daisy chain compatible. Outputs 1 and 2 can be controlled through an external PWM signal.

Features

- Low Quiescent Current Sleep Mode
- High–Side and Low–Side Drivers Connected in Half–Bridge Configurations
- Integrated Freewheeling Protection (LS and HS)
- 500 mA Typical, 1.1 A Peak Current
- R_{DS(on)} = 0.8 P. (Typ)
- OUT1 and QUT2 External PWM Control
- 5 MHz SPI Communication
- 16 Bit Frame Error Detection
- Daisy Chain Compatible with Multiple of 8 bit Devices
- Compliance with 3.3 V and 5 V Systems
- Undervoltage and Overvoltage Lockout
- •

1

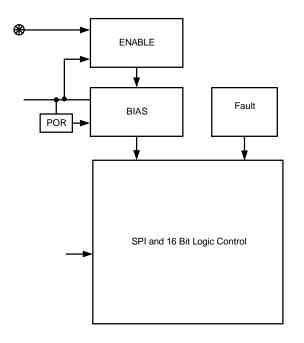


Figure 2. Block Diagram

о О	

MAXIMUM RATINGS (Voltages are with respect to GND)

	Rating	Symbol	Value	Unit
VSx Pin Voltage	(VS1, VS2) (DC) (AC), t < 500 ms, lvsx > 2 A	VsxdcMax VSxac	0.3 to 45 1.0	V
Pin Voltage	(Vcc, SI, SCLK, CSB, SO, EN, PWM1, PWM2)	VioMax	0.3 to 5.5	V
OUTx Pin Voltag	e (DC) (AC) (AC), t < 500 ms, IOUTx > 1.1 A (AC), t < 500 ms, IOUTx < 1 A	VoutxDc VoutxAc	0.3 to 45 0.3 to 45 1.0 1.0	V
OUTx Pin Currer	nt (OUT1,, OUT8)	loutxImax	2.0 to 2.0	А
Junction Temperature Range		TJ	40 to 150	°C
Storage Tempera	ature Range	Tstr	55 to 150	°C
Peak Reflow Sol	dering Temperature: Pb free 60 to 150 seconds at $217^{\circ}C$	(Note 1)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. 1. See or download **onsemi**'s Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ATTRIBUTES

Characteristic	Symbol	Value	Unit
Short Circuit Reliability Characterization	AECQ10x	Grade A	

ESD Capability

Human Body Model per AEC Q100per AEC1 4002 .9071 14.7T 40Sxac

ELECTRICAL CHARACTERISTICS

($~40^{\circ}C \leq T_J \leq 150^{\circ}C,~5.5~V \leq VSx \leq 40~V,~3.15~V \leq V_{CC} \leq 5.25~V,~EN$ = $V_{CC},~unless$ otherwise specified.)

Characteristic	Symbol	Conditions	Min	Тур	Max	Unit
POWER SUPPLIES						
Supply Current (VS1 + VS2) Sleep Mode	lqVSx85	$VS1 = VS2 = 13.2 V, V_{CC} = 0 V$ 40°C to 85°C		1.0	2.5	_ A
Supply Current (VS1 + VS2) Active Mode	lvsOp	EN = V _{CC} , 5.5V < VSx < 32 V No Load,All Outputs Off		0.5	1.0	mA
Supply Current (Vcc) Sleep Mode	IqV _{CC}	$CSB = V_{CC}, EN = SI = SCLK = 0 V$ $40^{\circ}C \text{ to } 85^{\circ}C$ $EN = CSB = V_{CC}, SI = SCLK = 0 V$		1.0	2.5	_ A
Active Mode	IV _{CC} Op	No Load, All Outputs Off		1.5	3.0	mA
Total Sleep Mode Current I(VS1) + I(VS2) + I(VCC)	lqTot	Sleep Mode, 40° C to 85° C VS1 = VS2 = 13.2 V, No Load		2.0	5.0	_ A
VCC Power on Reset Threshold	V _{CC} por	V _{CC} increasing		2.70	2.90	V
VSx Undervoltage Detection Threshold	VSxuv	VSx increasing	3.7	4.3	4.7	V
		VSx decreasing	3.5	4.1	4.5	
VSx Undervoltage Detection Hysteresis	VSxuHys			200		mV
VSx Overvoltage Detection Threshold	VsXov	VSx increasing	•	•	•	•

 $\label{eq:continued} \begin{array}{c} \textbf{ELECTRICAL CHARACTERISTICS} \\ (\ 40^{\circ}\text{C} \leq \text{T}_{J} \leq 150^{\circ}\text{C}, \ 5.5 \ \text{V} \leq \text{VSx} \leq 40 \ \text{V}, \ 3.15 \ \text{V} \leq \text{V}_{CC} \leq 5.25 \ \text{V}, \ \text{EN} = \text{V}_{CC}, \ \text{unless otherwise specified.}) \ (\text{continued}) \end{array}$

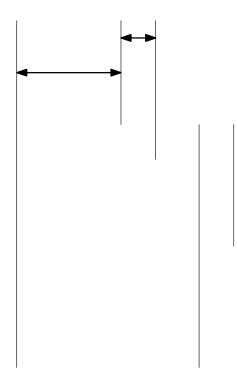
Characteristic	Symbol	Conditions	Min	Тур	Max	Unit
DRIVER OUTPUT SWITCHING CHAR	ACTERISTICS					
Low Side Off to High Side On Non Overlap Time	TIsOffHsOn	Vs = 13.2 V, R _{load} = 70 👧	5			S
PWM High to High Side On Time	ThsOnPWM	Vs = 13.2 V, R _{load} = 70 👧		120	165	S
PWM Low to High Side Off Time	ThsOffPWM	Vs = 13.2 V, R _{load} = 70 👧		20	45	S
PWM High to Low Side On Time	TIsOnPWM	Vs = 13.2 V, R _{load} = 70 🕰		120	165	S
PWM Low to Low Side Off Time	TIsOffPWM	Vs = 13.2 V, R _{load} = 70 🕰		35	75	S
THERMAL RESPONSE						
Thermal Warning	Twr	(Note 3)	120	140	170	°C
Thermal Warning Hysteresis	TwHy	(Note 3)		20		°C
Thermal Shutdown	Tsd	(Note 3)	150	175	200	°C
Thermal Shutdown Hysteresis	TsdHy	(Note 3)		20		°C

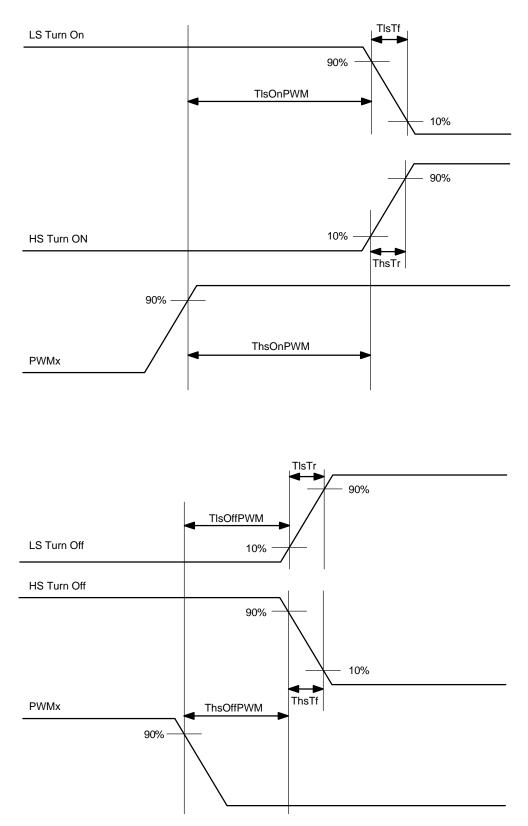
ELECTRICAL CHARACTERISTICS

($40^{\circ}C \le T_J \le 150^{\circ}C$, 5.5 V \le VSx ≤ 40 V, 3.15 V \le V_{CC} \le 5.25 V, EN = V_{CC}, unless otherwise specified.) (continued)

Characteristic	Symbol	Conditions	Timing Charts #	Min	Тур	Max	Unit
SERIAL PERIPHERAL INTERFACE							
SCLK Frequency	Fclk					5.0	MHz
SCLK Clock Period	TpClk	V _{CC} = 5 V V _{CC} = 3.3 V		200 500			ns
SCLK High Time	TclkH		1	85			ns
SCLK Low Time	TclkL		2	85			ns
SCLK Setup Time	TclkSup		3, 4	85			ns
SI Setup Time	TsiSup		11	•	•	•	•

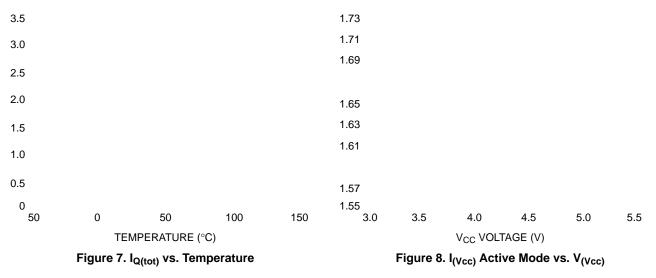
CHARACTERISTIC TIMING DIAGRAMS







TYPICAL CHARACTERISTICS



TEMPERATURE (°C) Figure 9. R_{DS(on)} vs. Temperature TEMPERATURE (

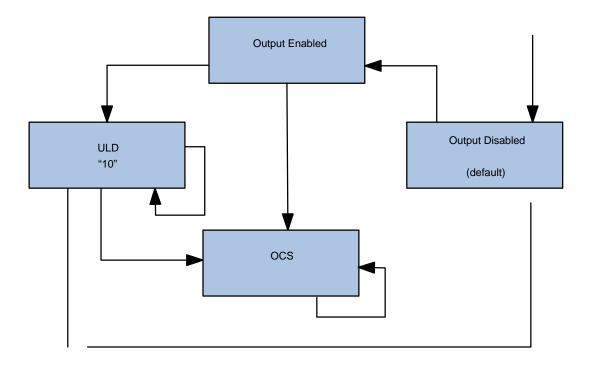
Figure 10. Body Diode Voltage vs. Temperature

Table 1. SPI COMMAND INPUT DEFINITIONS

		Channels 8 – 7	(Input Bit # 14 = 1)	
Bit#	Name	Function	Status*	Scope
15	SRR		-	

Table 2. SPI STATUS OUTPUT DEFINITIONS

		Channels 8 – 7 (If Pre	evious Input Bit # 14 = 1)	
Bit#	Name	Function	Status*	Scope
PRE_15	TSD	Latched Thermal Shutdown	1 = Fault	Global Notification; Per Half Bridge Operation
15	OCS	Latched Overcurrent Shutdown	1 = Fault	Notification per HBSEL ; Per Half Bridge Operation
14	PSF	VS1 and/or VS2 Undervoltage or Overvoltage	1 = Fault	Global Notification and Global Operation
13	ULD	Underload Detect	1 = Fault	Notification per HBSEL ; Per Half Bridge Operation
12				
11]			
10]			
9	x	Not Used		
8	X Not Used	Not Used		
7]			
6]			
5				
4		Holf Bridge & Output Statue	0x00b – Output Disabled	
3	HBST8 [1:0]	Half Bridge 8 Output Status 0x00b – Output Disabled 0x01b – OCS		Per Half Bridge
2	HBST7 [1:0] Half Bridge 7 Output Status		0x10b – ULD	rei nali biluye
1		Tail Bridge / Output Status	0x11b – Output Enabled	
0	TW	Thermal Warning	1 = Fault	Global Notification; Per Half Bridge Operation



 $\begin{array}{l} \mbox{CMD} [x, n] = \mbox{Command Word to Device `x', Length `n'} \\ \mbox{STA} [x, n] = \mbox{Status Word from Device `x', Length `n'} \\ \end{array}$

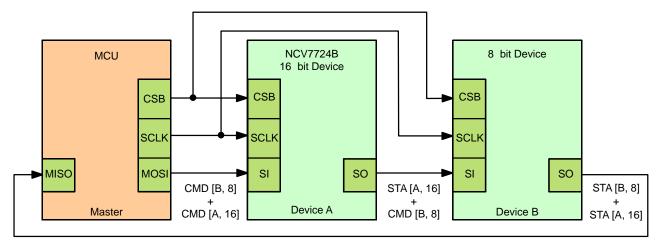


Figure 15. Daisy Chain Configuration

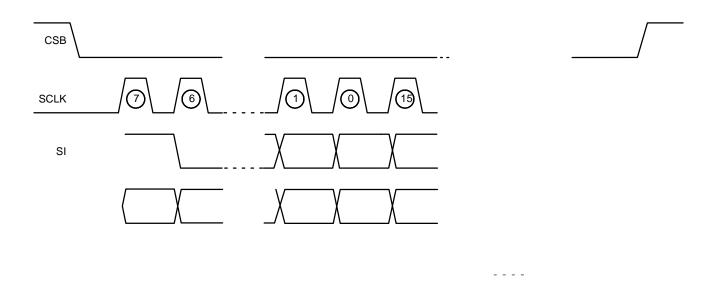
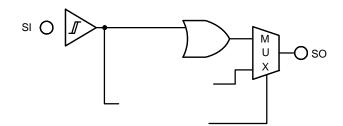


Figure 16. Daisy Chain – 24 bit Frame Format



/

Power Up/Down Control

The V_{CC} supply input powers the device's logic core. A V_{CC} power–on reset (POR) function provides controlled power–up/down. V_{CC} POR initializes the command input and status output registers to their default states (0x00), and ensures

DIAGNOSTICS, PROTECTIONS, STATUS REPORTING AND RESET

Overview

The NCV7724B employs diagnostics designed to prevent destructive overstress during a fault condition. Diagnostics are classified as either supervisory or protection functions (Table 3). Supervisory functions provide status information about device conditions. Protection functions provide status information and activate fault management behaviors. Diagnostics resulting in output shutdown and latched status may depend on a qualifier and may require user intervention for output recovery and status memory clear. Diagnostics resulting in output lockout and non–latched status (VSOV or VSUV) may recover and clear automatically. Output configurations can be changed during output lockout. Outputs assume the new configurations or resume the previous configurations when an auto–recover fault is resolved. Table 4 shows output states during faults and output recovery modes, and Table 5 shows the status memory and memory clear modes.

Table 3. DIAGNOSTIC CL01 ions can be chang62 9 310INTUS REmen

Diagnostics Details

The following sections describe individual diagnostics and behaviors. In each description and illustration, a SPI frame is assumed to always be valid and the SI data pattern sent for HBCNFx and HBENx is the same as the previous frame. Actual results can depend on asynchronous fault events and SPI clock frequency and frame rate.

Undervoltage Lockout

Global Notification, Global Operation

Undervoltage detection and lockout control is provided by monitoring the VS1 and VS2 supply inputs. Undervoltage hysteresis is provided to ensure clean detection transitions. Undervoltage timing is shown in Figure 21.

OUTx

Undervoltage at either VSx input turns off all outputs and sets the power supply fail (PSF) status bit. The outputs return to their previously programmed state and the PSF status bit is cleared when VSx rises above the hysteresis voltage level. SPI communication is available and programmed output enable and configuration states are maintained if proper VCC is present during VSx undervoltage. Output enable and configuration states can also be programmed during VSx undervoltage if proper VCC is present, and state changes will take effect as VSx rises above the undervoltage threshold level. VCC undervoltage turns all outputs off and clears the command input and status output registers.

Underload Shutdown

Global and per Channel Notification per HBSEL Shutdown Control per HBSEL, Per Half–Bridge Operation

Underload detection and shutdown control is provided by monitoring each half bridge driver. Underload timing is shown in Figure 24. Underload at any driver starts the global underload delay timer. If underload occurs in another channel after the global timer has been started, the delay for any subsequent underload will be the remainder of the timer.

If underload exists after the global delay timer and if the underload shutdown (ULDSC) command bit is set, both HSand LS drivers are latched off and the global underload (ULD) status bit is set along with the corresponding per channel status bits HBSTx[1:0] set to "10". Drivers will remain on if the ULDSC input bit is 0 (see Table 4 and 5). The global ULD bit and per channel HBSTx bits are cleared and channels are re-activated by sending SRR = 1 (HBSEL = X).

NOTE: underload may result from a fault (e.g. open-load)

Thermal Warning and Thermal Shutdown

Global Notification, Per Half-Bridge Operation Thermal warning (TW) and thermal shutdown (TSD)

THERMAL PERFORMANCE ESTIMATES

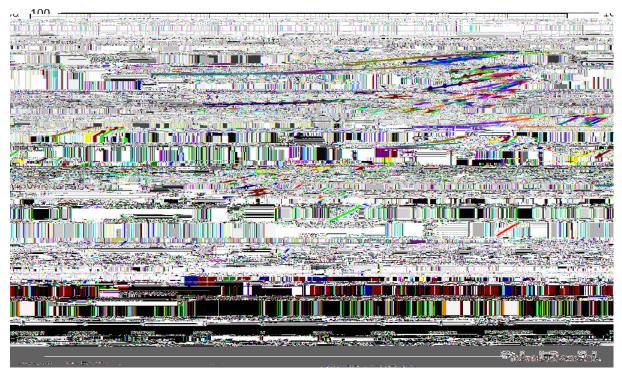


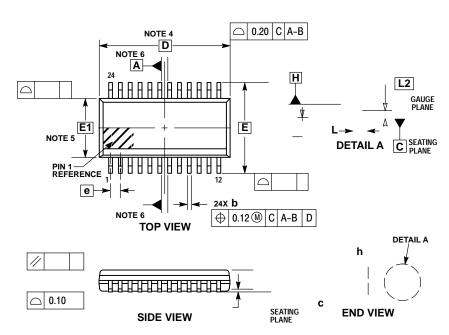
Figure 26. Transient R(t) vs. Pulse Time for 2 oz Spreader

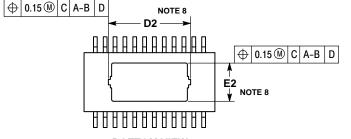
ORDERING INFORMATION

Device	Package	Shipping [†]
NCV7724DQBR2G	SSOP24 NB EP (Pb Free)	2500 / Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

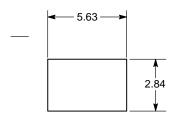






BOTTOM VIEW

SOLDERING FOOTPRINT



- NOTES:
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: MILLIMETERS. 3. DIMENSION b DOES NOT INCLUDE DAMBAR
- PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.10 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. DIMENSION 6 APPLIES TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
- FROM THE LEAD TIP.
 DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D IS DETERMINED AT DATUM PLANE H.
 DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR DROTBUISION SHALL NOT EXCEED 0.25 PER
- OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED AT DA-
- TUM PLANE H. 6. DATUMS A AND B ARE DETERMINED AT DATUM
- 7.
- DATUMS A AND B ARE DETERMINED AT DATE: PLANE H. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY. CONTOURS OF THE THERMAL PAD ARE UN-CONTROLLED WITHIN THE REGION DEFINED SY DIMENSIONS DO AND F2 8. BY DIMENSIONS D2 AND E2.

MILLIMETERS			
MIN	MAX		
	1.70		
0.00	0.10		
0.19	0.30		
0.09	0.20		
	MIN 0.00 0.19		

D2	5.28	5.58
E1	3.90	BSC
E2	2.44	2.64
е	0.65	BSC
h	0.25	0.50
L	0.40	0.85
11	1 00	RFF

0.25 BSC 0° 8 8

L2 M

0

onsemi, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries. onsemi owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of onsemi's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. Onsemi reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and onsemi makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or incruit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using onsemi