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NCV7725B

The NCV7725B is a ten channel half bridge driver with protection features designed specifically for automotive and industrial motion control applications. The product has independent controls and diagnostics, and the drivers can be operated in forward, reverse, brake, and high impedance states. The device is controlled via a 16 bit SPI interface and is daisy chain compatible. Outputs 1 and 2 can be controlled through an external PWM signal.

MARKING DIAGRAM

SSOP24 NB EP
CASE 940AK

Features

- Low Quiescent Current Sleep Mode
- High Side and Low Side Drivers Connected in Half Bridge Configurations
- Integrated Freewheeling Protection (LS and HS)
- 500 mA Typical, 1.1 A Peak Current
- $R_{DS(on)}$ = 0.8 Ω (Typ)
- OUT1 and OUT2 External PWM Control
- 5 MHz SPI Communication
- 16 Bit Frame Error Detection
- Daisy Chain Compatible with Multiple of 8 bit Devices
- Compliance with 3.3 V and 5 V Systems
- Undervoltage and Overvoltage Lockout
- Per Channel Fault Reporting
- Overcurrent Protection
- Overtemperature Protection
- Underload Detection (HS and LS)
- Exposed Pad Package
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC Q100 Qualified and PPAP Capable
- This is a Pb Free Device

Typical Applications

- Automotive
- Industrial
- DC Motor Management for HVAC Application

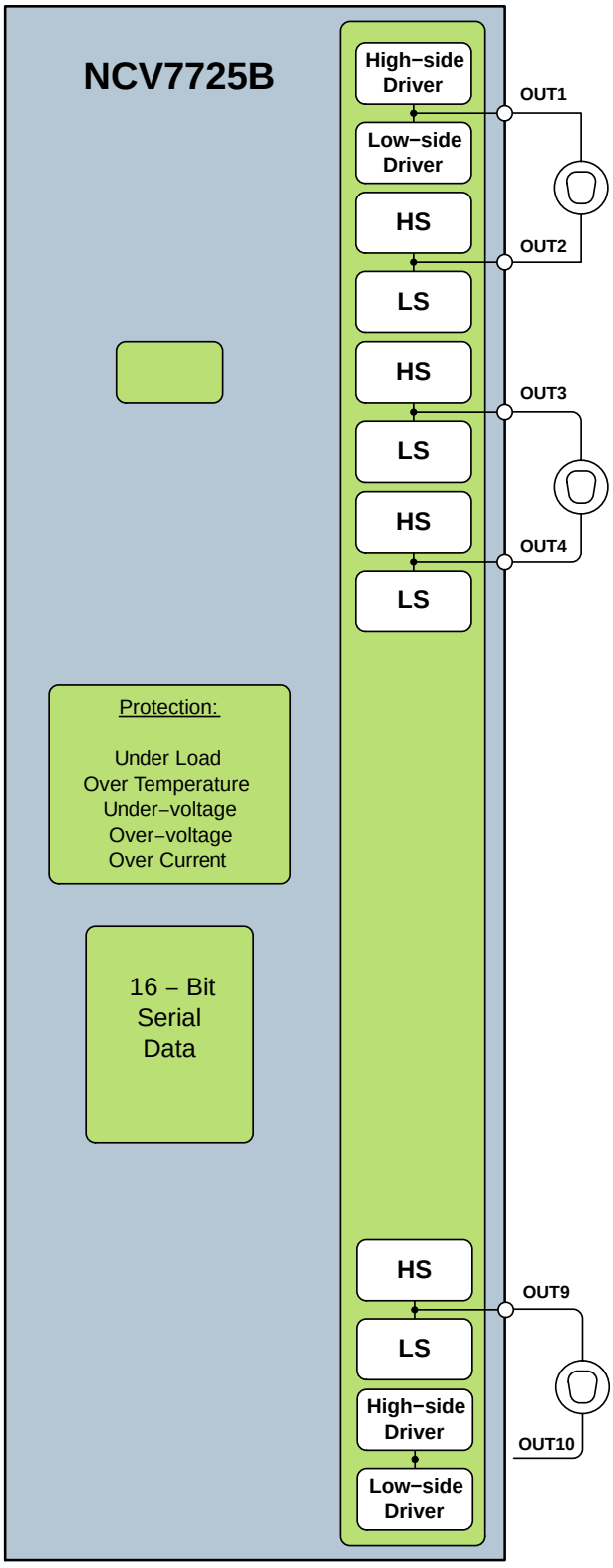


Figure 1. Typical Application

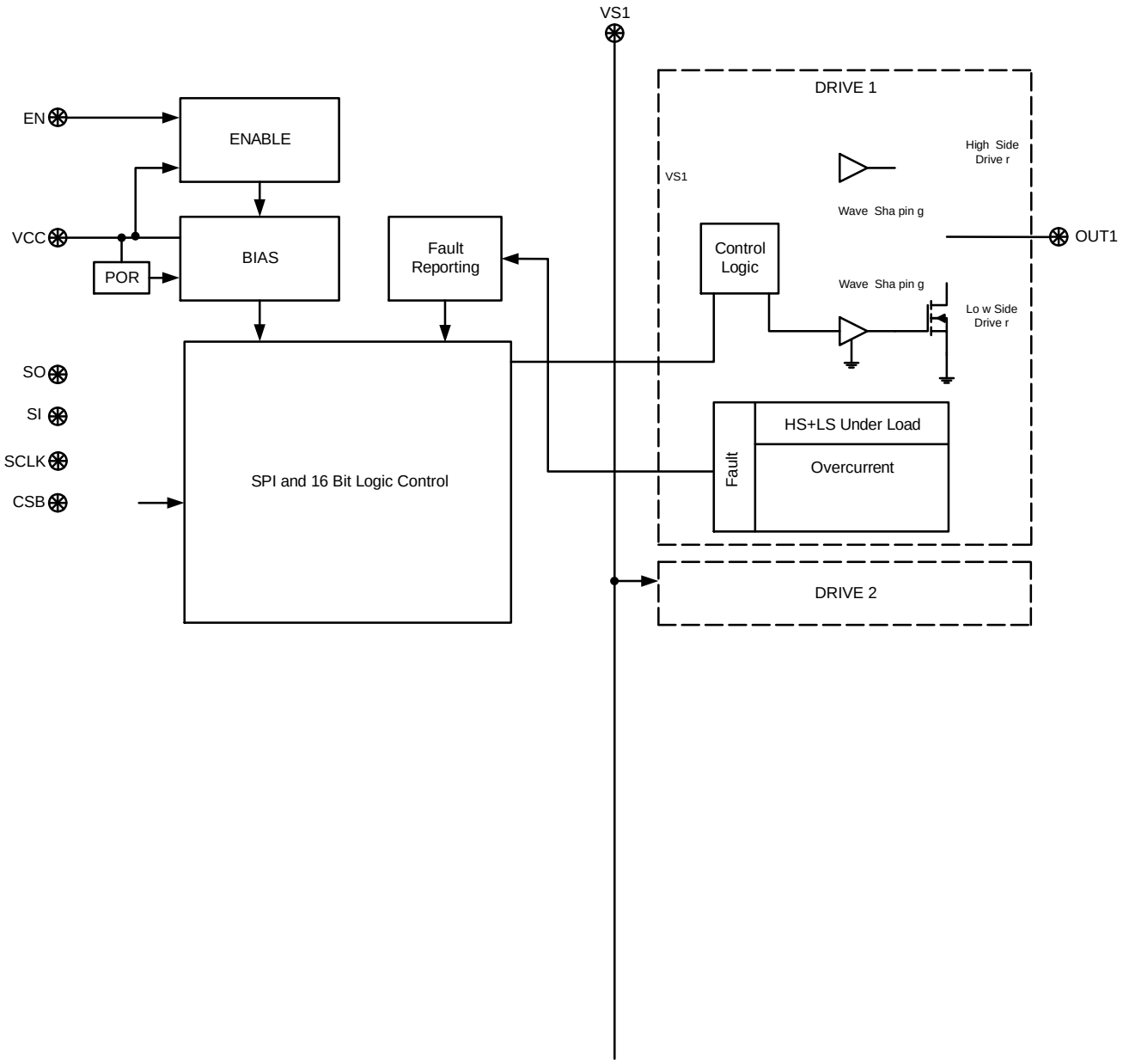


Figure 2. Block Diagram

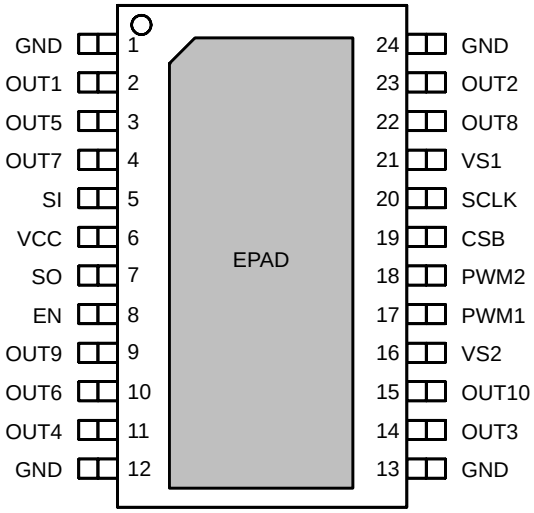


Figure 3. Pinout – SSOP24 NB EP

PIN FUNCTION DESCRIPTION The pin−out for the Half−Bridge Driver in SSOP24 NB EP package is shown in the table below.

Pin# SSOP24	Symbol	Description
1	GND	Ground. Must be connected to other GND pins externally.
2	OUT1	Half−bridge output 1
3	OUT5	Half−bridge output 5
4	OUT7	Half−bridge output 7
5	SI	16 bit serial communication input. 3.3 V / 5 V (TTL) Compatible – internally pulled down.
6	VCC	Power supply input for Logic.
7	SO	16 bit serial communication output. 3.3 V / 5 V Compliant
8	EN	Enable – active high; wakes the device from sleep mode. 3.3 V / 5 V (TTL) Compatible – internally pulled down.
9	OUT9	Half−bridge output 9
10	OUT6	Half−bridge output 6
11	OUT4	Half−bridge output 4
12	GND	Ground. Must be connected to other GND pins externally.
13	GND	Ground. Must be connected to other GND pins externally.
14	OUT3	Half−bridge output 3
15	OUT10	Half−bridge output 10
16	VS2	Power Supply input for outputs 3, 4, 6, 9, and 10. This pin must be connected to VS1 externally.
17	PWM1	External PWM input for output 1. 3.3 V / 5 V (TTL) Compatible – internally pulled down.
18	PWM2	External PWM input for output 2. 3.3 V / 5 V (TTL) Compatible – internally pulled down.
19	CSB	Chip select bar – active low; enables serial communication operation. 3.3 V / 5 V (TTL) Compatible – internally pulled up.
20	SCLK	Serial communication clock input. 3.3 V / 5 V (TTL) Compatible – internally pulled down.
21	VS1	Power Supply input for outputs 1, 2, 5, 7, and 8. This pin must be connected to VS2 externally.
22	OUT8	Half−bridge output 8
23	OUT2	Half−bridge output 2
24	GND	Ground. Must be connected to other GND pins externally.
EPAD	Exposed Pad	Connect to GND or leave unconnected.

MAXIMUM RATINGS (Voltages are with respect to GND)

Rating		Symbol	Value	Unit
VSx Pin Voltage	(VS1, VS2) (DC) (AC), t < 500 ms, Ivsx > −2 A	 VsxdcMax VSxac	 −0.3 to 45 −1.0	V
Pin Voltage	(Vcc, SI, SCLK, CSB, SO, EN, PWM1, PWM2)	VioMax	−0.3 to 5.5	V
OUTx Pin Voltage (DC) (AC) (AC), t < 500 ms, IOUTx > −1.1 A (AC), t < 500 ms, IOUTx < 1 A		 VoutxDc VoutxAc	 −0.3 to 45 −0.3 to 45 −1.0 1.0	V
OUTx Pin Current (OUT1, ..., OUT10)		IoutxImax	−2.0 to 2.0	A
Junction Temperature Range		T_J	−40 to 150	°C
Storage Temperature Range		Tstr	−55 to 150	°C
Peak Reflow Soldering Temperature: Pb−free 60 to 150 seconds at 217°C		(Note 1)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. See or download **onsemi**'s Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ATTRIBUTES

Characteristic		Symbol	Value	Unit
Short Circuit Reliability Characterization		AECQ10x	Grade A	
ESD Capability Human Body Model per AEC−Q100−002 Charged Device Model per AEC−Q100−011	 VSx, OUTx All Other Pins	 Vesd4k Vesd2k Vesd750	 ≥ ±4.0 kV ≥ ±2.0 kV ≥ ±750 V	
Moisture Sensitivity Level		MSL	MSL2	
Package Thermal Resistance – Still−air Junction–to–Ambient Junction–to–Board	 (Note 2) (Note 2)	 $R_{\theta JA}$ $R_{\Psi JBOARD}$	 31.0 12.0	 °C/W °C/W

2. Based on JESD51−7, 1.6 mm thick FR4, 2S2P PCB with 600 mm^2 2 oz. copper and 18 thermal vias to 80x80 mm 1 oz. internal spreader planes. Simulated with each channel dissipating 0.2 W.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Digital Supply Input Voltage	VCCOp	3.15	5.25	V
Battery Supply Input Voltage (VS1 = VS2)	VSxOp	5.5	32	V
DC Output Current	IxOp	–	0.5	A
Junction Temperature	TjOp	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

(−40°C ≤ T_J ≤ 150°C, 5.5 V ≤ VSx ≤ 40 V, 3.15 V ≤ V_{CC} ≤ 5.25 V, EN = V_{CC}, unless otherwise specified.)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
POWER SUPPLIES						
Supply Current (VS1 + VS2) Sleep Mode	IqVSx85	VS1 = VS2 = 13.2 V, V_{CC} = 0 V −40°C to 85°C	–	1.0	2.5	μA

ELECTRICAL CHARACTERISTICS

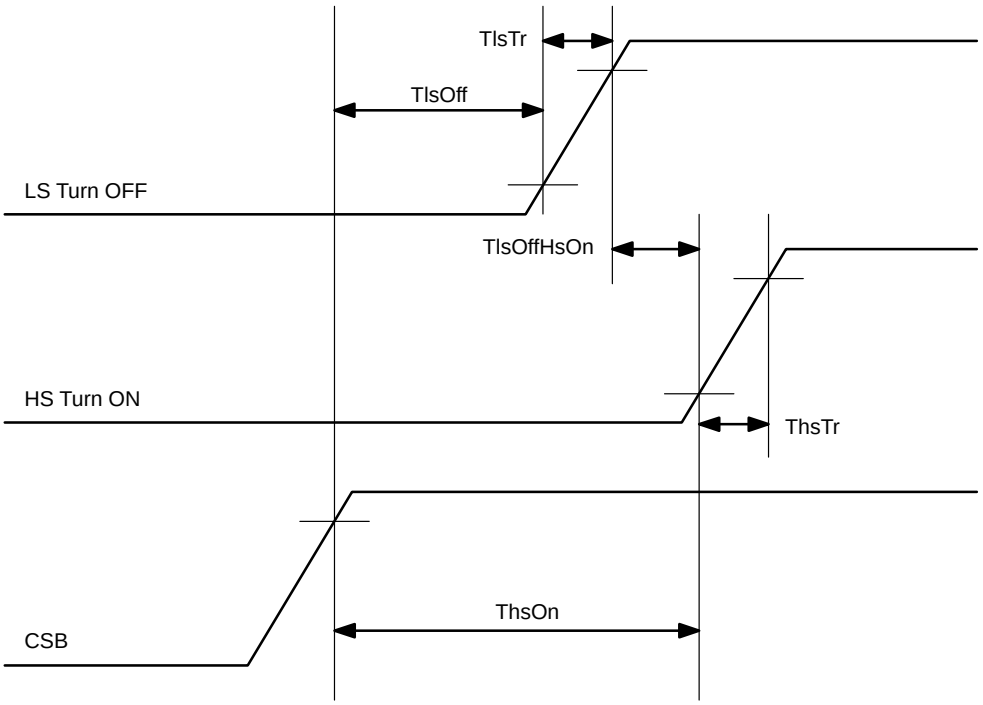
(−40°C ≤ T_J ≤ 150°C, 5.5 V ≤ VSx ≤ 40 V, 3.15 V ≤ V_{CC} ≤ 5.25 V, EN = V_{CC}, unless otherwise specified.) (continued)

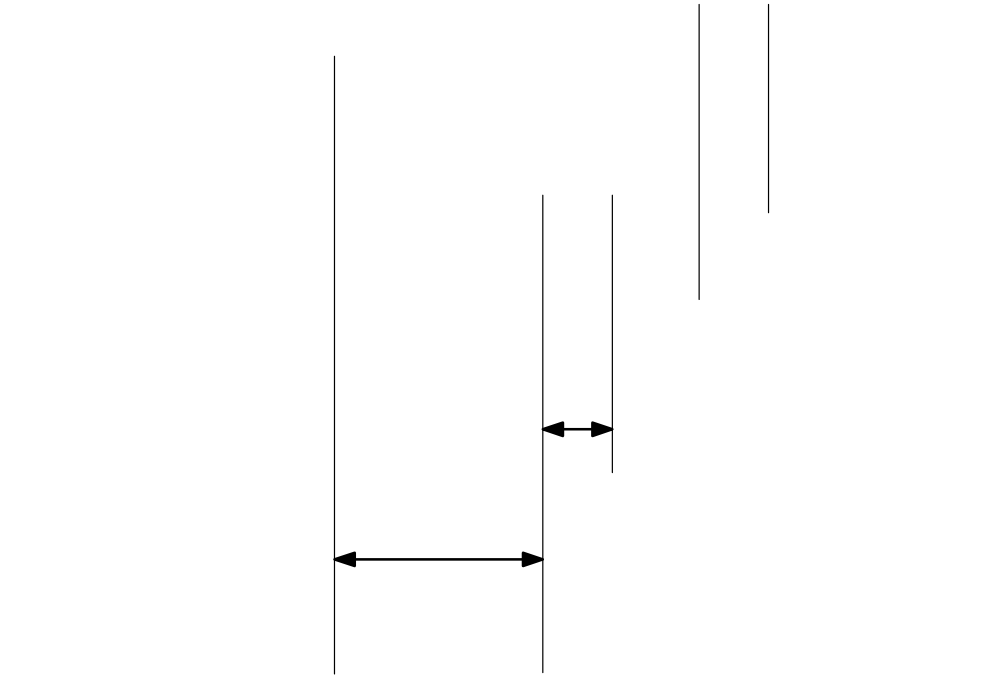
Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
DRIVER OUTPUT SWITCHING CHARACTERISTICS						
Low Side Off to High Side On Non−Overlap Time	TlsOffHsOn	Vs = 13.2 V, R_{load} = 70 Ω	5	–	–	μs
PWM High to High Side On Time	ThsOnPWM	Vs = 13.2 V, R_{load} = 70 Ω	–	120	165	μs
PWM Low to High Side Off Time	ThsOffPWM	Vs = 13.2 V, R_{load} = 70 Ω	–	20	45	μs
PWM High to Low Side On Time	TlsOnPWM	Vs = 13.2 V, R_{load} = 70 Ω	–	120	165	μs
PWM Low to Low Side Off Time	TlsOffPWM	Vs = 13.2 V, R_{load} = 70 Ω	–	35	75	μs
THERMAL RESPONSE						
Thermal Warning	Twr	(Note 3)	120	140	170	°C
Thermal Warning Hysteresis	TwHy	(Note 3)	–	20	–	°C
Thermal Shutdown	Tsd	(Note 3)	150	175	200	°C
Thermal Shutdown Hysteresis	TsdHy	(Note 3)	–	20	–	°C

ELECTRICAL CHARACTERISTICS
(–40°C ≤ T_J ≤ 150°C, 5.5 V ≤ VSx ≤ 40 V, 3.15 V ≤ V_{CC} ≤ 5.25 V, EN = V_{CC}, unless otherwise specified.) (continued)

Characteristic	Symbol	Conditions	Timing Charts #	Min	Typ	Max	Unit
SERIAL PERIPHERAL INTERFACE							
SCLK Frequency	Fclk		–	–	–	5.0	MHz
SCLK Clock Period	TpClk	V_{CC} = 5 V V_{CC} = 3.3 V	 –	200 500	– –	– –	ns
SCLK High Time	TclkH		1	85	–	–	ns
SCLK Low Time	TclkL		2	85	–	–	ns
SCLK Setup Time	TclkSup		3, 4	85	–	–	ns
SI Setup Time	TsiSup		11				

CHARACTERISTIC TIMING DIAGRAMS





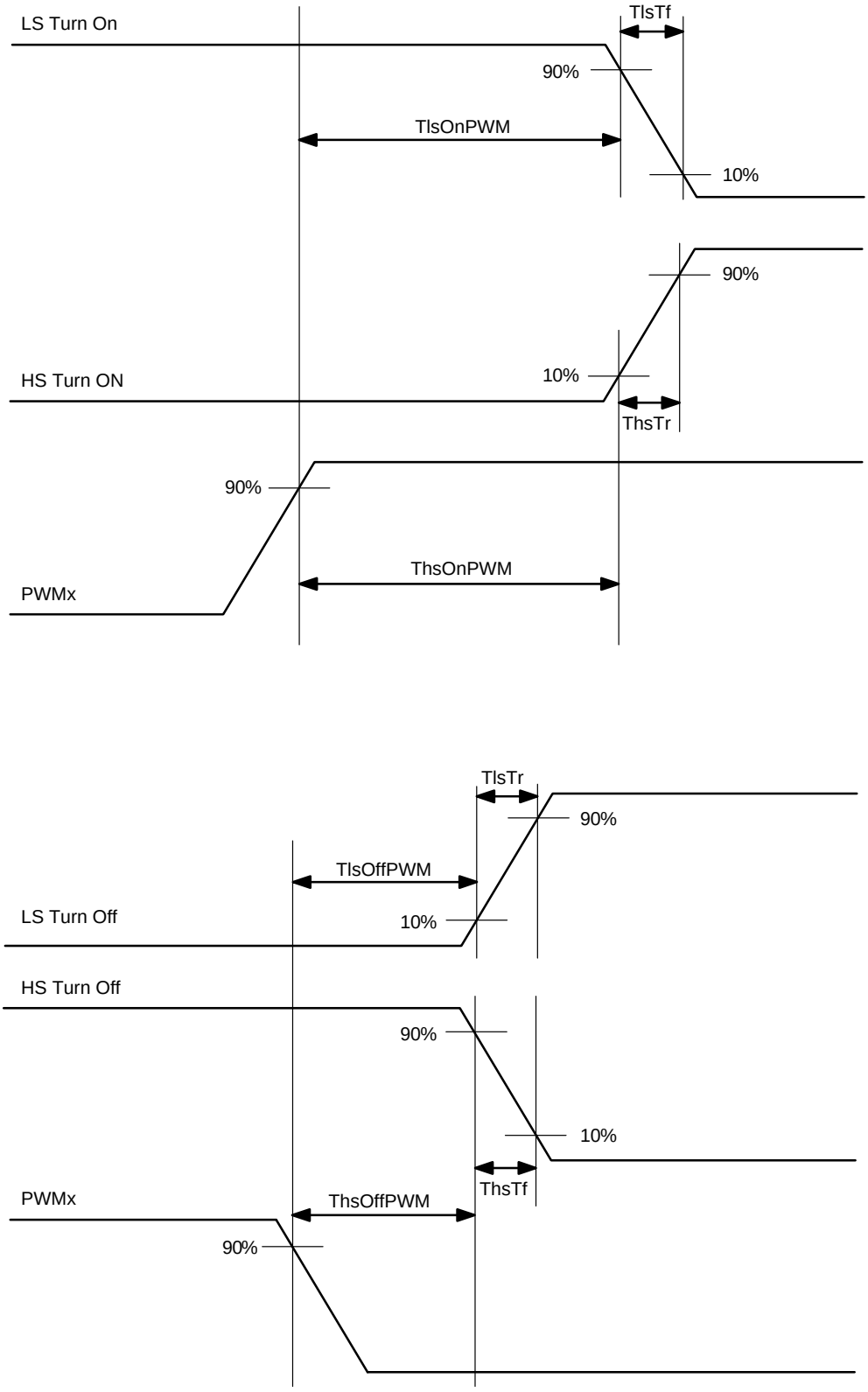


Figure 5. Detailed Driver Timing (OUT1 / OUT2 PWM)

TYPICAL CHARACTERISTICS

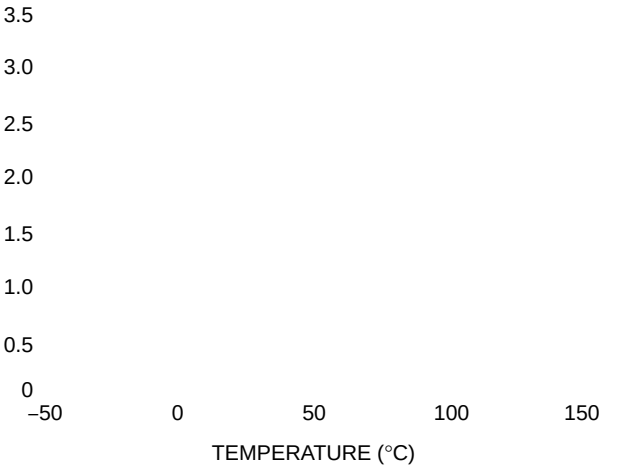


Figure 7. $I_{Q(tot)}$ vs. Temperature

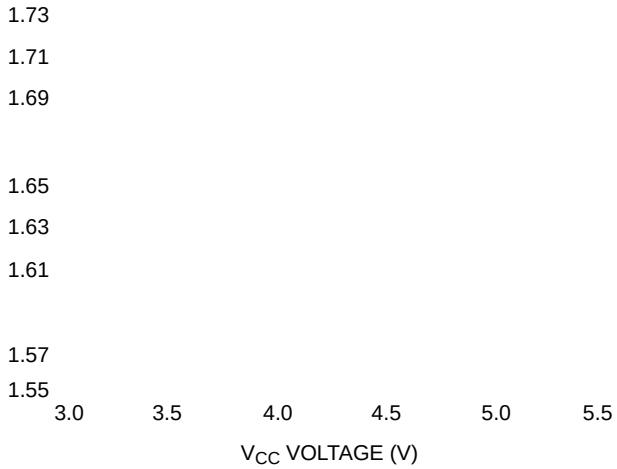


Figure 8. $I_{(Vcc)}$ Active Mode vs. $V_{(Vcc)}$

TEMPERATURE (°C)

Figure 9. $R_{DS(on)}$ vs. Temperature

TEMPERATURE (

Figure 10. Body Diode Voltage vs. Temperature

DETAILED OPERATING DESCRIPTION

General Overview

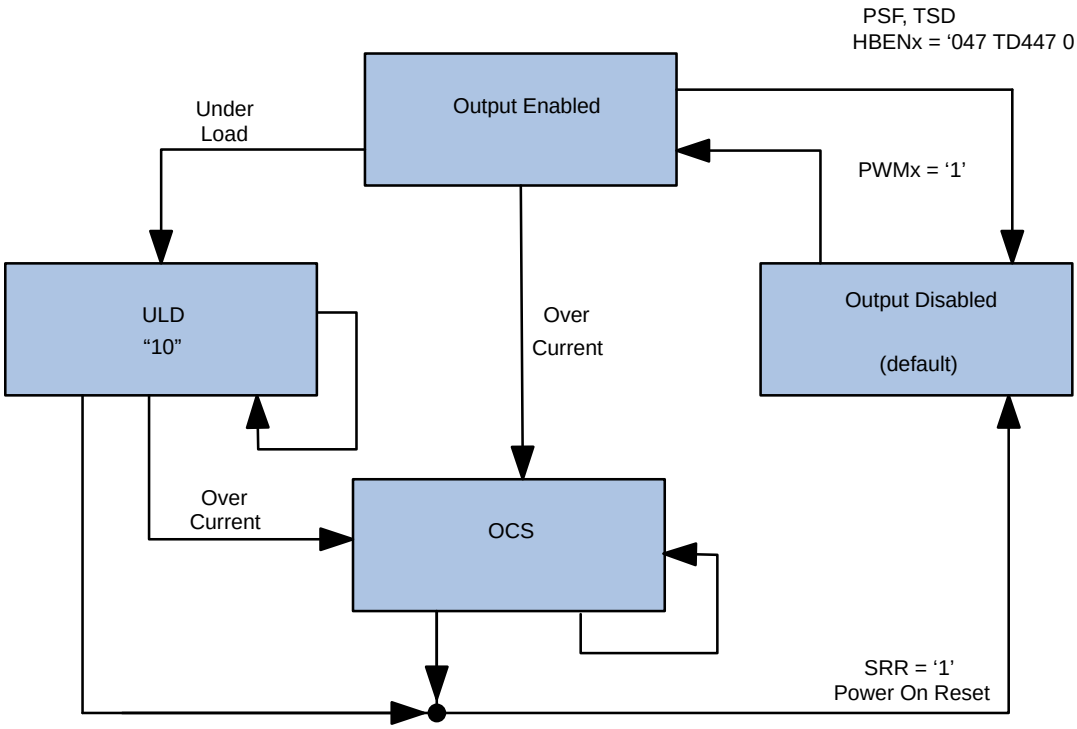
The NCV7725B is comprised of twenty NMOS power drivers. The drivers are arranged as ten half

Table 1. SPI COMMAND INPUT DEFINITIONS

Channels 10 – 7 (Input Bit # 14 = 1)				
Bit#	**Name**	**Function**	**Status***	**Scope**
15	SRR	Status Register Reset**	1 = Reset	

Table 2. SPI STATUS OUTPUT DEFINITIONS

Channels 10 – 7 (If Previous Input Bit # 14 = 1)				
Bit#	**Name**	**Function**	**Status***	**Scope**
PRE_15	TSD	Latched Thermal Shutdown	1 = Fault	Global Notification; Per Half−Bridge Operation
15	OCS	Latched Overcurrent Shutdown	1 = Fault	Notification per **HBSEL**; Per Half−Bridge Operation
14	PSF	VS1 and/or VS2 Undervoltage or Overvoltage	1 = Fault	Global Notification and Global Operation
13	ULD	Underload Detect	1 = Fault	Notification per **HBSEL**; Per Half−Bridge Operation
12	X	Not Used	–	–
11				
10				
9				
8	HBST10 [1:0]	Half−Bridge 10 Output Status	0x00b – Output Disabled 0x01b – OCS 0x10b – ULD 0x11b – Output Enabled	Per Half−Bridge
7				
6	HBST9 [1:0]	Half−Bridge 9 Output Status		
5				
4	HBST8 [1:0]	Half−Bridge 8 Output Status		
3				
2	HBST7 [1:0]	Half−Bridge 7 Output Status		
1				
0	TW	Thermal Warning	1 = Fault	Global Notification; Per Half−Bridge Operation
Channels 6 – 1 (If Previous Input Bit # 14 = 0)				
Bit#	**Name**	**Function**	**Status***	**Scope**
PRE_15	TSD	Latched Thermal Shutdown	1 = Fault	Global Notification; Per Half−Bridge Operation
15	OCS	Latched Overcurrent Shutdown	1 = Fault	
14	PSF	VS1 and/or VS2 Undervoltage or Overvoltage	1 = Fault	Global Notification; Global Operation
13	ULD	Underload Detect	1 = Fault	Global Notification; Per Half−Bridge Operation
12	HBST6 [1:0]	Half Bridge 6 Output Status	0x00b – Output Disabled 0x01b – OCS 0x10b – ULD 0x11b – Output Enabled	Per Half−Bridge
11				
10	HBST5 [1:0]	Half Bridge 5 Output Status		
9				
8				


PSF, TSD
HBENx = ‘047 TD447 0 l332.441057 ladFigure0 m SC
Output Enabled
Under
Load
PWMx = ‘1’
ULD
“10”
Over
Current
Output Disabled
(default)
Over
Current
OCS
SRR = ‘1’
Power On Reset

CMD [x, n] = Command Word to Device ‘x’, Length ‘n’
STA [x, n] = Status Word from Device ‘x’, Length ‘n’

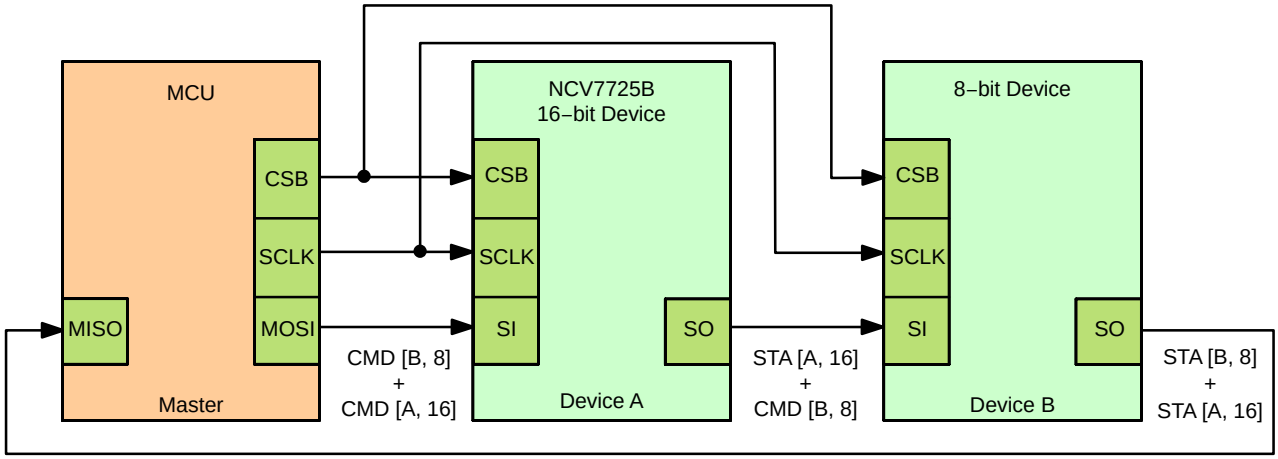


Figure 15. Daisy Chain Configuration

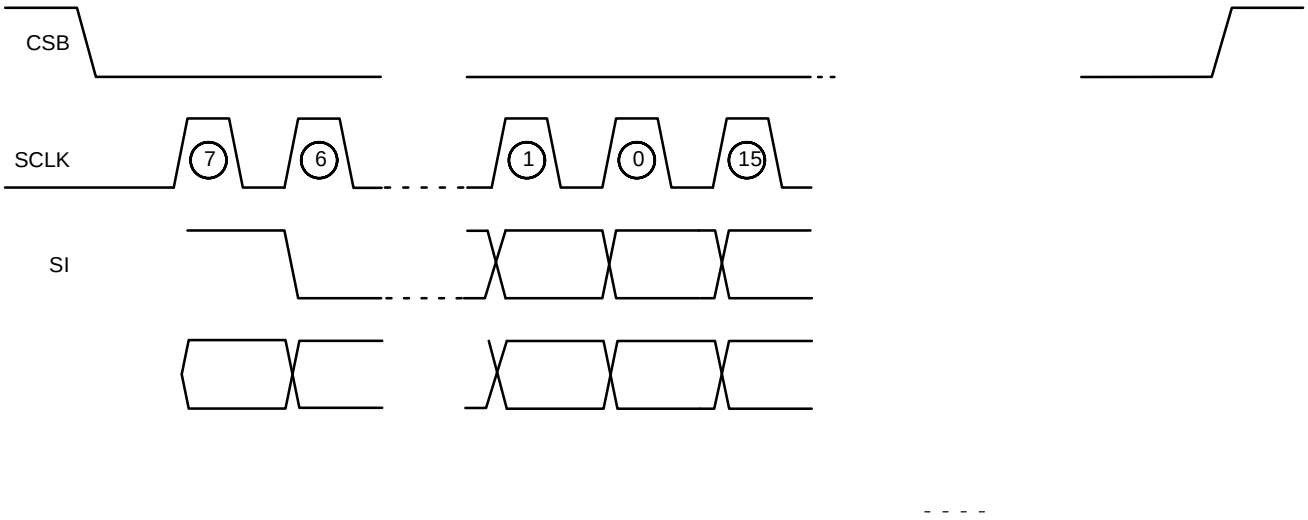
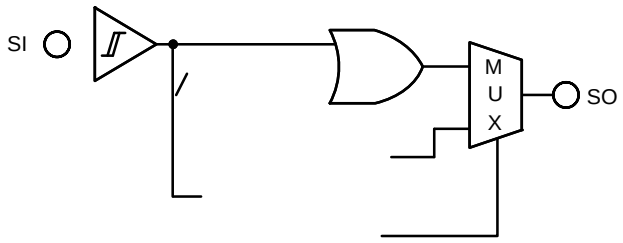


Figure 16. Daisy Chain – 24 bit Frame Format


SI
M
U
X
SO

Power Up/Down Control

The V_{CC} supply input powers the device's logic core. A V_{CC} power on reset (POR) function provides controlled power up/down. V_{CC} POR initializes the command input and status output registers to their default states (0x00), and ensures

DIAGNOSTICS, PROTECTIONS, STATUS REPORTING AND RESET

Overview

The NCV7725B employs diagnostics designed to prevent destructive overstress during a fault condition. Diagnostics are classified as either supervisory or protection functions (Table 3). Supervisory functions provide status information about device conditions. Protection functions provide status information and activate fault management behaviors. Diagnostics resulting in output shutdown and latched status may depend on a qualifier and may require user intervention for output recovery and status memory clear. Diagnostics resulting in output lockout and non latched status (VSOV or VSUV) may recover and clear automatically. Output configurations can be changed during output lockout. Outputs assume the new configurations or resume the previous configurations when an auto recover fault is resolved. Table 4 shows output states during faults and output recovery modes, and Table 5 shows the status memory and memory clear modes.

Table 3. DIAGNOSTIC CLASSES AND FUNCTIONS

Name	Class	Function
TSD	Protection	Thermal Shutdown
OCS	Protection	Overcurrent Shutdown
PSF	Protection	Under/overvoltage Lockout (OVLO = 1)
ULD	Protection	Underload Shutdown
HBSTx[1:0]	Supervisory	Half−Bridge X Output Status
TW	Supervisory	Thermal Warning

Table 4. OUTPUT STATE VS. FAULT AND OUTPUT RECOVERY

Fault	Qualifier	OUTx State	OUTx Recovery	OUTx Recovery Scope
TSD	–	$\rightarrow Z$	Send SRR	Per HBSEL
OCS	–	$\rightarrow Z$	Send SRR	Per HBSEL
PSF – VSOV	OVLO = 1	$\rightarrow Z \rightarrow Y_n \mid Y_{n+1}$	Auto*	All Outputs
	OVLO = 0	Unaffected	–	–
PSF – VSUV	–	$\rightarrow Z \rightarrow Y_n \mid Y_{n+1}$	Auto*	All Outputs

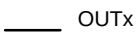
Diagnostics Details

The following sections describe individual diagnostics and behaviors. In each description and illustration, a SPI frame is assumed to always be valid and the SI data pattern sent for HBCNFx and HBENx is the same as the previous frame. Actual results can depend on asynchronous fault events and SPI clock frequency and frame rate.

Undervoltage Lockout

Global Notification, Global Operation

Undervoltage detection and lockout control is provided by monitoring the VS1 and VS2 supply inputs. Undervoltage hysteresis is provided to ensure clean detection transitions. Undervoltage timing is shown in Figure 21.



Undervoltage at either VSx input turns off all outputs and sets the power supply fail (PSF) status bit. The outputs return to their previously programmed state and the PSF status bit is cleared when VSx rises above the hysteresis voltage level. SPI communication is available and programmed output enable and configuration states are maintained if proper VCC is present during VSx undervoltage. Output enable and configuration states can also be programmed during VSx undervoltage if proper VCC is present, and state changes will take effect as VSx rises above the undervoltage threshold level. VCC undervoltage turns all outputs off and clears the command input and status output registers.

Underload Shutdown

Global and per Channel Notification per HBSEL
Shutdown Control per HBSEL,
Per Half−Bridge Operation

Underload detection and shutdown control is provided by monitoring each half bridge driver. Underload timing is shown in Figure 24. Underload at any driver starts the global underload delay timer. If underload occurs in another channel after the global timer has been started, the delay for any subsequent underload will be the remainder of the timer.

If underload exists after the global delay timer and if the underload shutdown (ULDSC) command bit is set, both HSand LS drivers are latched off and the global underload (ULD) status bit is set along with the corresponding per channel status bits HBSTx[1:0] set to “10”. Drivers will remain on if the ULDSC input bit is 0 (see Table 4 and 5). The global ULD bit and per channel HBSTx bits are cleared and channels are re activated by sending SRR = 1 (HBSEL = X).

NOTE: underload may result from a fault (e.g. open load)

Thermal Warning and Thermal Shutdown

Global Notification, Per Half−Bridge Operation

Thermal warning (TW) and thermal shutdown (TSD)

THERMAL PERFORMANCE ESTIMATES

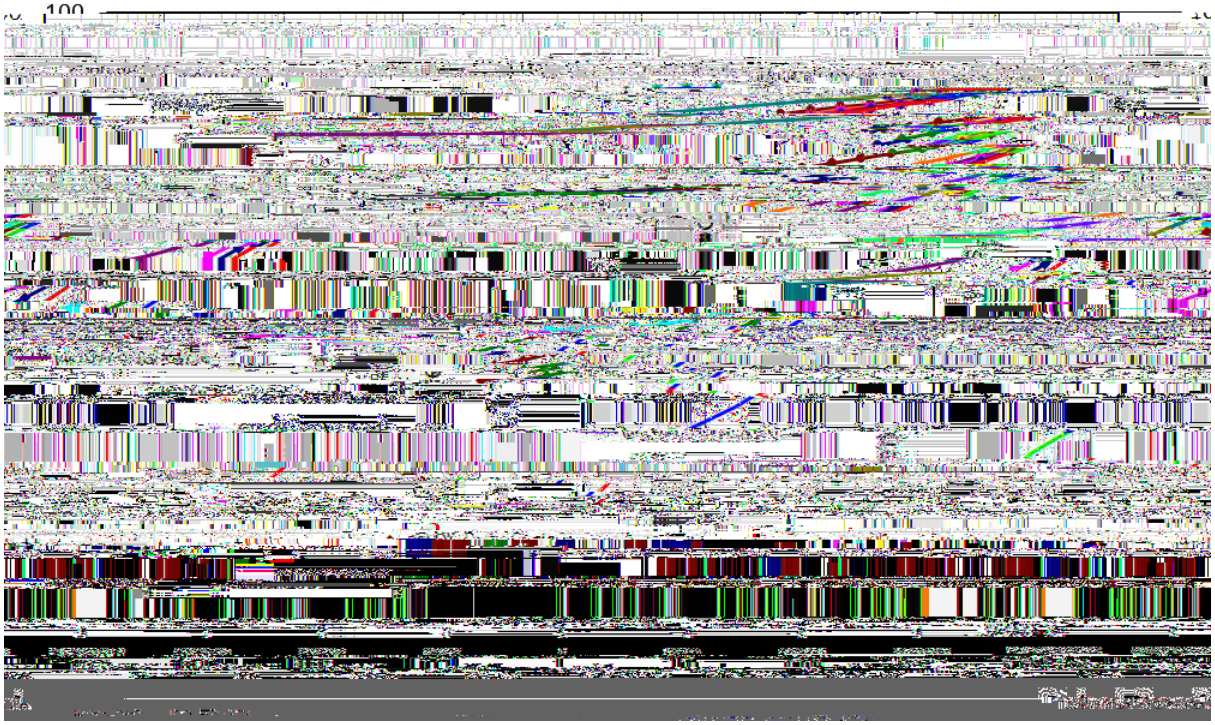


Figure 26. Transient R(t) vs. Pulse Time for 2 oz Spreader

ORDERING INFORMATION

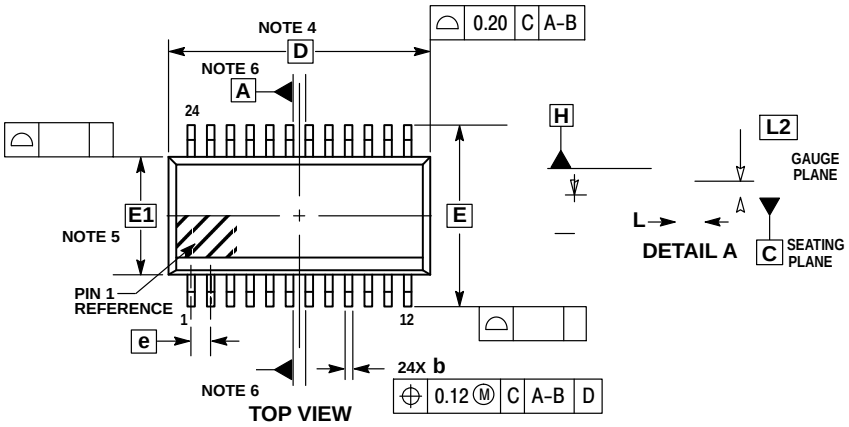
Device	Package	Shipping†
NCV7725DQBR2G	SSOP24 NB EP (Pb−Free)	2500 / Tape & Reel

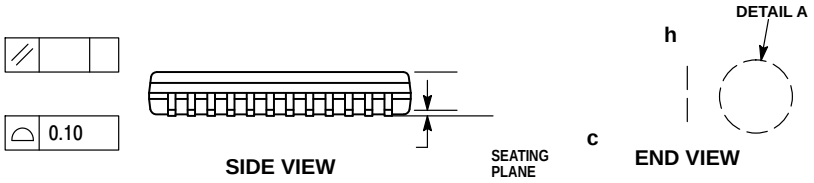
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

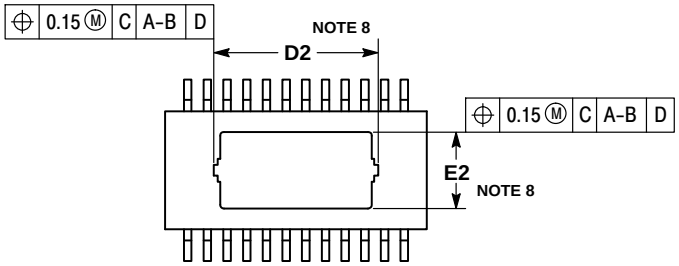
SSOP24 NB EP
CASE 940AK
ISSUE O

SCALE 1:1

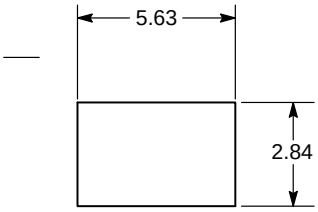
DATE 24 APR 2012







SOLDERING FOOTPRINT



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.10 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. DIMENSION b APPLIES TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D IS DETERMINED AT DATUM PLANE H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM PLANE H.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. CONTOURS OF THE THERMAL PAD ARE UNCONTROLLED WITHIN THE REGION DEFINED BY DIMENSIONS D2 AND E2.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.70
A1	0.00	0.10
b	0.19	0.30
c	0.09	0.20

D2	5.28	5.58

E1	3.90 BSC	
E2	2.44	2.64
e	0.65 BSC	
h	0.25	0.50
L	0.40	0.85
L1	1.00 REF	
L2	0.25 BSC	
M	0°	8°