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Figure 2. Block Diagram

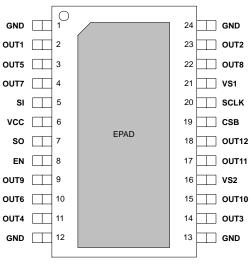


Figure 3. Pinout – SSOP24 NB EP

PIN FUNCTION DESCRIPTION The pin-out for the Half-Bridge Driver in SSOP24 NB EP package is shown in the table below.

Pin# SSOP24	Symbol	Description
1	GND	Ground. Must be connected to other GNDs externally.
2	OUT1	Half-bridge output 1
3	OUT5	Half-bridge output 5
4	OUT7	Half-bridge output 7
5	SI	16 bit serial communication input. 3.3V/5V (TTL) Compatible – internally pulled down.
6	VCC	Power supply input for Logic.
7	SO	16 bit serial communication output. 3.3V/5V Compliant
8	EN	Enable – active high; wakes the device from sleep mode. 3.3V/5V (TTL) Compatible – internally pulled down.
9	OUT9	Half-bridge output 9
10	OUT6	Half-bridge output 6
11	OUT4	Half-bridge output 4
12	GND	Ground. Must be connected to other GNDs externally.
13	GND	Ground. Must be connected to other GNDs externally.
14	OUT3	Half-bridge output 3
15	OUT10	Half-bridge output 10
16	VS2	Power Supply input for outputs 3, 4, 6, 9, 10, 11 and 12. This pin must be connected to VS1 externally.
17	OUT11	Half-bridge output 11
18	OUT12	Half-bridge output 12
19	CSB	Chip select bar – active low; enables serial communication operation. 3.3V/5V (TTL) Compatible – in- ternally pulled up.
20	SCLK	Serial communication clock input. 3.3V/5V (TTL) Compatible – internally pulled down.
21	VS1	Power Supply input for outputs 1, 2, 5, 7, 8. This pin must be connected to VS2 externally.
22	OUT8	Half-bridge output 8
23	OUT2	Half-bridge output 2
24	GND	Ground. Must be connected to other GNDs externally.
EPAD	Exposed Pad	Connect to GND or leave unconnected.

MAXIMUM RATINGS (Voltages are with respect to GND)

	Rating	Symbol	Value	Unit
VSx Pin Voltage	(VS1, VS2) (DC) (AC), t < 500 ms, lvsx > -2 A	VSxdcMax VSxac	-0.3 to 40 -1.0	V
I/O Pin Voltage	(Vcc, SI, SCLK, CSB, SO, EN)	VioMax	-0.3 to 5.5	V
OUTx Pin Voltage	(DC) (AC) (AC), t< 500 ms, IOUTx > -1.1 A (AC), t< 500 ms, IOUTx < 1 A	VoutxDc VoutxAc	-0.3 to 40 -0.3 to 40 -1.0 1.0	V
OUTx Pin Current	(OUT1,, OUT12)	loutxImax	-2.0 to 2.0	A
Junction Temperate	ure Range	TJ	-40 to 150	°C
Storage Temperature Range		Tstr	-55 to 150	°C
Peak Reflow Solde	ring Temperature: Pb-free 60 to 150 seconds at 217 $^\circ C$	(Note 1)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. 1. See or download **onsemi**'s Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ELECTRICAL CHARACTERISTICS

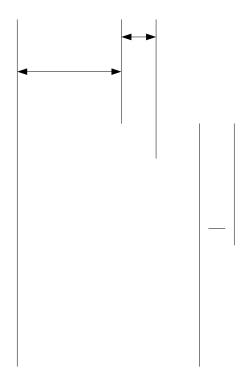
(-40 °C \leq T_J \leq 150 °C, 5.5 V \leq VSx \leq 40 V, 3.15 V \leq V_{CC} \leq 5.25 V, EN = V_{CC}

ELECTRICAL CHARACTERISTICS (continued) (-40 $^{\circ}C \leq T_J$

 $\begin{array}{l} \textbf{ELECTRICAL CHARACTERISTICS} (\text{continued}) \\ (-40 \ ^{\circ}\text{C} \leq \text{T}_{J} \leq 150 \ ^{\circ}\text{C}, \ 5.5 \ \text{V} \leq \text{VSx} \leq 40 \ \text{V}, \ 3.15 \ \text{V} \leq \text{V}_{CC} \leq 5.25 \ \text{V}, \ \text{EN} = \text{V}_{CC}, \ \text{unless otherwise specified.}) \end{array}$

Characteristic	Symbol	Conditions	Timing Charts #	Min	Тур	Мах	Uni
SERIAL PERIPHERAL INTERFACE		•	•		•		
SCLK Frequency							
SCLK Clock Period							
SCLK High Time	TclkH		1	85	-	-	ns
SCLK Low Time	TclkL		2	85	-	-	ns
SCLK Setup Time	TclkSup		3, 4	85	-	-	ns
SI Setup Time	TsiSup		11	50	-	-	ns
SI Hold Time	TsiH		12	50	-	-	ns
CSB Setup Time	TcsbSup		5, 6	100	-	-	ns
CSB High Time	TcsbH	(Note 4)	7	5.0	-	-	μs
SO enable after CSB falling edge	TenSo		8	-	-	200	ns
SO disable after CSB rising edge	TdisSo		9	-	-	200	ns

CHARACTERISTIC TIMING DIAGRAMS



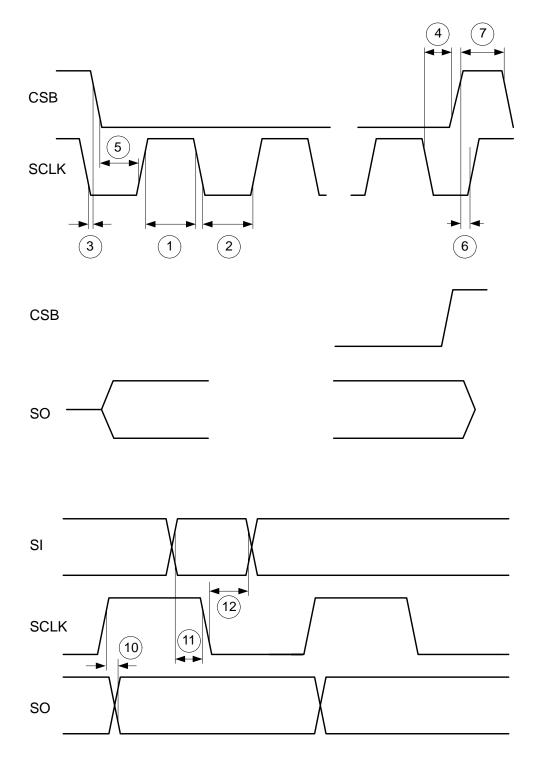


Table 1. SPI COMMAND INPUT DEFINITIONS

Channels 12 – 7 (Input Bit # 14 = 1)						
Bit#	Name	Function	Status*	Scope		
15	SRR	Status Register Reset**	1 = Reset	Status Reset per HBSEL		
14	HBSEL	Channel Group Select	1 = HB [12:7]	1 = HB [12:7] 0 = HB [6:1]		
13	ULDSC					

Table 2. SPI STATUS OUTPUT DEFINITIONS

Channels 12 – 7 (If Previous Input Bit # 14 = 1)						
Name Function Status*		Status*	Scope			
TSD	15 TSD Latched Thermal Shutdown	1 = Fault	Global Notification; Per Half-Bridge Operation			
OCS	OCS Latched Overcurrent Shutdown	1 = Fault	Notification per HBSEL ; Per Half-Bridge Operation			
PSF	PSF VS1 and/or VS2 Undervoltage or Overvoltage	1 = Fault	Global Notification and Global Operation			
ULD	ULD Underload Detect	1 = Fault	Notification per HBSEL ; Per Half-Bridge Operation			
HBST12	HBST12 Half-Bridge 12 Output Status					
HBST11	HBST11					
		0 = Hi–Z				
		1 = Enabled	Per Half-Bridge			
		I = Enableu				

Table 2. SPI STATUS OUTPUT DEFINITIONS (continued)

	Channels 6 – 1 (If Previous Input Bit # 14 = 0)						
Bit# Name Function Status* Scope							
PRE_15	TSD	Latched Thermal Shutdown	1 = Fault	Global Notification;			

 $\begin{array}{l} \mbox{CMD } [x,\,n] = \mbox{Command Word to Device `x', Length `n'} \\ \mbox{STA } [x,\,n] = \mbox{Status Word from Device `x', Length `n'} \\ \end{array}$

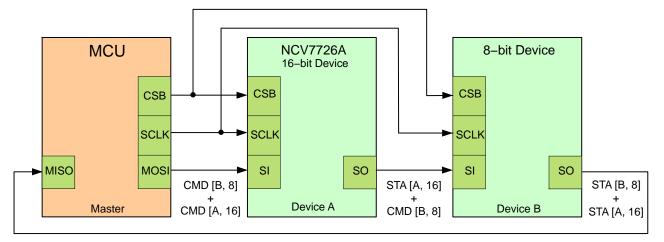
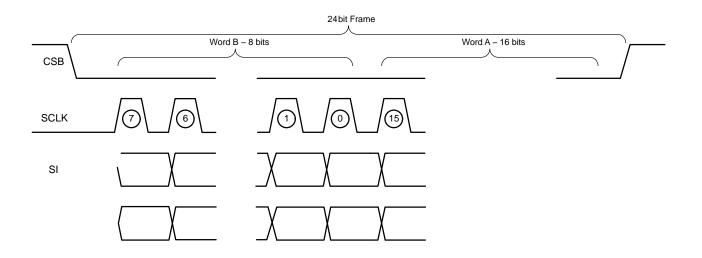


Figure 13. Daisy Chain Configuration



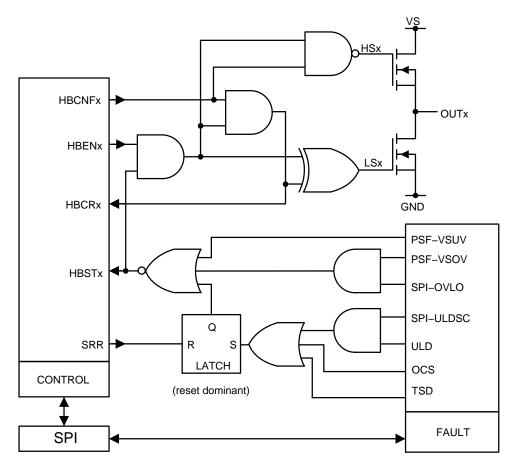


Figure 18. Simplified Half-Bridge Control Logic

Command		Sta		
HBENx	HBCNFx	HBSTx HBCRx		OUTx
X	•	•	•	

DIAGNOSTICS, PROTECTIONS, STATUS REPORTING AND RESET

Overview

The NCV7726A employs diagnostics designed to prevent destructive overstress during a fault condition. Diagnostics are classified as either supervisory or protection functions (Table 4). Supervisory functions provide status information about device conditions. Protection functions provide status information and activate fault management behaviors.

Diagnostics resulting in output shutdown and latched status may depend on a qualifier and may require user

intervention for output recovery and status memory clear. Diagnostics resulting in output lockout and non-latched status (VSOV or VSUV) may recover and clear automatically. Output configurations can be changed during output lockout. Outputs assume the new configurations or resume the previous configurations when an auto-recover fault is resolved. Table 5 shows output states during faults and output recovery modes, and Table 6 shows the status memory and memory clear modes.

Table 4. D	DIAGNOSTIC	CLASSES AND	FUNCTIONS
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Name	Class	Function
TSD	Protection	Thermal Shutdown
OCS	Protection	Overcurrent Shutdown
PSF	Protection	Under/overvoltage Lockout (OVLO = 1)
ULD	Protection	Underload Shutdown
HBSTX	Supervisory	Half-Bridge X Output Status
HBCRX	Supervisory	Half-Bridge X Config Status
TW	Supervisory	Thermal Warning

Table 5. OUTPUT STATE VS. FAULT AND OUTPUT RECOVERY

Fault	Qualifier	OUTx State	OUTx Recovery	OUTx Recovery Scope
TSD	-	→Z	Send SRR	Per HBSEL
OCS	-	→Z	Send SRR	Per HBSEL
PSF – VSOV	OVLO = 1	$\rightarrow Z \rightarrow Y_n \mid Y_{n+1}$	Auto*	All Outputs
	OVLO = 0	Unaffected	-	-
PSF – VSUV	-	$\rightarrow Z \rightarrow Y_n \mid Y_{n+1}$	Auto*	All Outputs
ULD	ULDSC = 1	→Z	Send SRR	Per HBSEL
	ULDSC = 0	Unaffected	-	-
TW	_	Unaffected	_	-

*OUTx returns to its previous state (Yn) or new state (Yn+1) if fault is removed.

Table 6. STATUS MEMORY VS. FAULT AND MEMORY CLEAR

Fault	Qualifier	Status Memory	Memory Clear	Memory Clear Scope
TSD	-	Latched	Send SRR	Per HBSEL
OCS	-	Latched	Send SRR	Per HBSEL
PSF – VSOV	OVLO = X	Non-Latched	Auto*	Global
PSF – VSUV	-	Non-Latched	Auto*	Global
ULD	ULDSC = X	Latched	Send SRR	Per HBSEL
TW	-	Non-Latched	Auto*	Global

*Status memory returns to its no-fault state if fault is removed.

Status Information Retrieval

Current status information as selected by HBSEL is retrieved during each SPI frame. To preserve device configuration and output states, the previous SI data pattern must be sent during the status retrieval frame.

Status information is prevented from being updated during a SPI frame but new status becomes available after CSB goes high at the end of the frame provided the frame did not contain an SRR request. For certain device faults, it may not be possible to determine which channel (or channels) has a particular fault (or faults) since notification may be via a single global status bit. The complete status data from all channels may need to be examined to determine where a fault may exist.

Status Register Reset SRR

Sending SRR = 1 clears status memory and re – activates faulted outputs for channels as selected by HBSEL. The previous SI data pattern must be sent with SRR to preserve device configuration and output states. SRR takes effect at the rising edge of CSB and a timer (Tsrr) is started. Tsrr is the minimum time the user must wait between consecutive SRR requests. If a fault is still present when SRR is sent, protection can be re – engaged and shutdown will recur. The status registers can also be reset by toggling the EN pin or by VCC power – on reset.

Diagnostics Details

The following sections describe individual diagnostics and behaviors. In each description and illustration, a SPI frame is assumed to always be valid and the SI data pattern sent for HBCNFx and HBENx is the same as the previous frame. Actual results can depend on asynchronous fault events and SPI clock frequency and frame rate.

Undervoltage Lockout

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Overvoltage Lockout

Global Notification, Global Operation

Overvoltage detection and lockout control is provided by monitoring the VS1 and VS2 supply inputs. Overvoltage hysteresis is provided to ensure clean detection transitions. Overvoltage timing is shown in Figure 20.

Overvoltage at either VSx input turns off all outputs if the overvoltage lockout input bit is set (OVLO = 1,

HBSEL = X), and sets the power supply fail (PSF) status bit (see Tables 5 and 6). The outputs return to their previously programmed state and the PSF status bit is cleared when VSx falls below the hysteresis voltage level.

To reduce stress, it is recommended to operate the device with OVLO bit asserted to ensure that the drivers turn off during a load dump scenario.

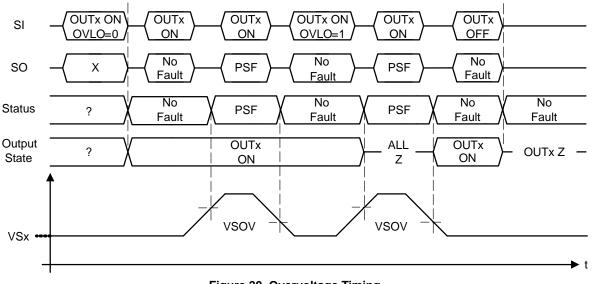


Figure 20. Overvoltage Timing

Overcurrent Shutdown

Global Notification per HBSEL, Per Half-Bridge Operation

Overcurrent detection and shutdown control is provided by monitoring each HS and LS driver. Overcurrent timing is shown in Figure 21. Overcurrent in either driver starts a channel's overcurrent delay timer. If overcurrent exists after the delay, both drivers are latched off and the overcurrent (OCS) status bit is set. The OCS bit is cleared and channels are re – activated by sending SRR = 1. The channel group select (HBSEL) input bit determines which channels are affected by SRR.

A persistent overcurrent cause should be resolved prior to re – activation to avoid repetitive stress on the drivers. Extended exposure to stress may affect device reliability.

Underload Shutdown

Global Notification per HBSEL, Shutdown Control per HBSEL, Per Half-Bridge Operation

Underload detection and shutdown control is provided by monitoring each LS driver. Underload timing is shown in Figure 22. Underload at a LS driver starts the global underload delay timer. If underload occurs in another channel after the global timer has been started, the delay for any subsequent underload will be the remainder of the timer. The timer runs continuously with a persistent underload condition.

If underload exists after the delay and if the underload shutdown (ULDSC) command bit is set, both HS and LS drivers are latched off and the underload (ULD) status bit is set; otherwise the drivers remain on and the ULD bit is set (see Tables 5 and 6). The ULD bit is cleared and channels are re – activated by sending SRR = 1. The channel group select (HBSEL) input bit determines which channels are affected by SRR and also determines which half – bridges are latched off via the ULDSC command bit (see Table 1).

Underload may result from a fault (e.g. open-

THERMAL PERFORMANCE ESTIMATES

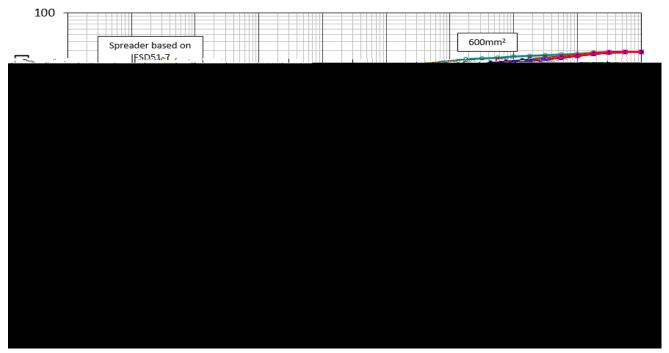
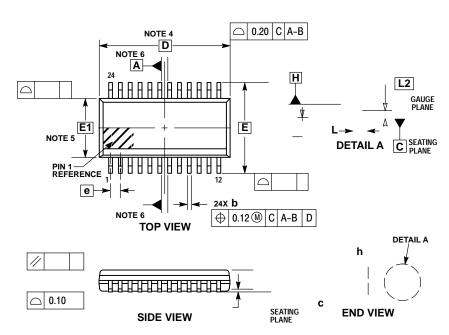
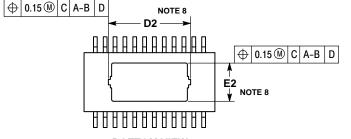


Figure 24. Transient R(t) vs. Pulse Time for 2 oz Spreader

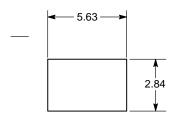






BOTTOM VIEW

SOLDERING FOOTPRINT



- NOTES:
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: MILLIMETERS. 3. DIMENSION b DOES NOT INCLUDE DAMBAR
- PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.10 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. DIMENSION 6 APPLIES TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
- FROM THE LEAD TIP.
 DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D IS DETERMINED AT DATUM PLANE H.
 DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR DROTBUISION SHALL NOT EXCEED 0.25 PER
- OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED AT DA-
- TUM PLANE H. 6. DATUMS A AND B ARE DETERMINED AT DATUM
- 7.
- DATUMS A AND B ARE DETERMINED AT DATE: PLANE H. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY. CONTOURS OF THE THERMAL PAD ARE UN-CONTROLLED WITHIN THE REGION DEFINED SY DIMENSIONS DO AND F2 8. BY DIMENSIONS D2 AND E2.

MILLIMETERS	
MIN	MAX
	1.70
0.00	0.10
0.19	0.30
0.09	0.20
	MIN 0.00 0.19

D2	5.28	5.58
E1	3.90	BSC
E2	2.44	2.64
е	0.65 BSC	
h	0.25	0.50
L	0.40	0.85
11	1.00 BEE	

0.25 BSC 0° 8 8

L2 M

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