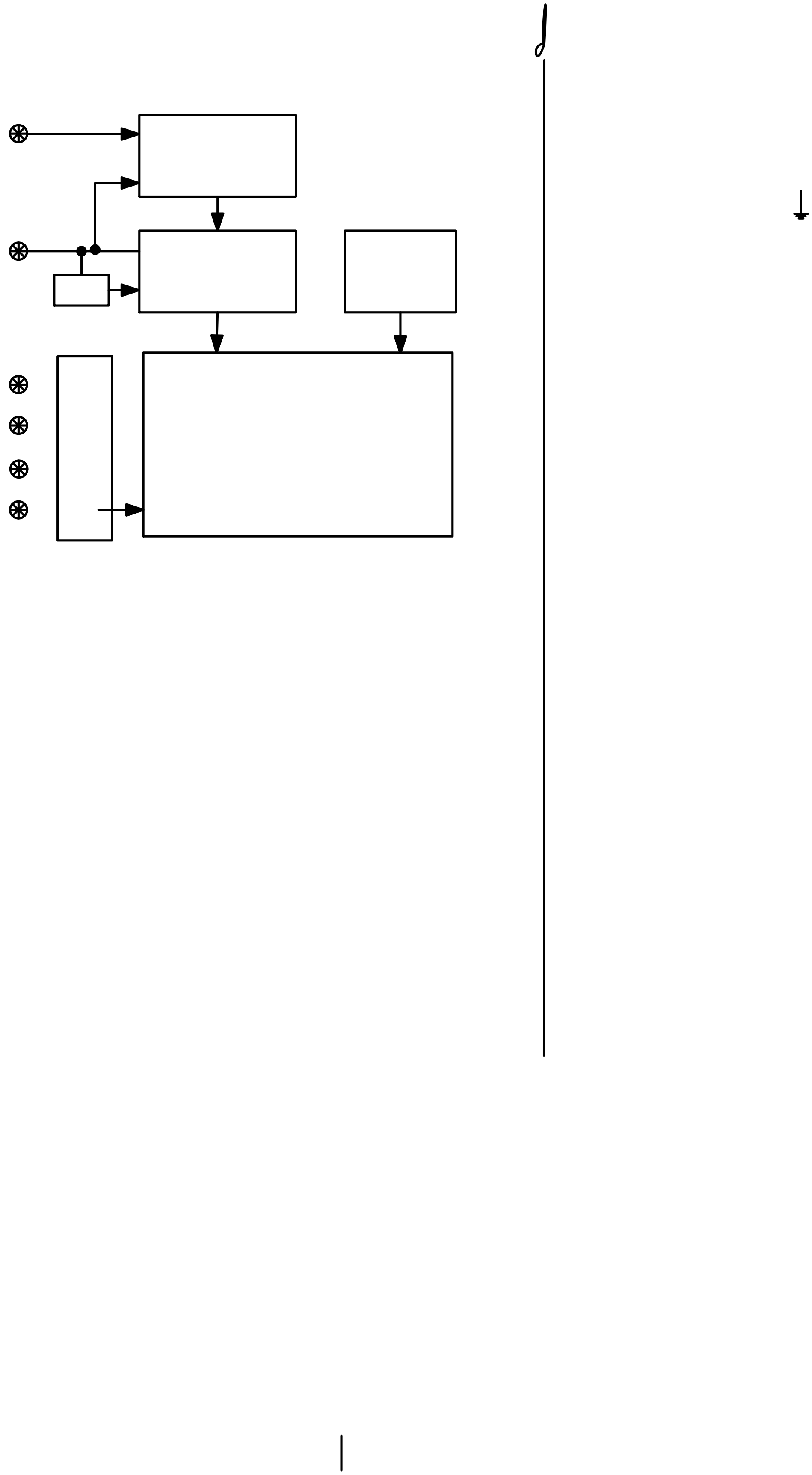


Figure 2. Block Diagram

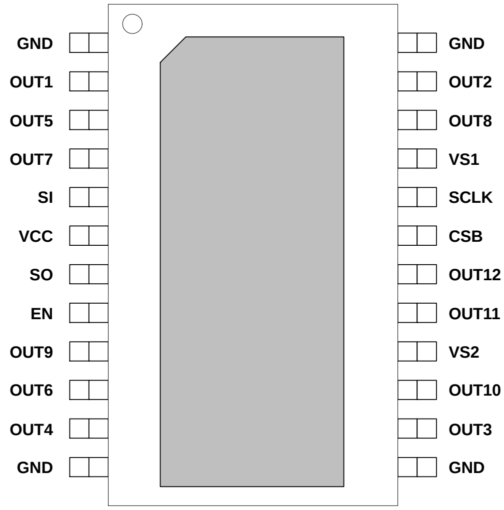


Figure 3. Pinout – SSOP24 NB EP

PIN FUNCTION DESCRIPTION

Pin# SSOP24	Symbol	Description
		–
		– –
		– –
		–

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
–		– –	
		–	
–		– – –	
		–	
		–	°
		–	°
°			°

onsemi

ELECTRICAL CHARACTERISTICS

− ° ≤ ≤ ° ≤ ≤ ≤ ≤

ELECTRICAL CHARACTERISTICS

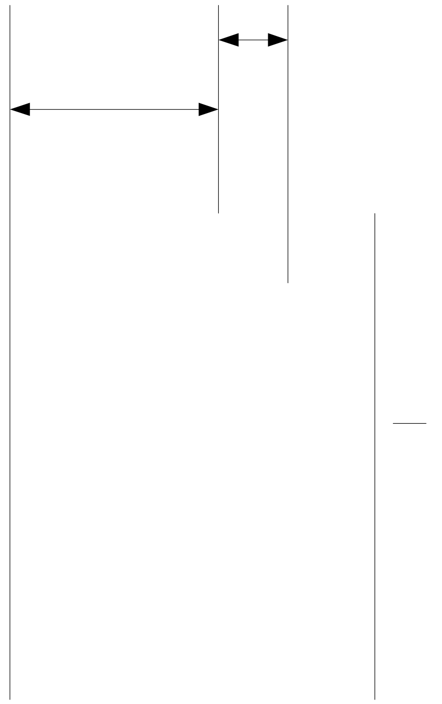
− ° ≤ °

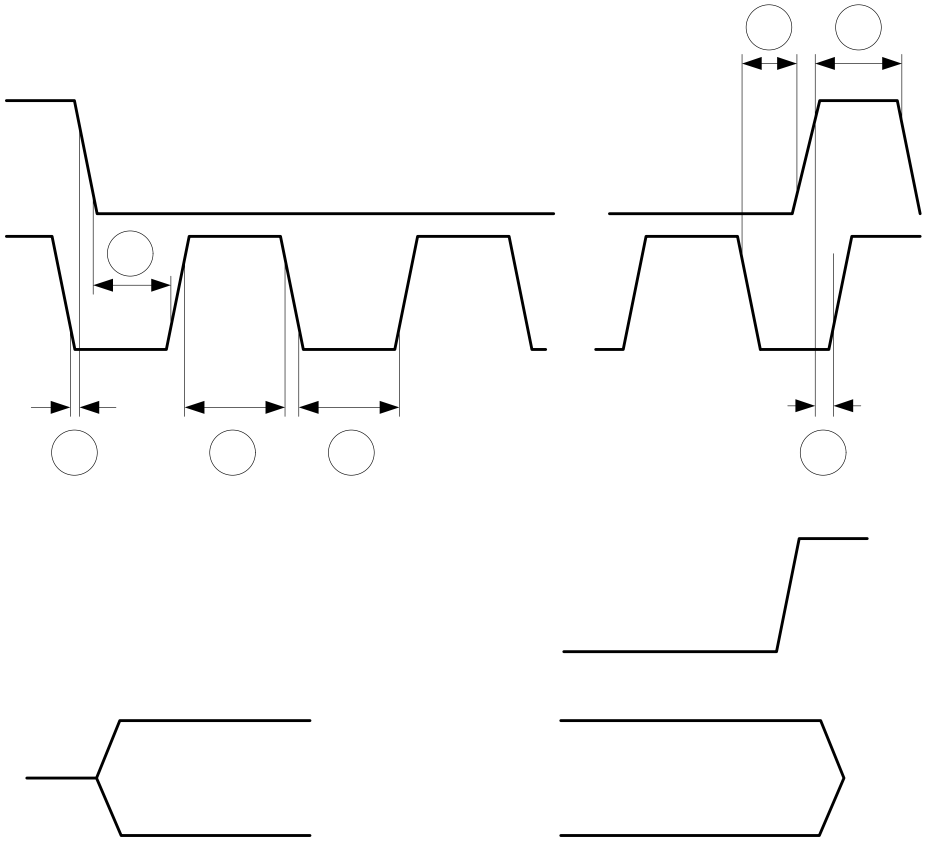
ELECTRICAL CHARACTERISTICS

− ° ≤ ≤ ° ≤ ≤ ≤ ≤

Characteristic	Symbol	Conditions	Timing Charts #	Min	Typ	Max	Unit
SERIAL PERIPHERAL INTERFACE							
			−	−	−		
			−		− −	− −	
					−	−	
					−	−	
					−	−	
					−	−	
					−	−	
					−	−	
					−	−	μ
				−	−		
				−	−		

CHARACTERISTIC TIMING DIAGRAMS





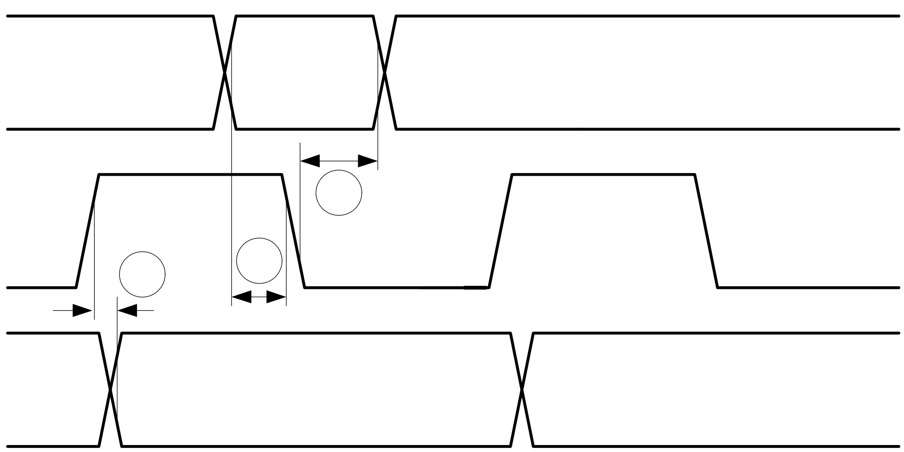


Table 1. SPI COMMAND INPUT DEFINITIONS

Channels 12 – 7 (Input Bit # 14 = 1)				
Bit#	Name	Function	Status*	Scope
				HBSEL
	HBSEL		1 = HB [12:7]	

Table 2. SPI STATUS OUTPUT DEFINITIONS

Channels 12 – 7 (If Previous Input Bit # 14 = 1)				
Bit#	**Name**	**Function**	**Status***	**Scope**
				HBSEL
				HBSEL
			–	

Table 2. SPI STATUS OUTPUT DEFINITIONS

Channels 6 – 1 (If Previous Input Bit # 14 = 0)				
Bit#	**Name**	**Function**	**Status***	**Scope**

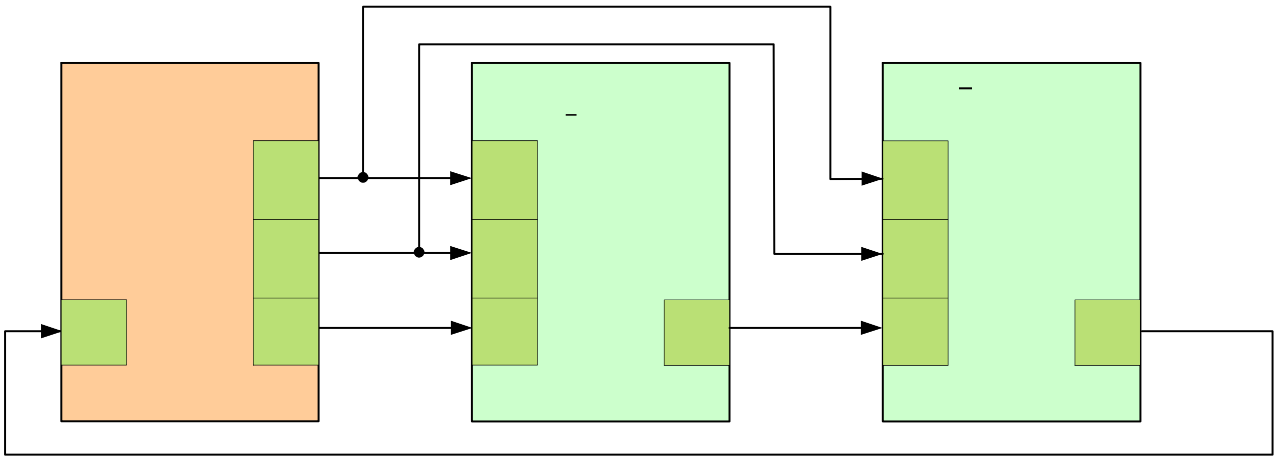
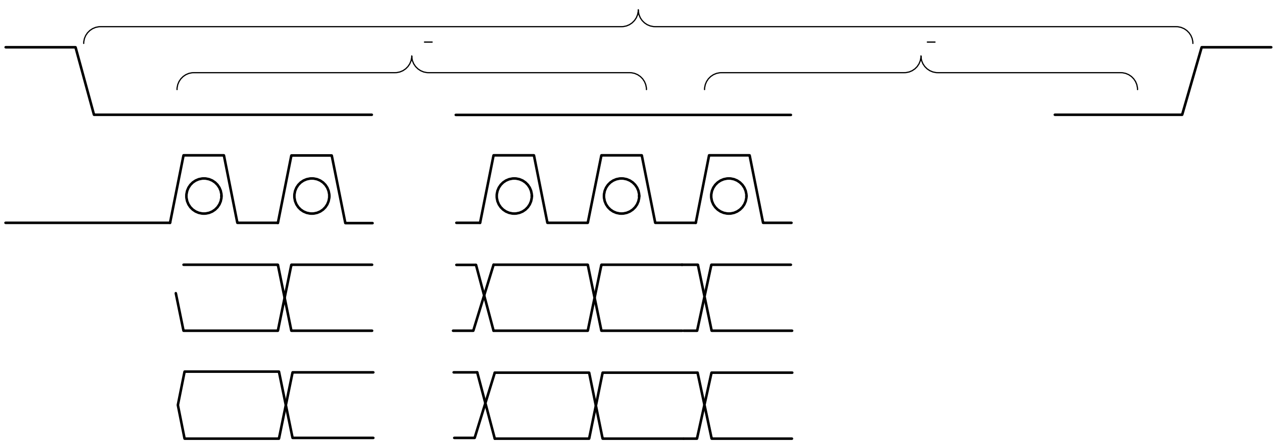


Figure 13. Daisy Chain Configuration



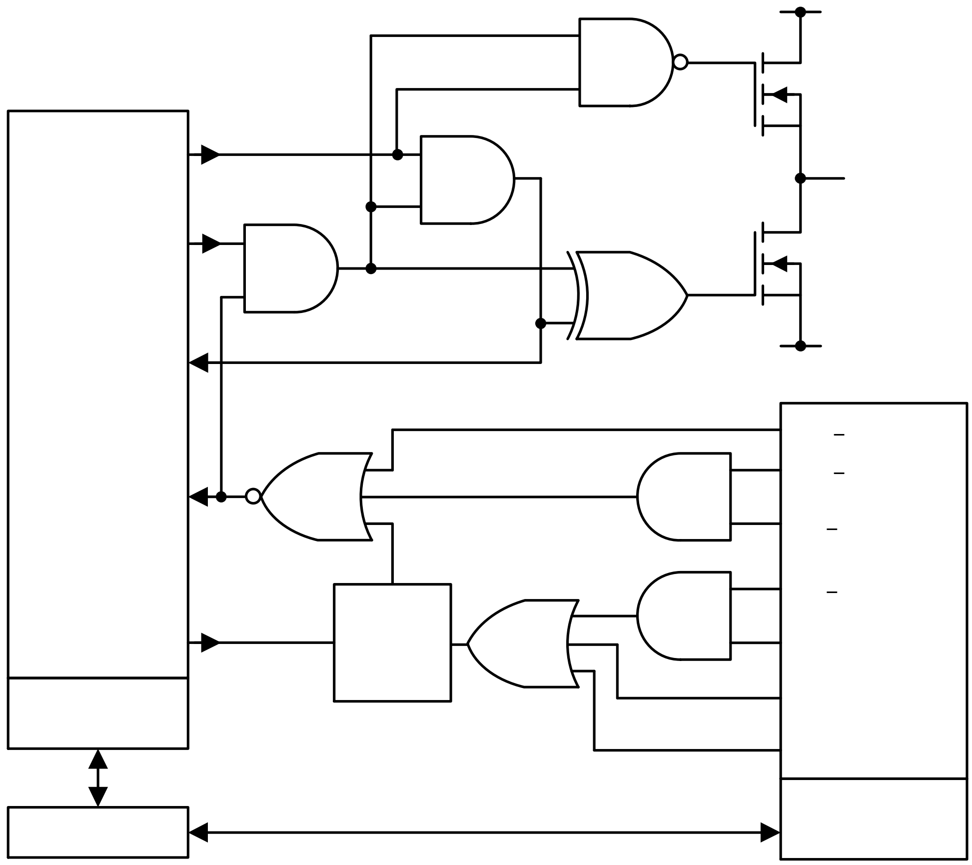


Figure 18. Simplified Half-Bridge Control Logic

Table 3. OUTPUT STATE VS. COMMAND AND STATUS

Command		Status		
HBENx	HBCNFx	HBSTx	HBCRx	OUTx

DIAGNOSTICS, PROTECTIONS, STATUS REPORTING AND RESET

Overview

The NCV7726A employs diagnostics designed to prevent destructive overstress during a fault condition. Diagnostics are classified as either supervisory or protection functions (Table 4). Supervisory functions provide status information about device conditions. Protection functions provide status information and activate fault management behaviors.

Diagnostics resulting in output shutdown and latched status may depend on a qualifier and may require user intervention for output recovery and status memory clear. Diagnostics resulting in output lockout and non-latched status (VSOV or VSUV) may recover and clear automatically. Output configurations can be changed during output lockout. Outputs assume the new configurations or resume the previous configurations when an auto-recover fault is resolved. Table 5 shows output states during faults and output recovery modes, and Table 6 shows the status memory and memory clear modes.

Table 4. DIAGNOSTIC CLASSES AND FUNCTIONS

Name	Class	Function

Table 5. OUTPUT STATE VS. FAULT AND OUTPUT RECOVERY

Fault	Qualifier	OUTx State	OUTx Recovery	OUTx Recovery Scope
	–	→		
	–	→		
		→ →		
			–	–
	–	→ →		
		→		
			–	–
	–		–	–

Table 6. STATUS MEMORY VS. FAULT AND MEMORY CLEAR

Fault	Qualifier	Status Memory	Memory Clear	Memory Clear Scope
	–			
	–			
	–			
	–			

Status Information Retrieval

Current status information as selected by HBSEL is retrieved during each SPI frame. To preserve device configuration and output states, the previous SI data pattern must be sent during the status retrieval frame.

Status information is prevented from being updated during a SPI frame but new status becomes available after CSB goes high at the end of the frame provided the frame did not contain an SRR request. For certain device faults, it may not be possible to determine which channel (or channels) has a particular fault (or faults) since notification may be via a single global status bit. The complete status data from all channels may need to be examined to determine where a fault may exist.

Status Register Reset SRR

Sending SRR = 1 clears status memory and re−activates faulted outputs for channels as selected by HBSEL. The previous SI data pattern must be sent with SRR to preserve device configuration and output states. SRR takes effect at the rising edge of CSB and a timer (Tsrr) is started. Tsrr is the minimum time the user must wait between consecutive SRR requests. If a fault is still present when SRR is sent, protection can be re−engaged and shutdown will recur. The status registers can also be reset by toggling the EN pin or by VCC power−on reset.

Diagnostics Details

The following sections describe individual diagnostics and behaviors. In each description and illustration, a SPI frame is assumed to always be valid and the SI data pattern sent for HBCNFx and HBENx is the same as the previous frame. Actual results can depend on asynchronous fault events and SPI clock frequency and frame rate.

Undervoltage Lockout

Overvoltage Lockout

Overvoltage detection and lockout control is provided by monitoring the VS1 and VS2 supply inputs. Overvoltage hysteresis is provided to ensure clean detection transitions. Overvoltage timing is shown in Figure 20.

Overvoltage at either VSx input turns off all outputs if the overvoltage lockout input bit is set (OVLO = 1, HBSEL = X), and sets the power supply fail (PSF) status bit (see Tables 5 and 6). The outputs return to their previously programmed state and the PSF status bit is cleared when VSx falls below the hysteresis voltage level.

To reduce stress, it is recommended to operate the device with OVLO bit asserted to ensure that the drivers turn off during a load dump scenario.

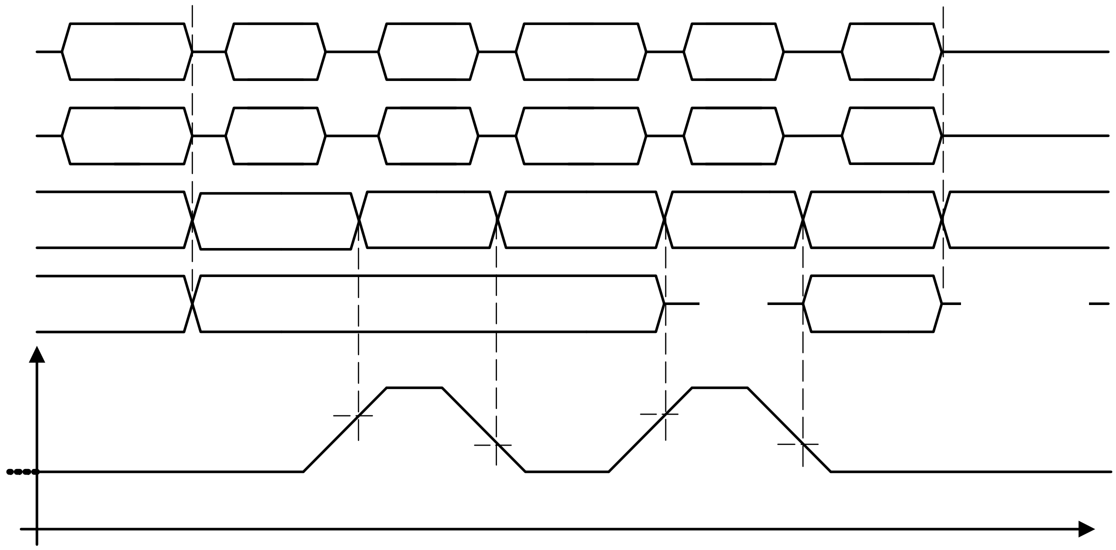


Figure 20. Overvoltage Timing

Overcurrent Shutdown

Overcurrent detection and shutdown control is provided by monitoring each HS and LS driver. Overcurrent timing is shown in Figure 21. Overcurrent in either driver starts a channel's overcurrent delay timer. If overcurrent exists after the delay, both drivers are latched off and the overcurrent (OCS) status bit is set. The OCS bit is cleared and channels are re–activated by sending SRR = 1. The channel group select (HBSEL) input bit determines which channels are affected by SRR.

A persistent overcurrent cause should be resolved prior to re–activation to avoid repetitive stress on the drivers. Extended exposure to stress may affect device reliability.

Underload Shutdown

Underload detection and shutdown control is provided by monitoring each LS driver. Underload timing is shown in Figure 22. Underload at a LS driver starts the global underload delay timer. If underload occurs in another channel after the global timer has been started, the delay for any subsequent underload will be the remainder of the timer. The timer runs continuously with a persistent underload condition.

If underload exists after the delay and if the underload shutdown (ULDSC) command bit is set, both HS and LS drivers are latched off and the underload (ULD) status bit is set; otherwise the drivers remain on and the ULD bit is set (see Tables 5 and 6). The ULD bit is cleared and channels are re−activated by sending SRR = 1. The channel group select (HBSEL) input bit determines which channels are affected by SRR and also determines which half−bridges are latched off via the ULDSC command bit (see Table 1).

Underload may result from a fault (e.g. open−

THERMAL PERFORMANCE ESTIMATES

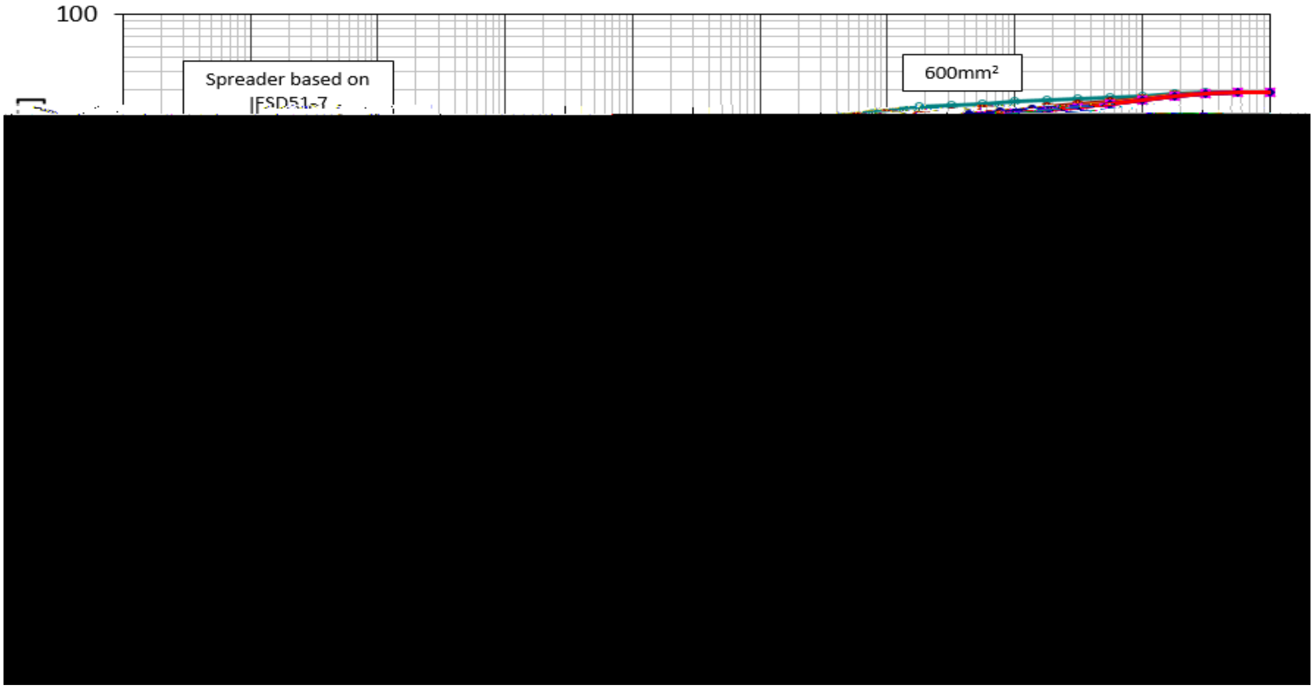


Figure 24. Transient R(t) vs. Pulse Time for 2 oz Spreader

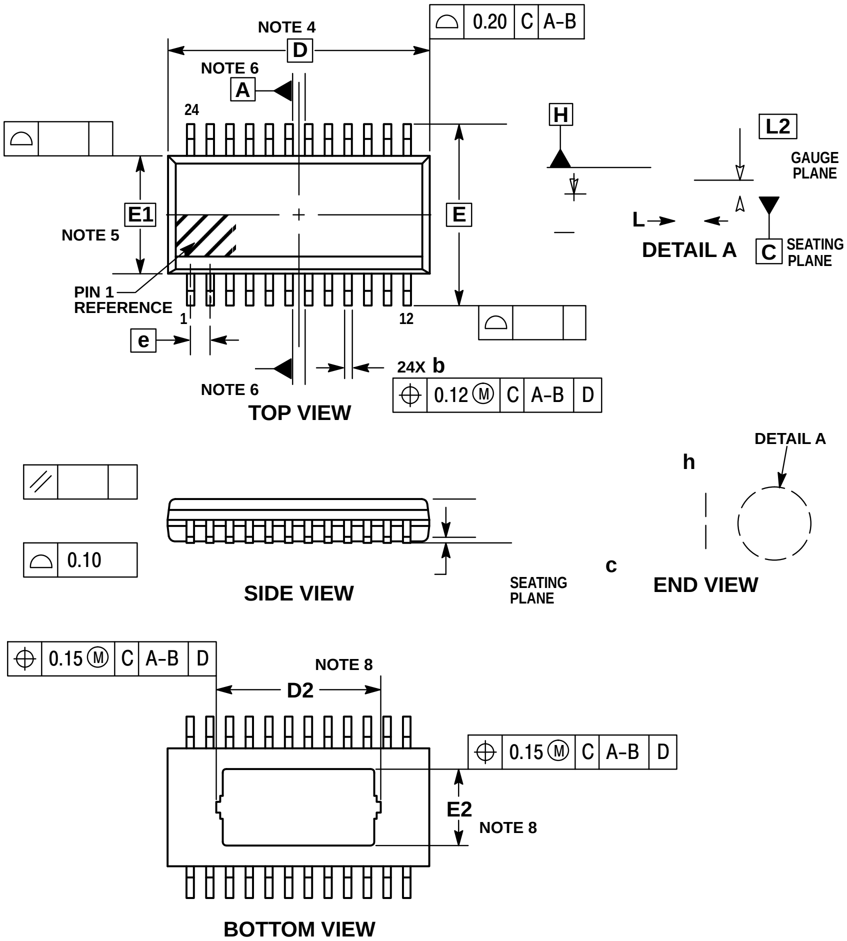
SCALE 1:1

SSOP24 NB EP

CASE 940AK

ISSUE O

DATE 24 APR 2012



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.10 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. DIMENSION b APPLIES TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D IS DETERMINED AT DATUM PLANE H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM PLANE H.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. CONTOURS OF THE THERMAL PAD ARE UNCONTROLLED WITHIN THE REGION DEFINED BY DIMENSIONS D2 AND E2.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.70
A1	0.00	0.10
b	0.19	0.30
c	0.09	0.20
D2	5.28	5.58
E1	3.90 BSC	
E2	2.44	2.64
e	0.65 BSC	
h	0.25	0.50
L	0.40	0.85
L1	1.00 REF	
L2	0.25 BSC	
M	0°	8°

SOLDERING FOOTPRINT