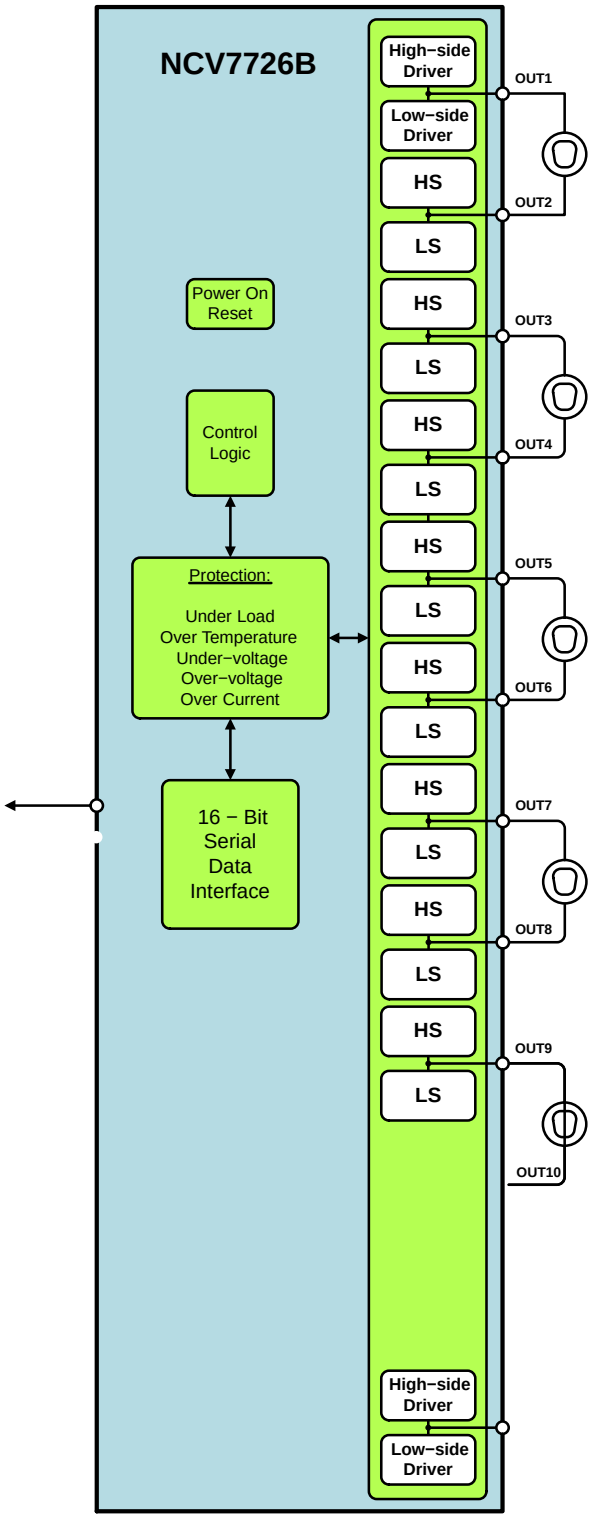


Figure 1. Typical Application

MAXIMUM RATINGS (Voltages are with respect to GND)

Symbol	Rating	Value	Unit
VSxdcMax VSxac	VSx Pin Voltage (VS1, VS2) (DC) (AC), t < 500 ms, Ivsx > −2 A	 −0.3 to 40 −1.0	V
VioMax	I/O Pin Voltage (Vcc, SI, SCLK, CSB, SO, EN)	−0.3 to 5.5	V
VoutxDc VoutxAc	OUTx Pin Voltage (DC) (AC) (AC), t< 500 ms, IOUTx > −1.1 A (AC), t< 500 ms, IOUTx < 1 A	 −0.3 to 40 −0.3 to 40 −1.0 1.0	V
IoutxImax	OUTx Pin Current (OUT1, ..., OUT12)	−2.0 to 2.0	A
T_J	Junction Temperature Range	−40 to 150	C
Tstr	Storage Temperature Range	−55 to 150	C
(Note 1)	Peak Reflow Soldering Temperature: Pb−free 60 to 150 seconds at 217 C	260	C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. See or download **onsemi**'s Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ATTRIBUTES

Symbol	Characteristic		Value	Unit
AECQ10x	Short Circuit Reliability Characterization		Grade A	−
Vesd4k Vesd2k Vesd750	ESD Capability Human Body Model per AEC−Q100−002 All Other Pins Charged Device Model per AEC−Q100−011	VSx, OUTx	 4.0 kV 2.0 kV 750 V	
MSL	Moisture Sensitivity Level		MSL2	−
$R_{\theta JA}$ $R_{\Psi JBOARD}$	Package Thermal Resistance – Still−air Junction–to–Ambient Junction–to–Board (Note 2)	(Note 2)	 29.4 10.5	 C/W C/W

2. Based on JESD51−7, 1.6 mm thick FR4, 2S2P PCB with 600 mm^2 2 oz. copper and 18 thermal vias to 80x80 mm 1 oz. internal spreader planes. Simulated with each channel dissipating 0.2 W.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
VCCOp	Digital Supply Input Voltage	3.15	5.25	V
VSxOp	Battery Supply Input Voltage (VS1 = VS2)	5.5	32	V
IxOp	DC Output Current	−	0.5	A
TjOp	Junction Temperature	−40	125	C

ELECTRICAL CHARACTERISTICS

(−40 C T$_J$ 150 C, 5.5 V VSx 40 V, 3.15 V V$_{CC}$ 5.25 V, EN = V$_{CC}$, unless otherwise specified.)

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
POWER SUPPLIES						
IqVSx85	Supply Current (VS1 + VS2) Sleep Mode	VS1 = VS2 = 13.2V, V$_{CC}$ = 0 V −40 C to 85 C	−	1.0	2.5	μA
IvsOp	Supply Current (VS1 + VS2) Active Mode	EN = V$_{CC}$, 5.5V < VSx < 28 V No Load, All Outputs Off	−	2.5	5.0	mA
IqV$_{CC}$	Supply Current (Vcc) Sleep Mode	CSB = V$_{CC}$, EN = SI = SCLK = 0 V −40 C to 85 C	−	1.0	2.5	μA
IV$_{CC}$Op	Active Mode	EN = CSB = V$_{CC}$, SI = SCLK = 0 V All Outputs Off	−	1.5	3.0	mA
IqTot	Total Sleep Mode Current I(VS1) + I(VS2) + I(VCC)	Sleep Mode, −40 C to 85 C VS1 = VS2 = 13.2 V, No Load	−	2.0	5.0	μA
V$_{CC}$por	VCC Power−on Reset Threshold	V$_{CC}$ increasing	−	2.70	2.90	V
VSxuv	VSx Undervoltage Detection Threshold	VSx decreasing	3.5	4.1	4.5	V
VSxuHys	VSx Undervoltage Detection Hysteresis		100	−	450	mV
VsXov	VSx Overvoltage Detection Threshold	VSx increasing	32	36	40	V
VSxoHys	VSx Overvoltage Detection Hysteresis		1	2.5	4	V
DRIVER OUTPUT CHARACTERISTICS						
R$_{DSon}$HS	Output High R$_{DS(on)}$ (source)					

ELECTRICAL CHARACTERISTICS (continued)
(−40 C T_J 150 C, 5.5 V VSx 40 V, 3.15 V V_{CC} 5.25 V, EN = V_{CC}, unless otherwise specified.)

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
DRIVER OUTPUT SWITCHING CHARACTERISTICS						
ThsTr	High Side Rise Time	Vs = 13.2 V, R_{load} = 70 Ω	−	4.0	8.0	μs
ThsTf	High Side Fall Time	Vs = 13.2 V, R_{load} = 70 Ω	−	2.0		

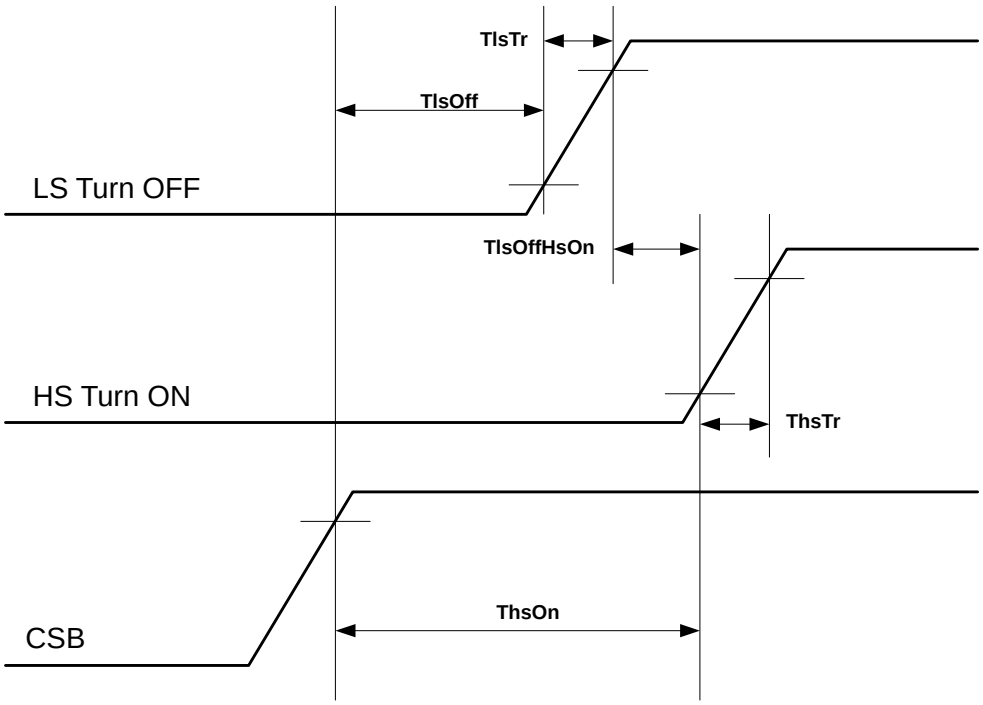
ELECTRICAL CHARACTERISTICS (continued)
(−40 C T_J 150 C, 5.5 V VSx 40 V, 3.15 V V_{CC} 5.25 V, EN = V_{CC}, unless otherwise specified.)

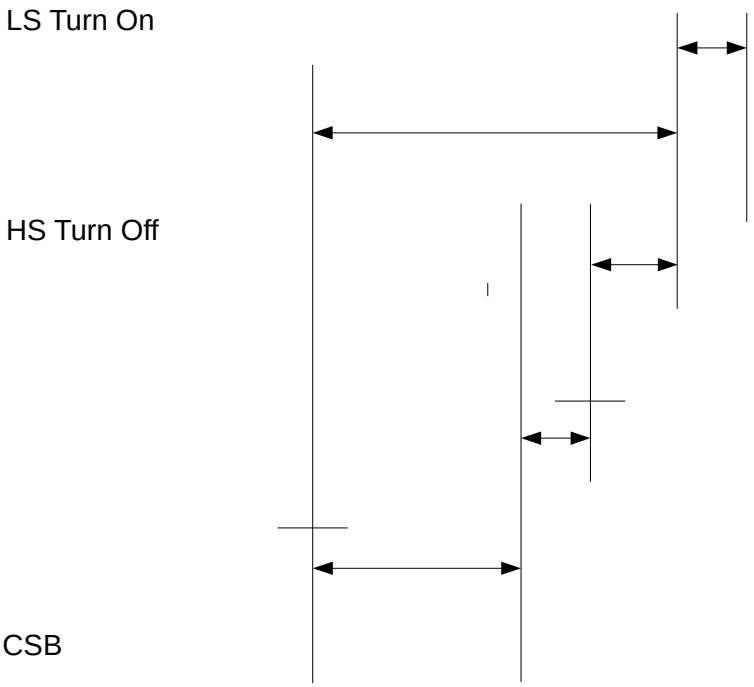
Symbol	Characteristic	Conditions	Timing Charts #	Min	Typ	Max	Unit
SERIAL PERIPHERAL INTERFACE							
Fclk	SCLK Frequency		−	−	−	5.0	MHz
TpClk	SCLK Clock Period	V_{CC} = 5 V V_{CC} = 3.3 V	−	200 500	− −	− −	ns
TclkH	SCLK High Time		1	85	−	−	ns
TclkL	SCLK Low Time		2	85	−	−	ns
TclkSup	SCLK Setup Time		3, 4	85	−	−	ns
TsiSup	SI Setup Time		11	50	−	−	ns
TsiH	SI Hold Time		12	50	−	−	ns
TcsbSup	CSB Setup Time		5, 6	100	−	−	ns
TcsbH	CSB High Time	(Note 4)	7	5.0	−	−	µs
TenSo	SO enable after CSB falling edge		8	−	−	200	ns
TdisSo	SO disable after CSB rising edge		9	−	−	200	ns
TsoR/F	SO Rise/Fall Time	Cload = 40 pF (Note 3)	−	−	10	25	ns
TsoV	SO Valid Time	Cload = 40 pF (Note 3) SCLK to SO 50%	10	−	50	100	ns
TenL	EN Low Valid Time	V_{CC} = 5V; EN H L 50% to OUTx turning off 50%	−	10	−	−	µs
TenHspiV	EN High to SPI Valid		−	−	−	100	µs
Tsrr	SRR Delay Between Consecutive Frames	(Note 5)	−	150	−	−	µs

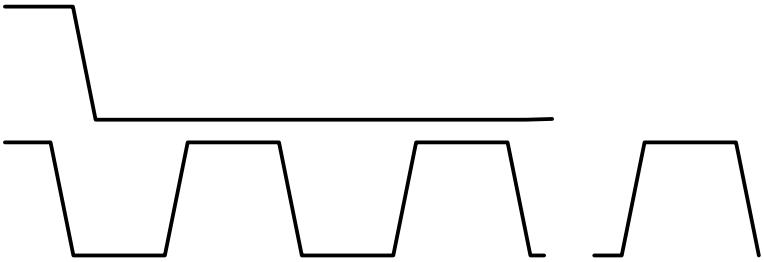
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

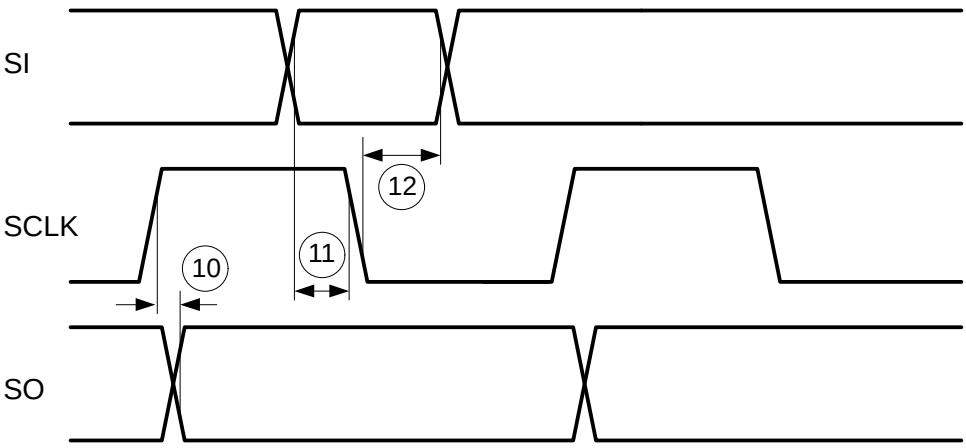
3. Not production tested.
4. This is the minimum time the user must wait between SPI commands.
5. This is the minimum time the user must wait between consecutive SRR requests.

CHARACTERISTIC TIMING DIAGRAMS








SI
SCLK
SO
10
11
12

TYPICAL CHARACTERISTICS

TEMPERATURE (C)

Figure 6. IqTot vs. Temperature

V_{CC}

Figure 7. I(V_{CC}) Active Mode vs. V(V_{CC})

DETAILED OPERATING DESCRIPTION

General Overview

The NCV7726B is comprised of twenty four NMOS power drivers. The drivers are arranged as twelve half−bridge output channels, allowing for six independent full−bridge configured loads. Output control and status reporting is handled via the SPI (Serial Peripheral Interface) communications port.

Each output is characterized for a typical 0.5 A DC load

Table 1. SPI COMMAND INPUT DEFINITIONS

Channels 12 – 7 (Input Bit # 14 = 1)				
Bit#	**Name**	**Function**	**Status***	**Scope**
15	SRR	Status Register Reset**	1 = Reset	Status Reset per **HBSEL**
14	**HBSEL**	Channel Group Select	**1 = HB [12:7]**	1 = HB [12:7] | 0 = HB [6:1]
13	ULDSC	Underload Shutdown Control	1 = Enabled	Enabled per **HBSEL**; Per Half−Bridge Operation
12	HBEN12	Enable Half−Bridge 12	0 = Hi−Z 1 = Enabled	Per Half−Bridge
11	HBEN11	Enable Half−Bridge 11		
10	HBEN10	Enable Half−Bridge 10		
9	HBEN9	Enable Half−Bridge 9		
8	HBEN8	Enable Half−Bridge 8		
7	HBEN7	Enable Half−Bridge 7		
6	HBCNF12	Configure Half−Bridge 12	0 = LS On, HS Off 1 = LS Off, HS On	Per Half−Bridge
5	HBCNF11	Configure Half−Bridge 11		
4	HBCNF10	Configure Half−Bridge 10		
3	HBCNF9	Configure Half−Bridge 9		
2	HBCNF8	Configure Half−Bridge 8		
1	HBCNF7	Configure Half−Bridge 7		
0	OVLO	VSx Overvoltage Lockout	1 = Enabled	Global Lockout
Channels 6 – 1 (Input Bit # 14 = 0)				
Bit#	**Name**	**Function**	**Status***	**Scope**
15	SRR	Status Register Reset**	1 = Reset	Status Reset per **HBSEL**
14	**HBSEL**	Channel Group Select	**0 = HB [6:1]**	1 = HB [12:7] | 0 = HB [6:1]
13	ULDSC	Underload Shutdown Control	1 = Enabled	Enabled per **HBSEL**; Per Half−Bridge Operation
12	HBEN6	Enable Half−Bridge 6	0 = Hi−Z 1 = Enabled	Per Half−Bridge
11	HBEN5	Enable Half−Bridge 5		
10	HBEN4	Enable Half−Bridge 4		
9	HBEN3	Enable Half−Bridge 3		
8	HBEN2	Enable Half−Bridge 2		
7	HBEN1	Enable Half−Bridge 1		
6	HBCNF6	Configure Half−Bridge 6	0 = LS On, HS Off 1 = LS Off, HS On	Per Half−Bridge
5	HBCNF5	Configure Half−Bridge 5		
4	HBCNF4	Configure Half−Bridge 4		
3	HBCNF3	Configure Half−Bridge 3		
2	HBCNF2	Configure Half−Bridge 2		
1	HBCNF1	Configure Half−Bridge 1		
0	OVLO	VSx Overvoltage Lockout	1 = Enabled0	= H i

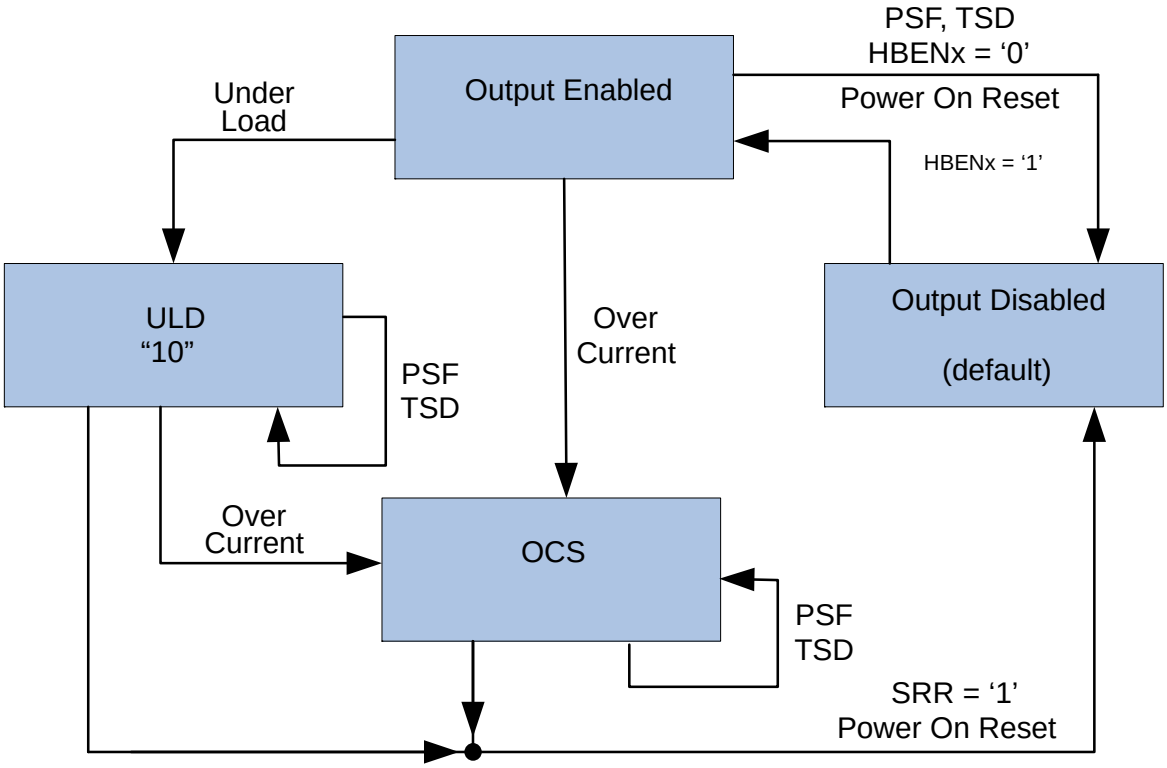
Table 2. SPI STATUS OUTPUT DEFINITIONS

Channels 12 – 7 (If Previous Input Bit # 14 = 1)				
Bit#	**Name**	**Function**	**Status***	**Scope**
PRE_15	TSD	Latched Thermal Shutdown	1 = Fault	Global Notification; Per Half−Bridge Operation
15	OCS	Latched Overcurrent Shutdown	1 = Fault	Notification per **HBSEL**; Per Half−Bridge Operation
14	PSF	VS1 and/or VS2 Undervoltage or Overvoltage	1 = Fault	Global Notification and Global Operation
13	ULD	Underload Detect	1 = Fault	Notification per **HBSEL**; Per Half−Bridge Operation
12	HBST12 [1:0]	Half−Bridge 12 Output Status	0x00b − Output Disabled 0x01b − OCS 0x10b − ULD 0x11b − Output Enabled	Per Half−Bridge
11				
10	HBST11 [1:0]	Half−Bridge 11 Output Status		
9				
8	HBST10 [1:0]	Half−Bridge 10 Output Status		
7				
6	HBST9 [1:0]	Half−Bridge 9 Output Status		
5				
4	HBST8 [1:0]	Half−Bridge 8 Output Status		
3				
2	HBST7 [1:0]	Half−Bridge 7 Output Status		
1				
0	TW	Thermal Warning	1 = Fault	Global Notification; Per Half−Bridge Operation

*All status output bits are set to 0 at Vcc power−on reset (POR).
HBSTx[1:0] bits are priority encoded to provide the status information of each of the half−bridge outputs. Figure 13 shows the priority encoding state diagram for the HBSTx[1:0] bits.

Table 2. SPI STATUS OUTPUT DEFINITIONS

Channels 6 – 1 (If Previous Input Bit # 14 = 0)				
Bit#	**Name**	**Function**	**Status***	**Scope**


PSF, TSD
HBENx = ‘0’
Power On Reset
Output Enabled
Under
Load
HBENx = ‘1’
ULD
“10”
PSF
TSD
Over
Current
Output Disabled
(default)
Over
Current
OCS
PSF
TSD
SRR = ‘1’
Power On Reset

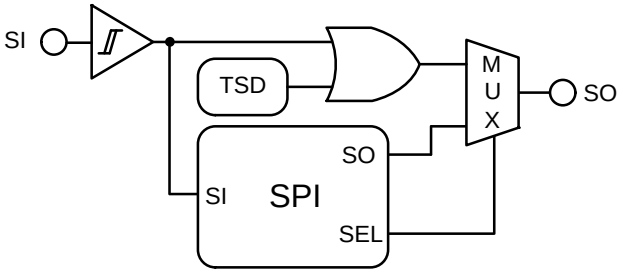
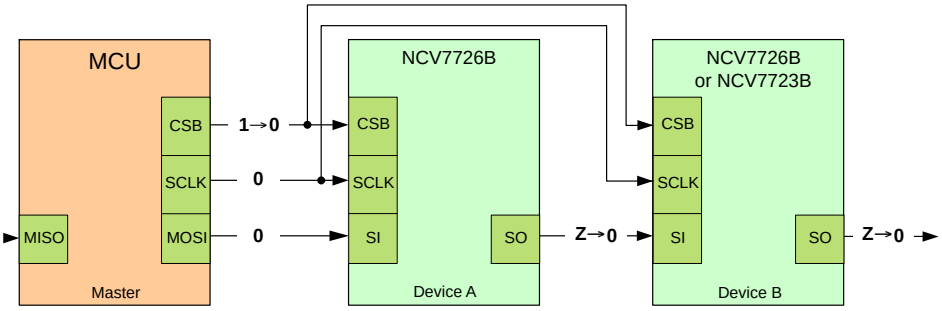


Figure 16. TSD SPI Link



DIAGNOSTICS, PROTECTIONS, STATUS REPORTING AND RESET

Overview

The NCV7726B employs diagnostics designed to prevent destructive overstress during a fault condition. Diagnostics are classified as either supervisory or protection functions (Table 3). Supervisory functions provide status information about device conditions. Protection functions provide status information and activate fault management behaviors.

Diagnostics resulting in output shutdown and latched status may depend on a qualifier and may require user intervention for output recovery and status memory clear. Diagnostics resulting in output lockout and non−latched status (VSOV or VSUV) may recover and clear automatically. Output configurations can be changed during output lockout. Outputs assume the new configurations or resume the previous configurations when an auto−recover fault is resolved. Table 4 shows output states during faults and output recovery modes, and Table 5 shows the status memory and memory clear modes.

Table 3. DIAGNOSTIC CLASSES AND FUNCTIONS

Name	Class	Function
TSD	Protection	Thermal Shutdown
OCS	Protection	Overcurrent Shutdown
PSF	Protection	

Status Information Retrieval

Current status information as selected by HBSEL is retrieved during each SPI frame. To preserve device configuration and output states, the previous SI data pattern must be sent during the status retrieval frame.

Status information is prevented from being updated

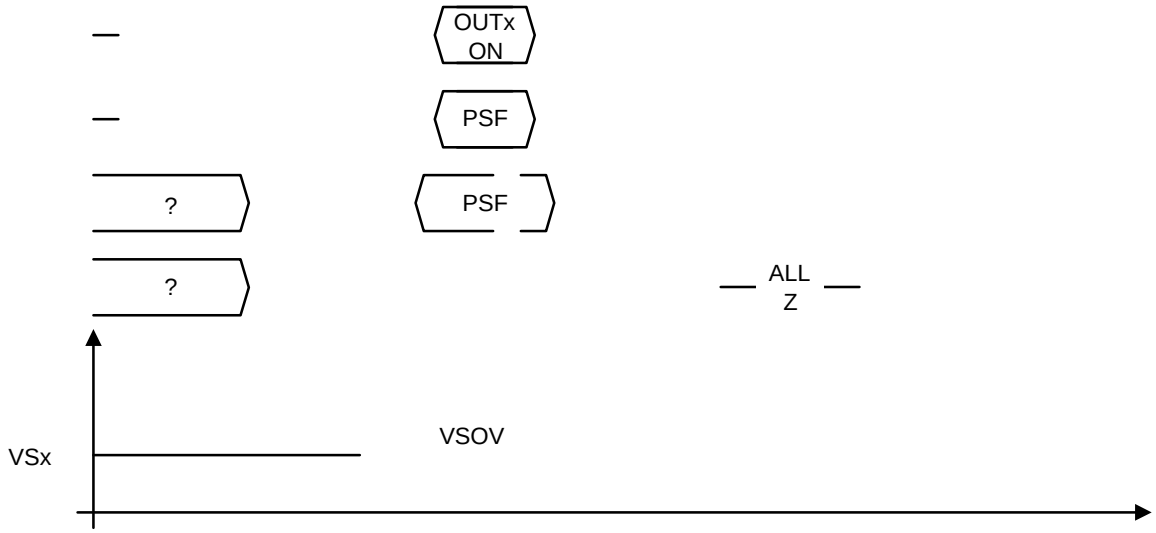
Overvoltage Lockout

Global Notification, Global Operation

Overvoltage detection and lockout control is provided by monitoring the VS1 and VS2 supply inputs. Overvoltage hysteresis is provided to ensure clean detection transitions. Overvoltage timing is shown in Figure 20.

Overvoltage at either VSx input turns off all outputs if the overvoltage lockout input bit is set (OVLO = 1, HBSEL = X), and sets the power supply fail (PSF) status bit (see Tables 4 and 5). The outputs return to their previously programmed state and the PSF status bit is cleared when VSx falls below the hysteresis voltage level. Output enable and configuration states can also be programmed during an overvoltage lockout event but will not change state until VSx falls below the overvoltage threshold level.

To reduce stress, it is recommended to operate the device with OVLO bit asserted to ensure that the drivers turn off during a load dump scenario. If OVLO = 0 during an overvoltage condition, outputs will remain on and the PSF status bit will be set.



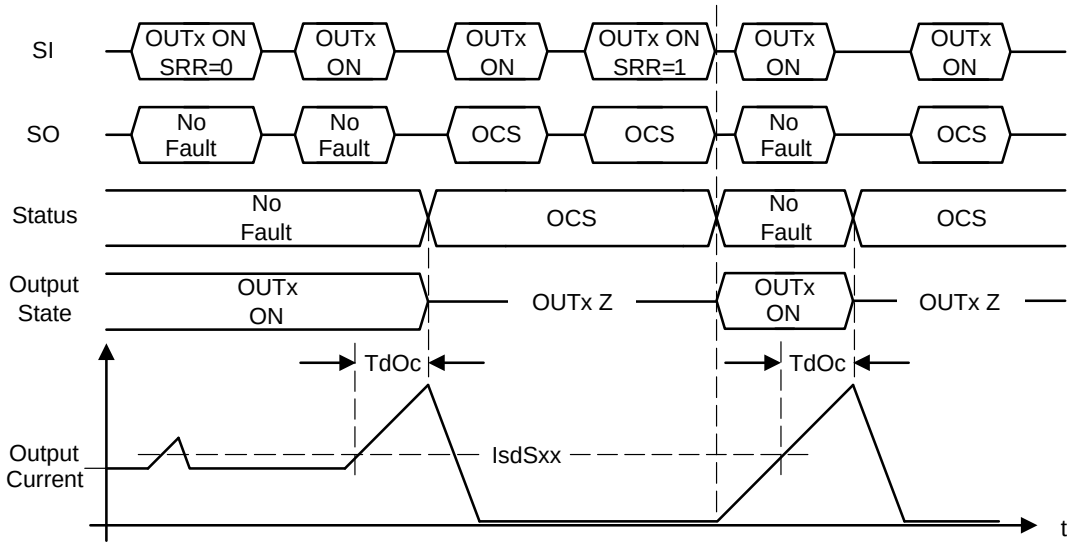


Figure 21. Overcurrent Timing

Underload Shutdown

Global and per Channel Notification per HBSEL
Shutdown Control per HBSEL
Per Half−Bridge Operation

Underload

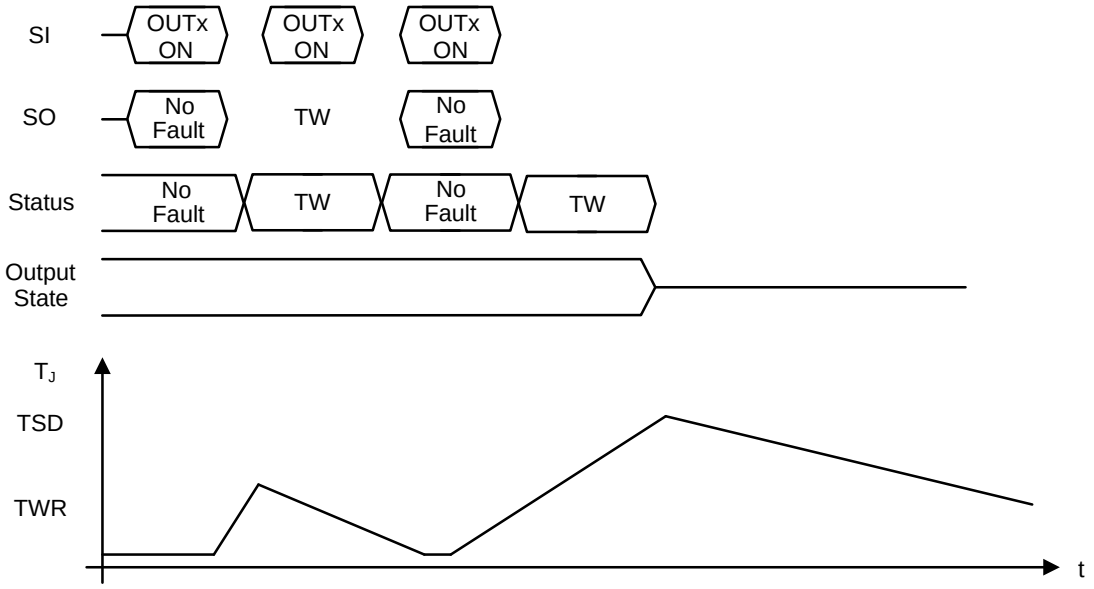
Thermal Warning and Thermal Shutdown

Global Notification, Per Half−Bridge Operation

Thermal warning (TW) and thermal shutdown (TSD) detection and control are provided for each half−bridge by monitoring the driver pair's thermal sensor. Thermal hysteresis is provided for each of the warning and shutdown functions to ensure clean detection transitions. Software polling of the TW bit allows for avoidance of thermal shutdown since TW notification precedes TSD notification. Thermal warning and shutdown timing is shown in Figure 23.

The TW status bit is set when a half−bridge's sensor temperature exceeds the warning level (T_J > Twr), and the bit is automatically cleared when sensor temperature falls below the warning hysteresis level (T_J < TwHy). A channel's output state is unaffected by TW.

When sensor temperature exceeds the shutdown level (T_J > Tsd), the channel's HS and LS drivers are latched off, the TW bit is/remains set, and the TSD (PRE_15) bit is set. The TSD bit is cleared and all affected channels are re−activated (T_J < TsdHy) by sending SRR = 1. The channel group select (HBSEL) input bit determines which channels are affected by SRR.



TW

THERMAL PERFORMANCE ESTIMATES

Figure 24. Transient R(t) vs. Pulse Time for 2 oz Spreader

ORDERING INFORMATION

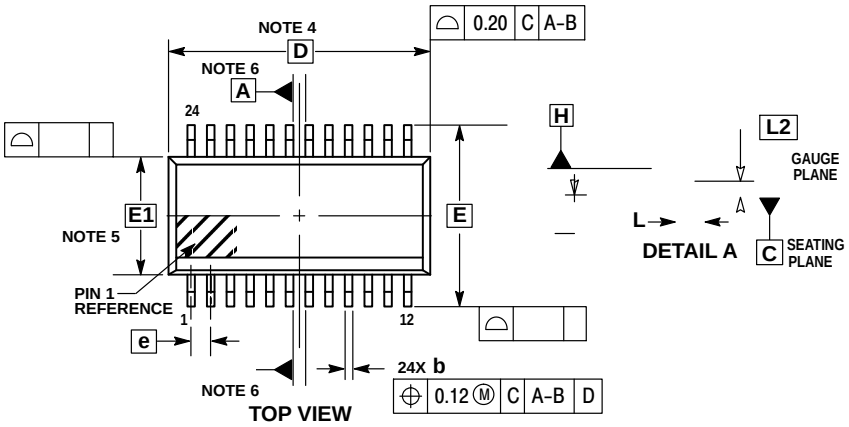
Device	Package	Shipping†
NCV7726DQBR2G	SSOP24 EP (Pb−Free)	2,500 / Tape & Reel

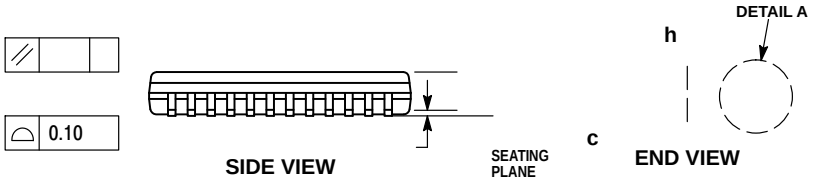
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

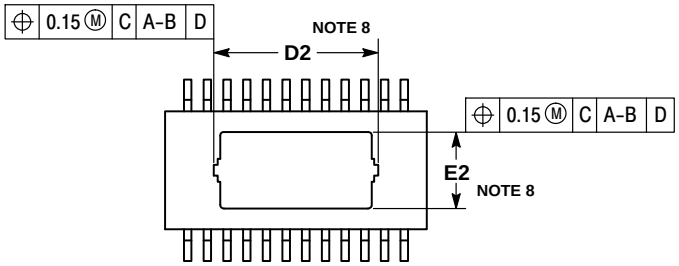
SSOP24 NB EP
CASE 940AK
ISSUE O

SCALE 1:1

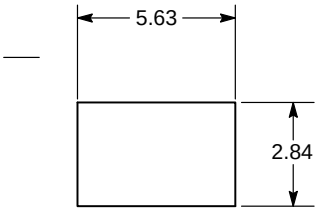
DATE 24 APR 2012







SOLDERING FOOTPRINT



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.10 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. DIMENSION b APPLIES TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D IS DETERMINED AT DATUM PLANE H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM PLANE H.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. CONTOURS OF THE THERMAL PAD ARE UNCONTROLLED WITHIN THE REGION DEFINED BY DIMENSIONS D2 AND E2.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.70
A1	0.00	0.10
b	0.19	0.30
c	0.09	0.20

D2	5.28	5.58

E1	3.90 BSC	
E2	2.44	2.64
e	0.65 BSC	
h	0.25	0.50
L	0.40	0.85
L1	1.00 REF	
L2	0.25 BSC	
M	0°	8°