NCV7728

Hex Half-Bridge Driver

The NCV7728 is a Hex Half−Bridge Driver with protection features designed specifically for automotive and industrial motion control applications. The NCV7728 has independent controls and diagnostics. The device can be operated in forward, reverse, brake, and Cge Dr6h5.3001962 TD0 Tc (onsemi.com)TjET441.411 610.696 5

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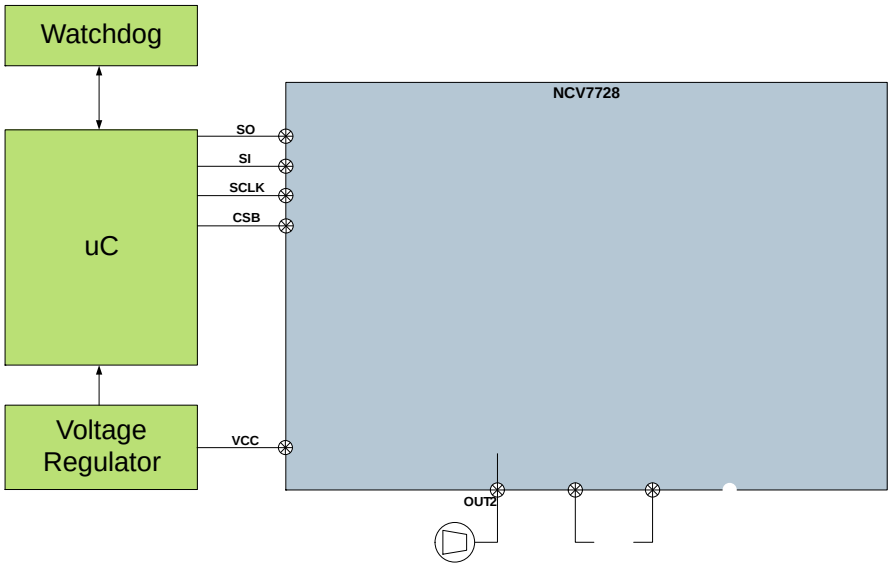
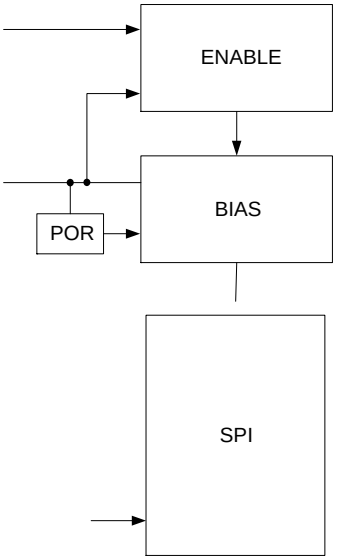
Publication Order Number:
NCV7728/D

Shown below is a typical application for the NCV7728 configuration.




ENABLE
BIAS
POR
SPI

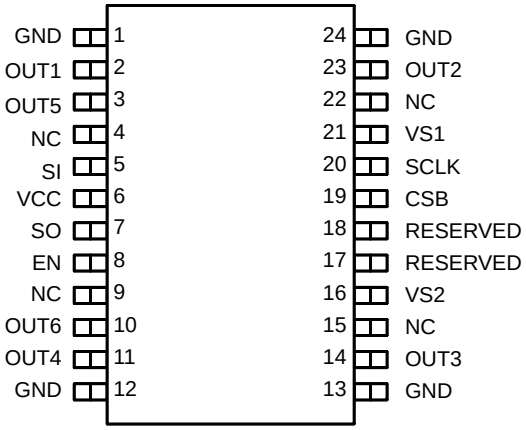


Figure 3. Pinout − SSOP24

PACKAGE DESCRIPTION The pin−out for the Hex Half−Bridge in SSOP24 package is shown in the table below.

Pin # SSOP24	Symbol	Description
1	GND	Ground. Shorted to pin 24 internally.
2	OUT1	Half Bridge Output 1
3	OUT5	Half Bridge Output 5
4	NC	No Connection. This pin should be isolated from any traces or via on the PCB board.
5	SI	Serial Input. 16 bit serial communications input. 3.3 V/5 V (TTL) Compatible. Internally pulled down.
6	VCC	Power supply input for Logic.
7	SO	Serial Output. 16 bit serial communications output. 3.3 V/5 V Complaint
8	EN	Enable. Input high wakes the IC up from a sleep mode. 3.3 V/5 V (TTL) Compatible. Internally pulled down.
9	NC	No Connection. This pin should be isolated from any traces or via on the PCB board.
10	OUT6	Half Bridge Output 6
11	OUT4	Half Bridge Output 4
12	GND	Ground. Shorted to pin 13 internally.
13	GND	Ground. Shorted to pin 12 internally.
14	OUT3	Half Bridge Output 3
15	NC	No Connection. This pin should be isolated from any traces or via on the PCB board.
16	VS2	Voltage Power Supply input for the Drivers 3, 4 and 6. This pin must be connected to VS1 externally.
17	Reserved	Factory use − connect to GND or leave unconnected − internally pulled down.
18	Reserved	Factory use − connect to GND or leave unconnected − internally pulled down.
19	CSB	Chip Select Bar. Active low serial port operation. 3.3V/5V (TTL) Compatible. Internally pulled up.
20	SCLK	Serial Clock. Clock input for use with SPI communication. 3.3 V/5 V (TTL) Compatible. Internally pulled down.
21	VS1	Voltage Power Supply input for the Drivers 1, 2 and 5, all the pre−drivers and the charge pump. This pin must be connected to VS2 externally.
22	NC	No Connection. This pin should be isolated from any traces or via on the PCB board.
23	OUT2	Half Bridge Output 2
24	GND	Ground. Shorted to pin 1 internally.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (VS1, VS2) (DC) (AC), t < 500ms, Ivsx > −2A	VsxdcMax VSXac	 −0.3 to 40 −1.0	V
Output Pin OUTx (DC) (AC), t< 500ms, IOUTx > −1.1A (AC), t< 500ms, IOUTx < 1A	VoutxDc VoutxAc	 −0.3 to 40 −1.0 1.0	V
Pin Voltage (Logic Input pins, SI, SCLK, CSB, SO, EN, V_{CC})	VioMax	−0.3 to 5.5	V
Output Current (OUT1, OUT2, OUT3, OUT4, OUT5, OUT6)	IoutxImax	−2.0 to 2.0	A
Electrostatic Discharge, Human Body Model, VSx, OUTx (AEC−Q100−002)	Vesd4k	4.0	kV
Electrostatic Discharge, Human Body Model, all other pins (AEC−Q100−002)	Vesd2k	2.0	kV
Electrostatic Discharge, Machine Model (AEC−Q100−003)	Vesd200	200	V
Short Circuit Reliability Characterization	AECQ10x	Grade A	−
Operating Junction Temperature	Tj	−40 to 150	°C
Storage Temperature Range	Tstr	−55 to 150	°C
Moisture Sensitivity Level (MAX 260°C Processing)	MSL2	2	−

Stresses

ELECTRICAL CHARACTERISTICS (−40°C < TJ < 150°C, 5.5 V < VSx < 40 V, 3.15 < Vcc < 5.25 V, EN= Vcc, unless otherwise specified)

Characteristic	Symbol	Conditions	Timing Chart	Min	Typ	Max	Unit
DRIVER OUTPUT TIMING SPECIFICATIONS							
High Side Turn On Time	ThsOn	VSx = 13.2 V, R_{load} = 39 Ω		−	7.5	13	μs
High Side Turn Off Time	ThsOff	VSx = 13.2 V, R_{load} = 39 Ω		−	3.0	6.0	μs
Low Side Turn On Time	TlsOn	VSx = 13.2 V, R_{load} = 39 Ω		−	6.5	13	μs
Low Side Turn Off Time	TlsOff	VSx = 13.2 V, R_{load} = 39 Ω		−	2.0	6.0	μs
High Side Rise Time	ThsTr	VSx =13.2 V, R_{load} = 39 Ω		−	4.0	8.0	μs
High Side Fall Time	ThsTf	VSx = 13.2 V, R_{load} = 39 Ω		−	2.0	4.0	μs
Low Side Rise Time	TlsTr	VSx = 13.2 V, R_{load} = 39 Ω		−	1.0	3.0	μs
Low Side Fall Time	TlsTf	VSx = 13.2 V, R_{load} = 39 Ω		−	1.0	3.0	μs
High Side Off to Low Side On Non−Overlap Time	ThsOffLsOn	VSx = 13.2 V, R_{load} = 39 Ω		1.5	−	−	μs
Low Side Off to High Side On Non−Overlap Time	TlsOffHsOn	VSx = 13.2 V, R_{load} = 39 Ω		1.5	−	−	μs
SERIAL PERIPHERAL INTERFACE							
SCLK Frequency	Fclk	V_{CC} = 5 V V_{CC} = 3.15 V		− −	− −	5.0 2.0	MHz
SCLK Clock Period	TpClk	V_{CC} = 5 V V_{CC} = 3.15 V		200 500	− −	− −	ns
SCLK High Time	TclkH		1	85	−	−	ns
SCLK Low Time	TclkL		2	85	−	−	ns
SCLK Setup Time	TclkSup		3 4	85 85	− −	− −	ns
SI Setup Time	TsiSup		11	50	−	−	ns
SI Hold Time	TsiH		12	50	−		

ELECTRICAL CHARACTERISTIC TIMING DIAGRAMS

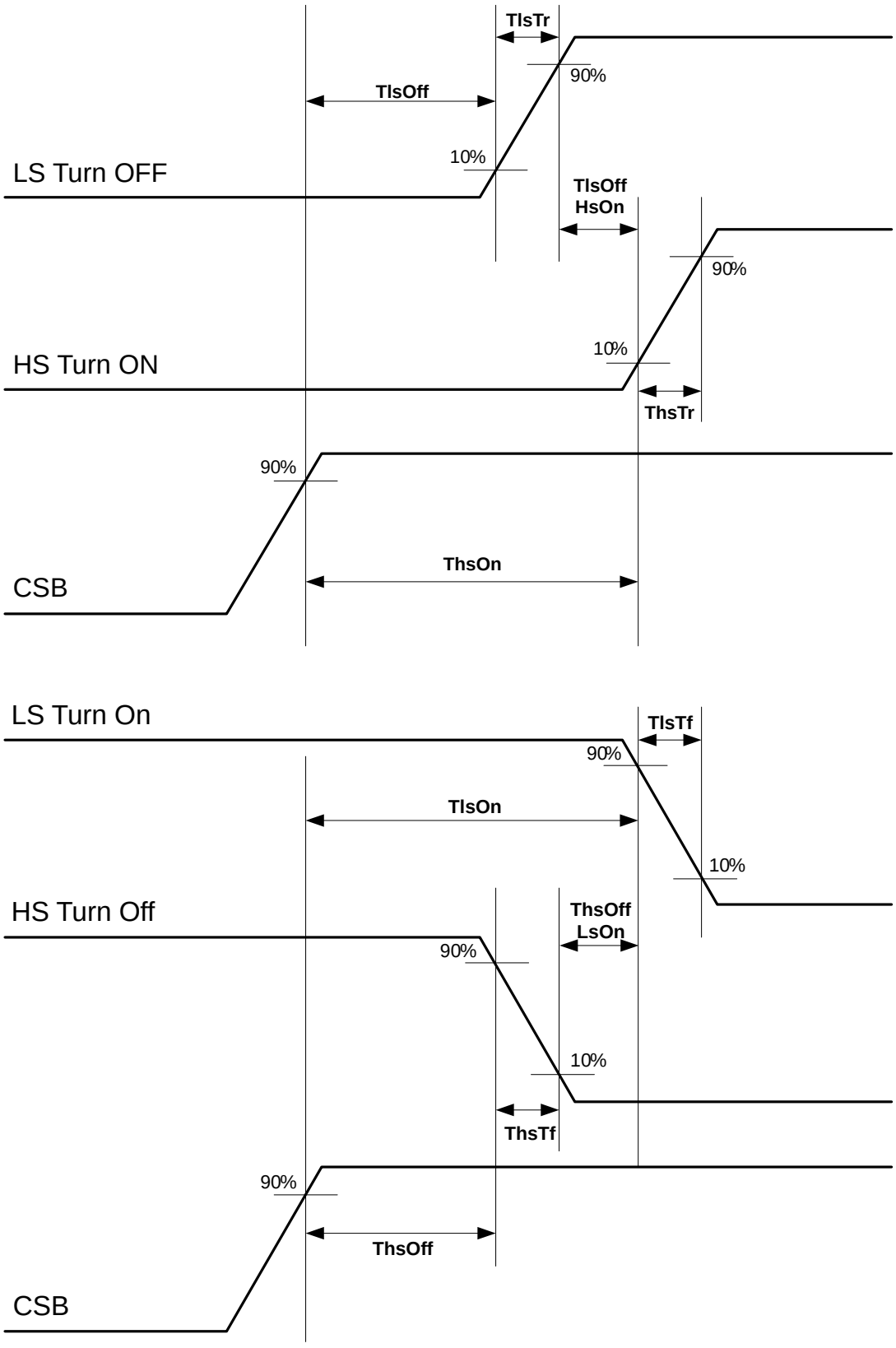


Figure 4. Detailed Driver Timing

TYPICAL PERFORMANCE GRAPHS

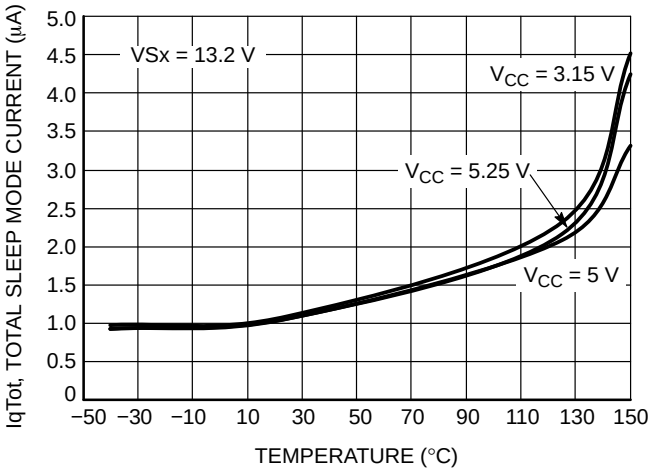


Figure 6. IqTot vs. Temperature

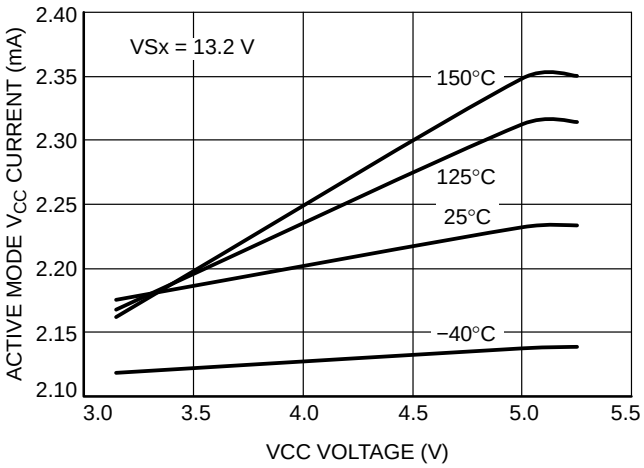


Figure 7. I(V_{CC}) Active Mode vs. V(V_{CC})

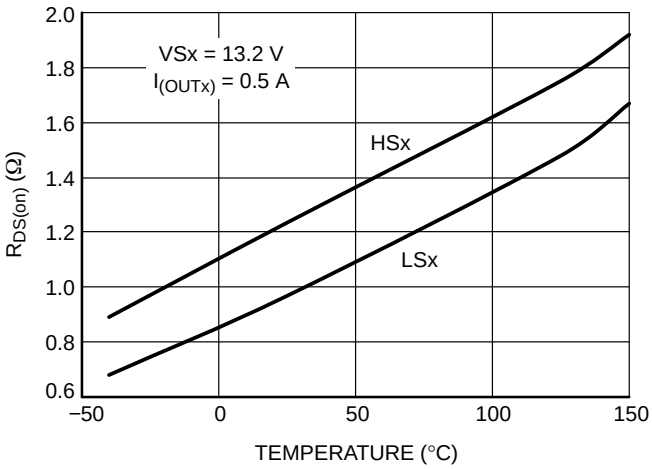


Figure 8. $R_{DS(on)}$ vs. Temperature

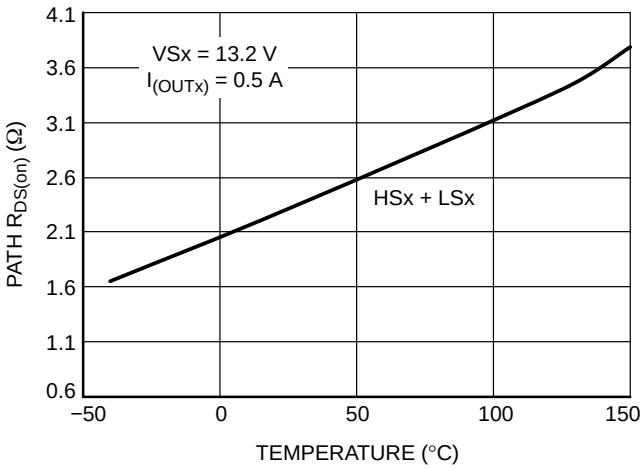


Figure 9. $R_{DS(on)}$ vs. Temperature

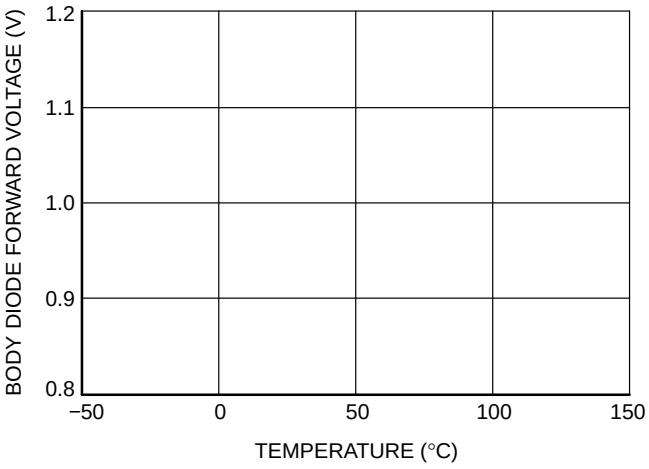


Figure 10. Body Diode vs. Temperature

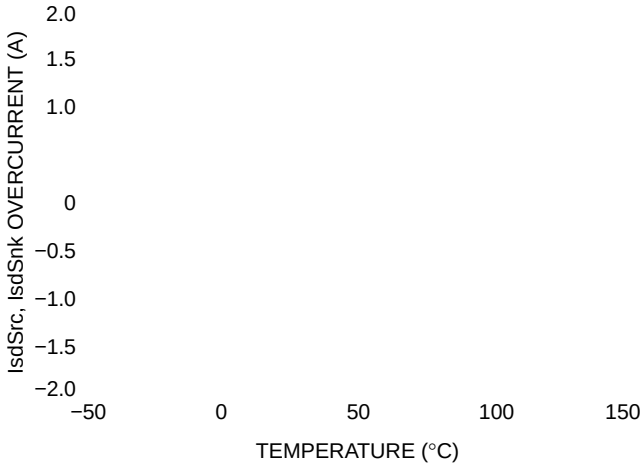


Figure 11. Overcurrent vs. Temperature

TYPICAL PERFORMANCE GRAPHS

OPERATING DESCRIPTION

General Overview

The NCV7728 is comprised of twelve DMOS power drivers (six PMOS High Side Driver and six NMOS Low Side Driver) configured as six half bridges that enables three independent Full Bridge operations. Each output drive is characterized for a max 550 mA DC load and has a typical 2 A surge capability (at VSx =13.2 V). Strict adherence to integrated circuit die temperature is necessary. Maximum die temperature is 150°C. This may limit the number of drivers enabled at one time. Output drive control and fault reporting is handled via the SPI (Serial Peripheral Interface) port.

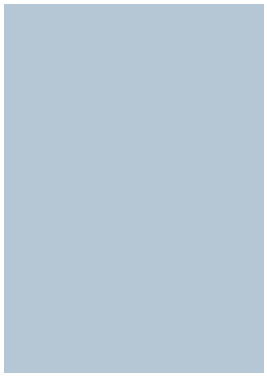
An Enable function (EN) provides a low quiescent sleep current mode when the device is not being utilized. No data is stored when the device is in sleep mode. An internal pull down resistor is provided on the EN input to ensure the device is off if the input signal is lost. De−asserting the EN signal clears all the registers and resets the driver. When the EN signal is asserted the IC will proceed with the V_{CC} POR cycle and brings the drivers into normal operation.

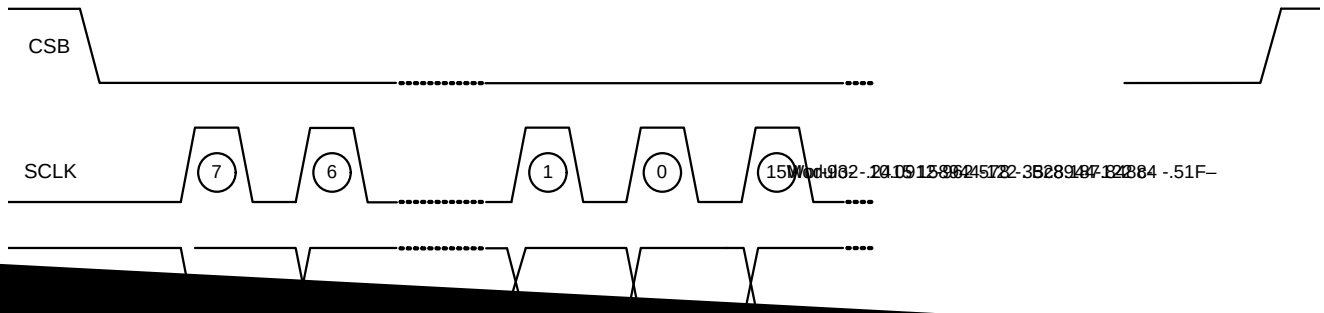
SPI Communication

16−bit full duplex SPI communication has been implemented for the communication of this IC for device configurations, driver controls and reading the diagnostic

Table 2. SPI OUTPUT DATA FRAME

Output Data			
Bit Number	**Bit Name**	**Bit Description**	**Bit Status**
PRE_15	TSD	Latched Thermal Shutdown	0 = No Fault 1 = Fault
15	OCS		




CSB
SCLK
7
6
1
0
15

DEVICE PROTECTION, DIAGNOSTICS AND FAULT REPORTING

Power Up/Down Control

Each analog power pin (VS1 or VS2) powers their respective output drivers. After a device has powered up and the output drivers are allowed to turn on, the output drivers will not turn off until the voltage on the supply pins is reduced below the initial under voltage threshold, exceeds the over voltage threshold or if shut down by either a SPI command or a fault condition.

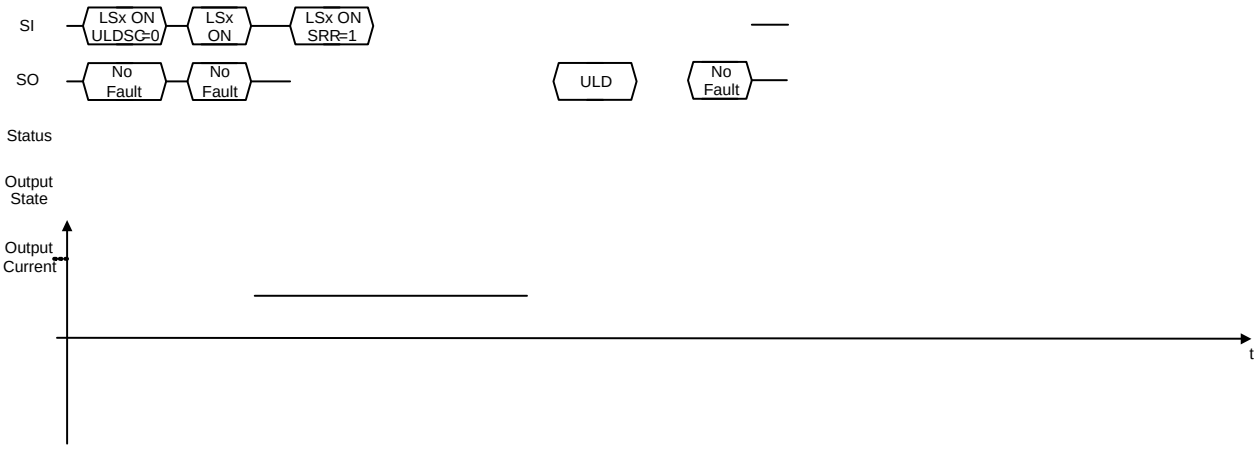
Internal power−up circuitry on the logic supply pin supports a smooth turn on transition. VCC power up resets the internal logic such that all output drivers will be off as power is applied. All the internal counters, SI and SO along with all the digital registers will be cleared on VCC POR. Exceeding the under voltage lockout threshold on VCC allows information to be input through the SPI port for turn on control. Logic information remains intact over the entire VS1 and VS2 voltage range.

Under Voltage Shutdown

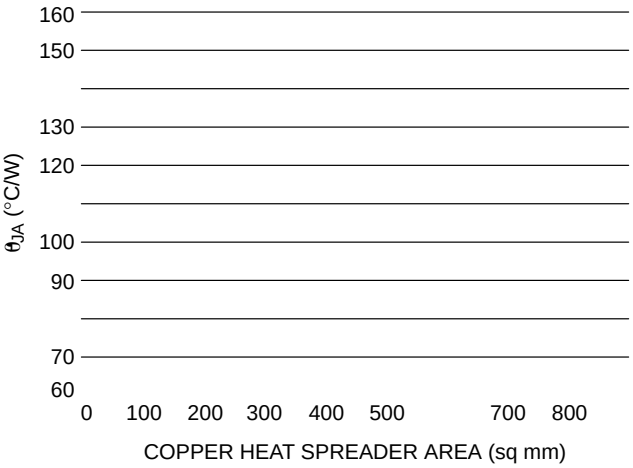
An under voltage lockout circuit prevents the output drivers from turning on unintentionally. This control is provided by monitoring the voltages on the VS1, VS2 and VCC pins. A built−in hysteresis on the under voltage threshold is included to prevent an unknown region on the power pins; VCC, VS1 and VS2. When the VCC goes below the threshold, all outputs are turned off and the input and output registers are cleared.

An under voltage condition on the VSx pins will result in shutting off

Over Voltage Shutdown


SI
LSx ON ULDSC=0
LSx ON
LSx ON SRR=1
SO
No Fault
No Fault
ULD
No Fault
Status
Output State
Output Current
t

Thermal Performance



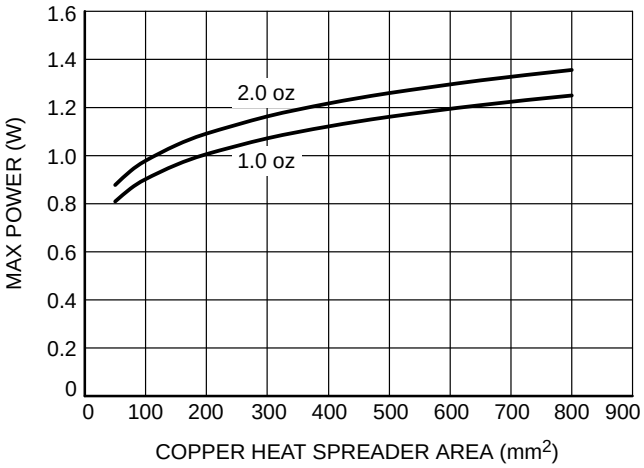


Figure 26. θ_{JA} vs. Cu Area

Fault Handling

At an event of a driver latched off fault, the offending half−bridge driver is disabled and the half−bridge configuration is defaulted to zero (HBENx =0, HBCNFx =

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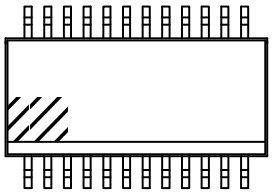
SCALE 1:1



DIM	MILLIMETERS MIN	MAX
A		1.75
A1	0.10	0.25
b	0.20	0.30
c	0.19	0.25
e	0.65 BSC	
h	0.22	0.50
L	0.40	1.27
L2	0.25 BSC	