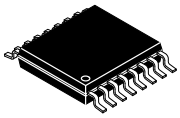
Inductive Position Sensor Interface

NCV77320



TSSOP−16
CASE 948F−01

Introduction

The NCV77320 is a single−chip inductive position sensor interface that, in combination with a *PCB*, forms a system that measures angular or linear positions accurately.

The operating principle of the inductive sensor is based on mutual inductance. The chip contains an excitation source, which generates an AC magnetic field through a primary coil on the PCB. The field mutually couples to the rotor. The rotor on its turn induces voltages in secondary coils. These voltages, measured by the chip, depend on the rotor position and give a measure for the position.

The NCV77320 contains 3 interfaces: A single ended analog output, a SENT interface with fast and slow channel and a SPI channel for direct interconnection to a micro controller.

The analog output is proportionally ratio metric with the supply voltage.

The NCV77320 has several fault detection circuitries. When a fault is detected, fault flags are set and available for readout. In case the analog output is used, OUT pin is put to HiZ and its voltage goes to fail band close to GND or VCC based on the pull−up or pull−down resistor assembled.

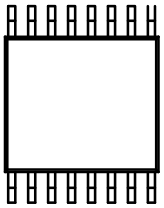
To address automotive functional safety, different kind of topologies can be implemented, e.g.:

- Two devices with independent supplies. There is no galvanic connection between the ICs. Each IC drives its own excitation coil and measures its own set of receiver coils.
- Two devices with their own supply but with a shared excitation coil connected to both ICs.

Features

- Integrated DSP Position Calculation with Flexible 15 Point Linearization
- Diagnostics, Including for Missing Wire / Wire Misconnection Tolerant
- Analog Output or SENT Output Configurable
- Temperature Sensor Embedded
- SPI Watchdog Feature
- Supply Voltage 5 V; −15 V to 30 V Tolerant Robustness
- Flexible SPI Operation with 3.3 V or 5 V Micro Controllers
- Maximum Rotational Speed of 10800 rpm
- Operating Ambient Temperature −40 to 150°C
- Developed According to the Automotive Safety Standard ISO26262
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MARKING DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping
	–	

Typical Applications

- Angular Position Sensors Up to 360°, e.g. Pedal Position, Throttle Position, Chassis Height, Actuators Position Feedback etc.
- Linear Position Sensors, e.g. Lever Position, Linear Actuator, Level Sensors etc.

QUICK REFERENCE DATA

Table 1. MAXIMUM RATINGS

Rating	Min	Max	Unit
	–		
	–		
	–		
	–		
	–		
	–		°
	–		°

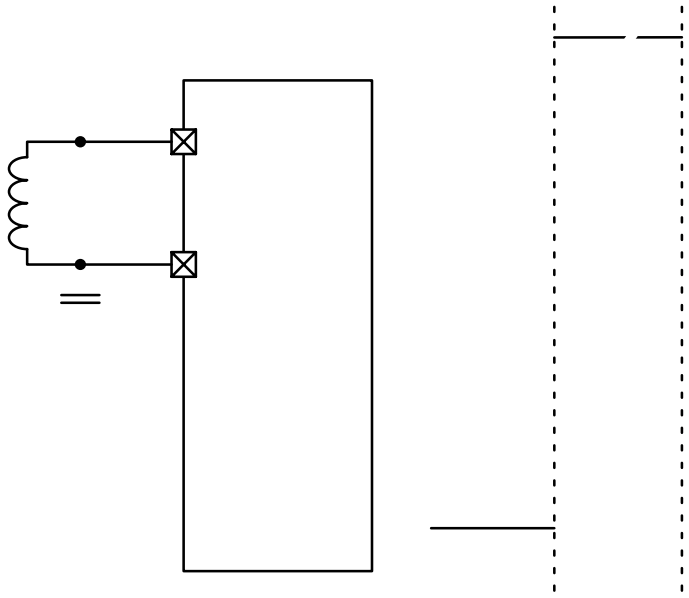


Figure 2. NCV77320 Single Chip Application Diagram with SENT Output

Table 4. EXTERNAL COMPONENTS

Component	Description	Min. Value	Typ. Value	Max. Value	Note

Table 6. OPERATING PARAMETERS

Parameter	(Test) Conditions	Min	Typ	Max	Unit
VCC RELATED					
		–	–		
		–	–		

Table 6. OPERATING PARAMETERS

Table 7. THERMAL ASPECTS

Parameter	Description	Typ	Unit

°

SPI TIMING PARAMETERS

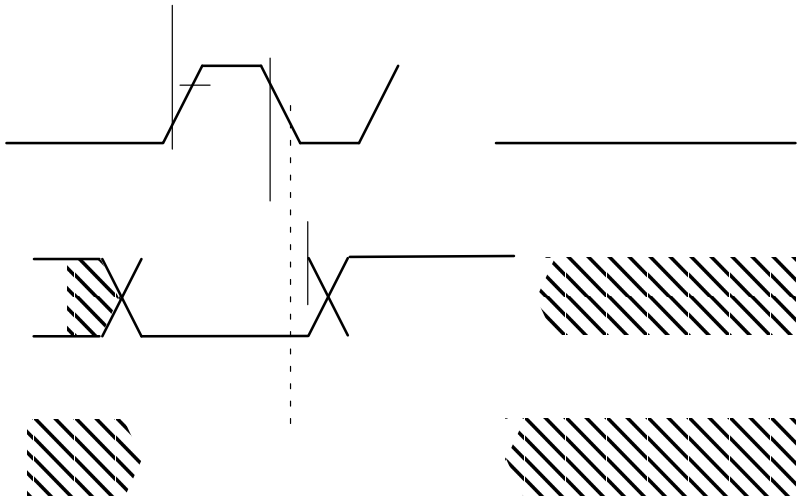


Figure 6. SPI Timing Diagram

Figure 9. Principle of Inductive Coupling Sensor

The calculated 16−bit position “pos_raw[15:0]” can be adjusted to application “zero” position by “pos_shift[15:0]” EEPROM parameter. This operation can replace a need for mechanical alignment of a rotor with a sensor PCB. The adjustment is shown in Figure 11 and follows the modulo equation:

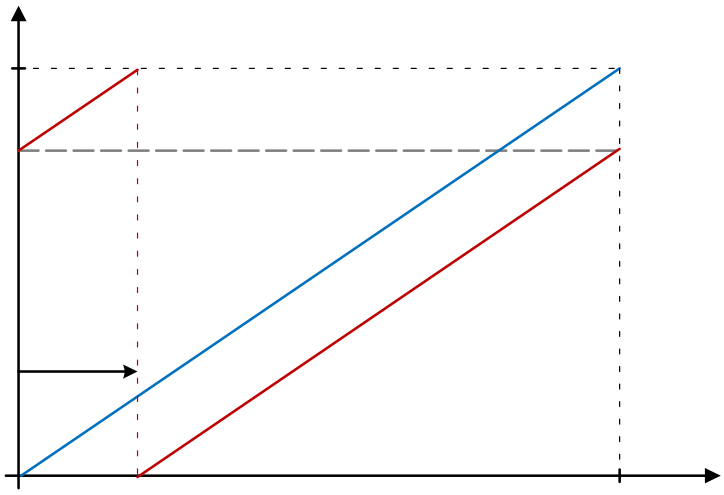


Figure 11. Zero Angle Adjustment Using “pos_shift[15:0]” Register

Multipoint PWL Correction Table

The adjusted position “pos_adj[15:0]” is processed by an 15−point PWL (piece−wise−linear) correction unit. Up to 15 points “$P_k[X_k,Y_k]$” are available ($k \in <0;14>$). The points 0 and 14 have x−position bound to the minimum and the maximum of the “pos_adj[15:0]” range, other points can be set to arbitrary values in ascending order as shown in Figure 12. Correction starts always with point P_0 and continues with next points P_1, P_2, … until a point which has value X_k = 65535.

When the analog output interface is used, it should be limited by programming the PWL table (Y_k) to stay within range of 5% to 95% Vcc, defined by parameters “V_{out_hi}” and “V_{out_lo}” in Table 6. The SENT output should be programmed with the PWL correction table to comply with the SENT specification for the output ranging between 1 and 4088. For the SPI interface, the full output range can be used.

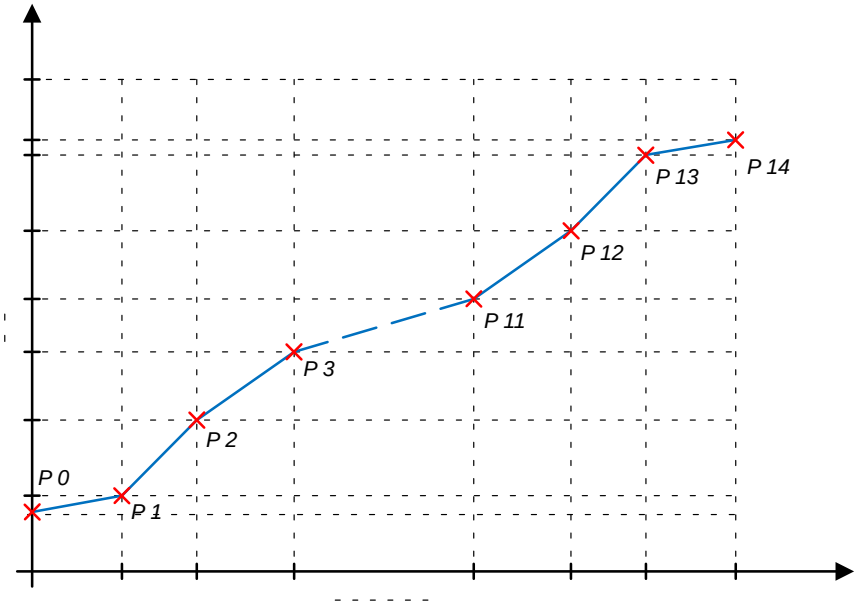


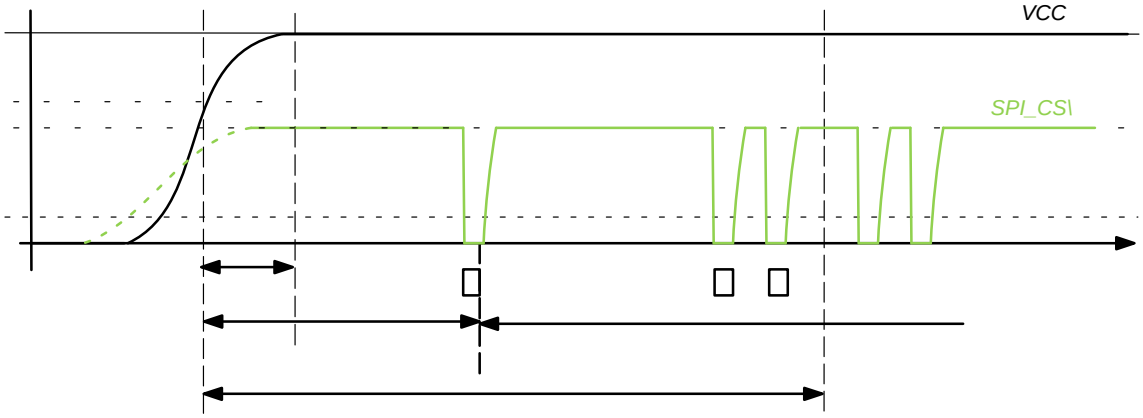
Figure 12. Multi−point PWL Correction Unit

POWER UP AND OPERATING MODES

The NCV77320 is in POR (power−on−reset) when regulated voltage (VDD pin) drops below “POR_hi” voltage level. The release from POR is additionally conditioned by VCC supply voltage going above “VCC_UV” threshold. A power−up sequencer is implemented in the NCV77320 to bring the device in different modes. The chip can be in two modes after power up:

1. Service mode
2. Operating mode

1) *Service mode* can be entered after POR within the “t_service_max” time window as specified in Table 6. Service mode can be achieved in two ways:
   a. With the serial communication bus operated via the OUT pin:
      This interface is suitable for end of line programming for automotive applications, where only 3 output terminals are used to interface the sensor (GND, OUT and VCC). The interface is described in application note AND90288/D, which is available under NDA.
   b. Via SPI:
      To enter Service mode, the SPI Key−code should be send to the device. After reception of the Key−code, the specific calibration registers can be addressed (Service mode). The SPI Key−code must be received as a first SPI frame and must be received before “t_service_max” time elapses. The NCV77320 is ready to decode SPI Key−code after initialization phase “t_INIT”. The SPI Key−code can be received and SPI Service mode can be opened regardless of SPI activation EEPROM bit “spi_ena”. Figure 16 shows the diagram for entering Service mode via SPI.
      For normal operation, the device needs to be brought to Operating mode via the “EXIT” SPI command.
2) *Operating mode* is achieved after appliance of the normal VCC operating voltage. After POR, the chip will load the operational EEPROM parameters into the device registers. The content of the registers defines behavior of the chip. When the device is brought into Operating mode from Service mode using the ”EXIT” command, the EEPROM parameters are not loaded to the device registers.
   Accessibility of the chip and pin function in Operating mode is summarized in Table 12. The OUT driver and/or SPI interface is activated after initialization phase “t_INIT” elapses.



Analog Output

The analog driver consists of 16−bit DAC and voltage

Table 13. SENT FRAME FORMAT

Pulse / Nibble	Nibble content	
	H.1 SENT Frame Format sent_ch2_cnt = 0	H.4 SENT Frame Format sent_ch2_cnt = 1

The total signal delay in the SENT configuration with pause pulse enabled is equal to (SENT_delay + POS_DLY). The delay is taken to the 1st falling edge of the status nibble.

Without pause pulse, additional delay varies between 0 s and SENT frame length. SENT_delay = 71 s at typ. clock.

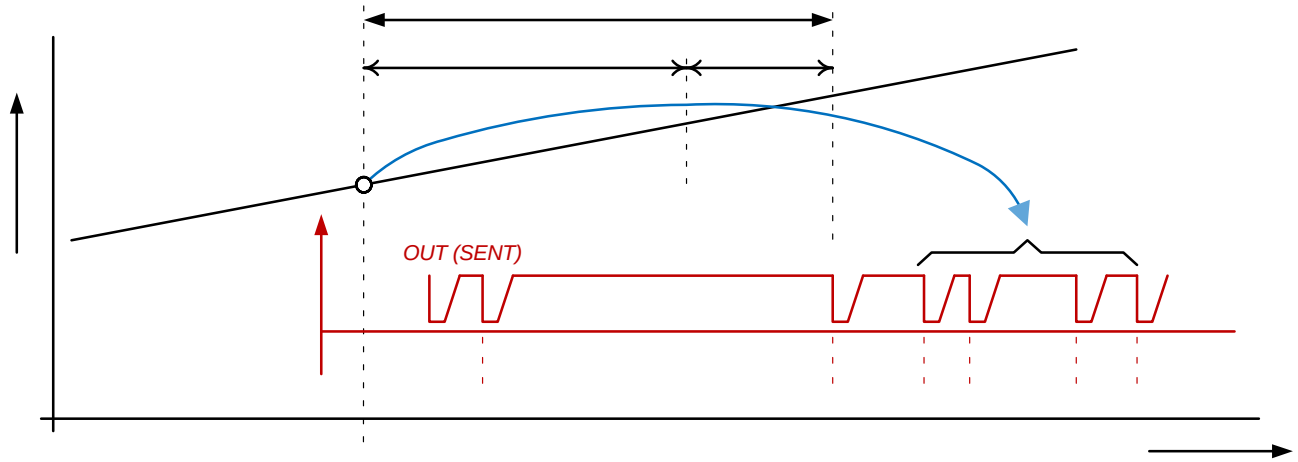


Figure 22. Signal Delay in the SENT Frame

Temperature Signal

Temperature information is provided on Fast Channel 2. Temperature is coded as a 12−bit number according to SAE J2716 E.2.2.1:

- Slope S_{TF} = 8 LSB / K
- Offset T_{OFFSET} = 200 K

–

Numerical temperature output range is limited to 1 .. 4088 which corresponds to −73.025°C to 437.85°C.

SENT Enhanced Serial Message

The NCV77320 makes use of the Enhanced serial channel for diagnostic and device information.

The Status bits 2 and 3 of the NCV77320 are used for the Enhanced serial channel operation. The drawing below shows the frame format. In total 18 SENT frames are used to build a full Enhanced serial message.

Bit 3 indicates the start of the Enhanced channel frame data when 6 consecutive “1” bits followed by one “0” is send. The configuration bit as being “0” and the 8 bits ID are following. Bit 2 contains only the CRC and 12 bits data content over the full Enhanced frame.

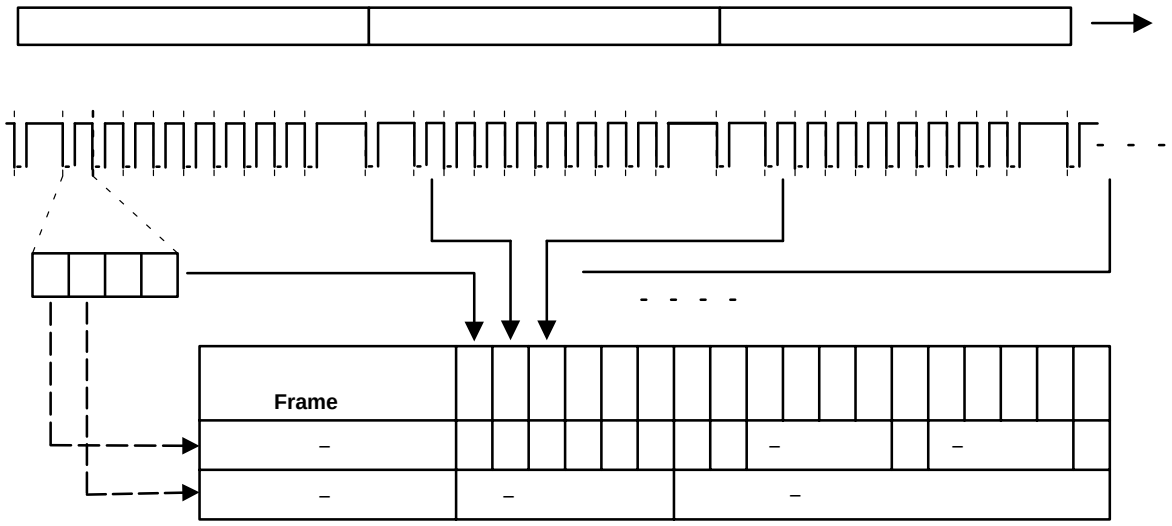


Figure 23. Enhanced Slow Channels SENT Frame Format

SENT serial communication is free running and not synchronized with any on chip failure. This means that depending on the error detected, the SENT driver is switched off (e.g. short at the output pin). The SENT serial communication does not necessarily start with SENT frame No.1 after the error is released and by that, the Master module always should resynchronize to the next full frame indicated by the start bits.

Table 15. ENHANCED SERIAL MESSAGE SEQUENCE

Serial Message No.	Message ID	Description	Data Field D[11:0]

SPI INTERFACE

Physical Interface

The NCV77320 has an SPI interface that is aside of the Analog output or SENT output operation active.

When the application does not require SPI operation, the “spi_ena” bit in the EEPROM should be set to “0”, the SPI_CS\, SPI_SI, SPI_CLK and SPI_SO pins should be tied to GND.

The VIO pin should be connected to the supply voltage (3.3 V or 5 V) of the micro controller that is used.

With the SPI interface, the NCV77320 is fully accessible and allows for event driven operation with the SPI_INT\ pin.

The SPI interface works in 32 bit mode but is compatible with 16 and 8 bit SPI interfaces. The high level block diagram of the SPI slave is shown in the following figure.

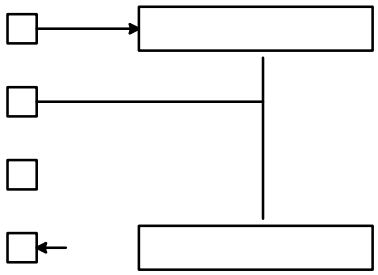


Figure 24. SPI High Level Block Diagram

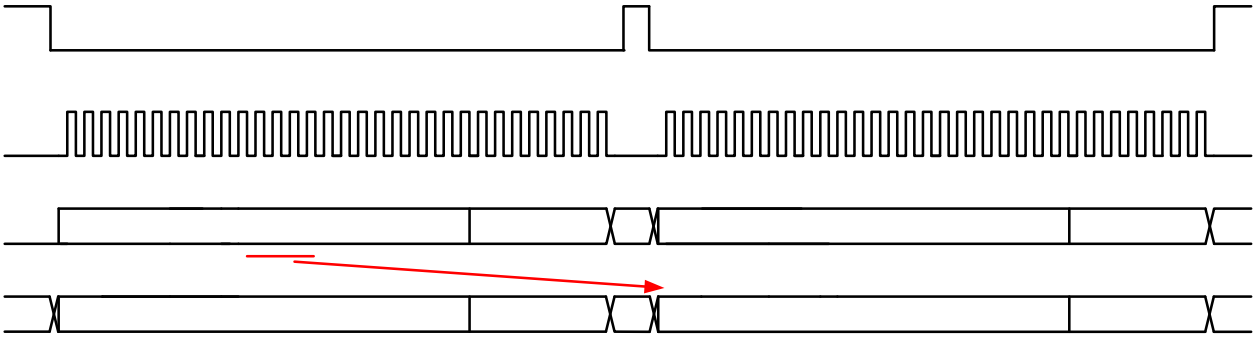


Figure 26. SPI Read Structure for Operational Mode Operation

SPI CRC 8−bit code (ATM−8) is calculated over the whole data in the frame using polynomial 0x107, seed value is 0xFF.

Polynomial:

+ + +

SPI in Service Mode

Figure 27 shows the command structure for Service mode. Sixteen bits are used for data. Next is a 6 bit start address, which selects an SPI address from where the data should be written or read. The command is given in the third byte, it is 3 bits long. The end address is given by the last 6 bits. While the Service mode is only used for End of line calibration, the messages do not contain a CRC for error detection and correction.

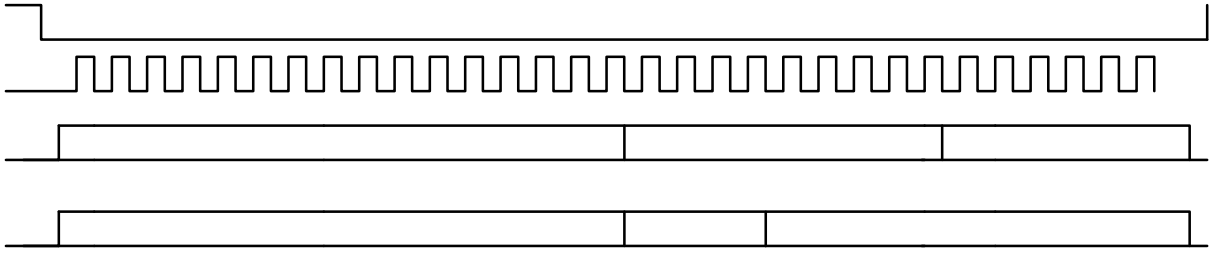


Figure 27. SPI Frame Structure for Service Mode Operation

After “PROG” command, the device is busy for “T_{PROG}” time with EEPROM programming. During that period, SPI response has all bits set to 1 and all incoming SPI frames are ignored.

After “VERIFY” command, master device should wait for “T_{VERIFY}” and then “ee_verify” (bit 15) can be checked by “READ_RT” command of address 12.

Tables 19 and 20 show all the accessible registers and the description for the bit and word functions.

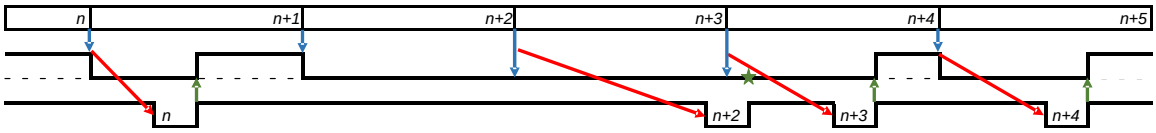
SPI Interrupt Output

The SPI interrupt is used to indicate to the micro controller that a new position/angle is available from the digital sampler or new ADC data is available in case of direct ADC data read out. After reset, the SPI_INT\ pin is high (Pull−up required to VIO). When a sample scan is finished, the SPI_INT\ pin goes low. After the SPI read of the position the SPI_INT\ pin is brought back to a high state again.

Position/Angle Data Read Out (direct_adc = 0)

There are two modes of operation determined by the “spi_int_edge” parameter:

Level sensitive interrupt (spi_int_edge = 0) provides always latest available data via the “pos_out[15:0]” register. If during the SPI transmission a new position becomes available, the SPI_INT\ pin will stay low, to indicate that there is new data available again.



DIAGNOSTICS

The NCV77320 has several diagnostic circuitries to check for errors in the chip and connected coil structure in− and outputs.

Table 18. Diagnostics

Detected Failure	fail_flags[15:0]	V(OUT) Analogue Config	OUT SENT Config	SPI

MEMORY MAP (EEPROM + STATE REGISTERS) CONTENTS TABLES

Table 19. CONFIGURATION MEMORY CONTENT

ADDRESS[5:0]	DATA[15:0] Bit Position	Access	Parameter	Description	Default Value
				… … … …	

Table 19. CONFIGURATION MEMORY CONTENT

ADDRESS[5:0]	DATA[15:0] Bit Position	Access	Parameter	Description	Default Value

Memory CRC Checksum

Memory CRC 16−bit code (CRC−16−DNP) is calculated using polynomial 0x13D65, seed value is 0xFFFF

Polynomial:

+ + + + + + + + +

Table 20. RUN TIME MEMORY CONTENT

ADDRESS[5:0]	DATA[15:0] Bit Position	Access	Parameter	Description	Default Value

APPLICATION SPECIFIC INFORMATION

Application Set−ups for Functional Safety

The NCV77320 has the capability to operate with a second chip to achieve a conclusive position. Several application diagrams can be imagined ranging from ASIL B to a higher functional safety level. In the following pictures some topologies are depicted.

In dual chip configuration, “inp_diag_per” bit shall be programmed differently for each device.

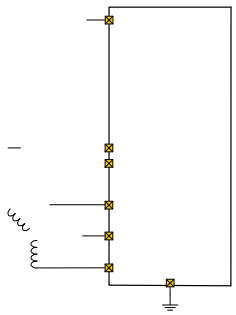


Figure 33. Dual Chip Configuration with Split Supplies and Common Rotor

Figure 34. Dual Chip Configuration with Shared Supplies and Excitation Source with Common Rotor

CRC Calculations Language Examples

SPI CRC 8−bit Code (ATM−8)

Input parameter for function is 32 bit SPI frame with 0x00 at CRC positon (bits [7:0]) of the SPI frame.

```
uint8_t calc_crc_spi(uint32_t data) {          //8-bit CRC with seed 0xFF and polynom 0x107

    uint32_t polynom = 0x10700000 << 3, crc = 0;
    uint8_t shift = 0, roll_back = 0;

    crc = 0xFF000000 | ((data >> 8) & 0x00FFFFFF); //data init
```

CRC Calculation for checksum Nibble of the SENT Frame

```
uint8_t calc_crc_fast_msg(uint32_t data) {     //4-bit CRC with seed 5 and polynom 0x1D

    uint32_t polynom = 0x1D000000 << 3, crc = 0;
    uint8_t shift = 0;

    crc = 0x50000000 | (data & 0x0FFFFFF0);    //data init

    while (shift <= 27) {                      //shift and if 1 perform XOR
        if ((crc & (1 << (31 - shift))) != 0) {
            crc = crc^(polynom >> (shift));
        }
        shift++;
    }
    return crc;
}

//example of use

int main(void) {
    uint32_t SENT_frame = 0x8301F332;          //32 bits, from MSB to LSB: status and comm
    volatile uint8_t result;                   //nbl, data nbl 1 … data nbl 6, CRC nibble
    result = calc_crc_fast_msg(SENT_frame);    //result = 0x02, SENT frame is valid
}
```

SENT Serial Message CRC – Slow Channel

```
ID   = 0x85  =      0b1000 0101
data = 0x2B1 = 0b0010 1011 0001
crc_frame = 0b0000 1100 1000 1010 0100 0110;   //organized according to SENT serial message
                                               //CRC chapter and figure 24 from ID and data

uint8_t calc_crc_slow_msg(uint32_t data) {     //6-bit CRC with seed 0x15 and polynom 0x59

    uint32_t polynom = 0x59000000 << 1, crc = 0;
    uint8_t shift = 0, roll_back = 0;

    crc = 0x15000000 | (data & 0x00FFFFFF);    //data init

    while (shift <= 25) { //shift and if 1 perform XOR
        if ((crc & (1 << (31 - shift))) != 0) {
            crc = crc^(polynom >> (shift));
        }
        shift++;

        if (shift == 6 && roll_back == 0) {    //shift back 6 bits to add 6 zeros at the end
            shift = 0;                         //of the message for proper result
            crc = crc << 6;
            roll_back = 1;
        }
    }
    return crc;
}

int main(void) {               //example of use
    volatile uint8_t result;
    uint32_t crc_frame = 0b000011001000101001000110;
    result = calc_crc_slow_msg(crc_frame);   //result = 0x3D
}
```

Memory CRC 16−bit code (CRC−16−DNP)

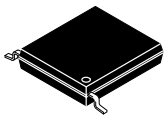
CRC calculation in the chip is starting with seed, then data from MSB of the high address to LSB low address in the chip memory and tailing zeros (e.g. 0xFFFF, data from MSB addr 29 to LSB addr 22 and 0x0000).

```
uint16_t calc_memory_crc16(uint8_t address_start, uint8_t address_end, uint16_t *data) {

    uint32_t polynom = 0x13D65000 << 3, crc;
    uint8_t polynom_shift = 0, current_step = 0, step_count;

    crc = 0xFFFF0000 | data[address_end];                       //data init
    step_count = address_end - address_start + 1;

    do {
        current_step++;
        for (polynom_shift = 0; polynom_shift < 16; polynom_shift++) {
            if ((crc & (1 << (31 - polynom_shift))) != 0) {     //XOR and shifting
                crc = crc^(polynom);
            }b
```



SCALE 2:1

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