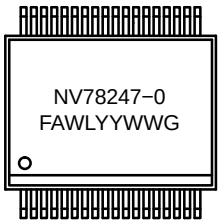
Series String Pixel Controller for Automotive (Front) Lighting

NCV78247



NV78247−0 = Specific Device Code
F = Fab Indicator
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCV78247DQ0AR2G	SSOP36 EP (P−Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Introduction

The NCV78247 is a single−chip pixel controller with embedded switches to control the LEDs in a series LED string, designed for automotive lighting applications and it is in particular designed for high current LEDs. In order to make a pixel light solution, the LEDs needs to be powered by preference with a current source like the NCV78763 or NCV78723/713 or NCV78825 LED drivers. The NCV78247 pixel controller devices receive the pixel control parameters from the pixel light ECU which translates the required light pattern or light image into individual pixel dimming info.

One pixel controller device can control up−to 12 pixels of 1x or 2x or 3x or 4x 1A LEDs per pixel. The maximum LED string voltage has to be limited to 60 V.

If more than 12 pixels need to be controlled, then multiple pixel controllers can be combined in 1 system.

The 12 integrated switches are typically organized as 12 x 1 switch of 1 A, but can be organized in 6 x 2 switches in parallel to offer 6 x 1 switch of 2 A. Besides that a configuration of two strings of 6 LEDs can be supported too, also other variants are possible.

Features

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PACKAGE AND PIN DESCRIPTION

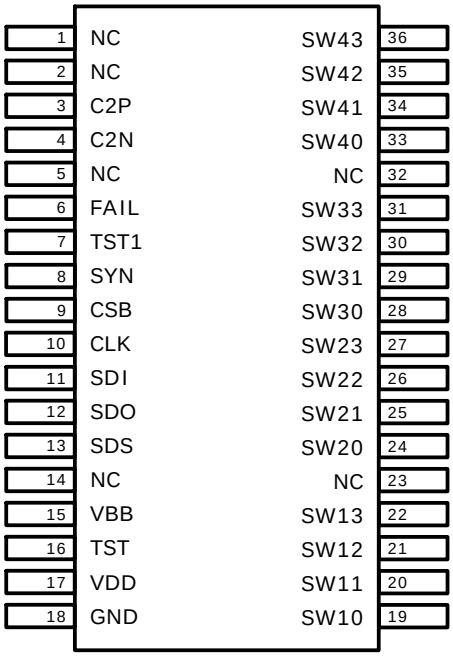
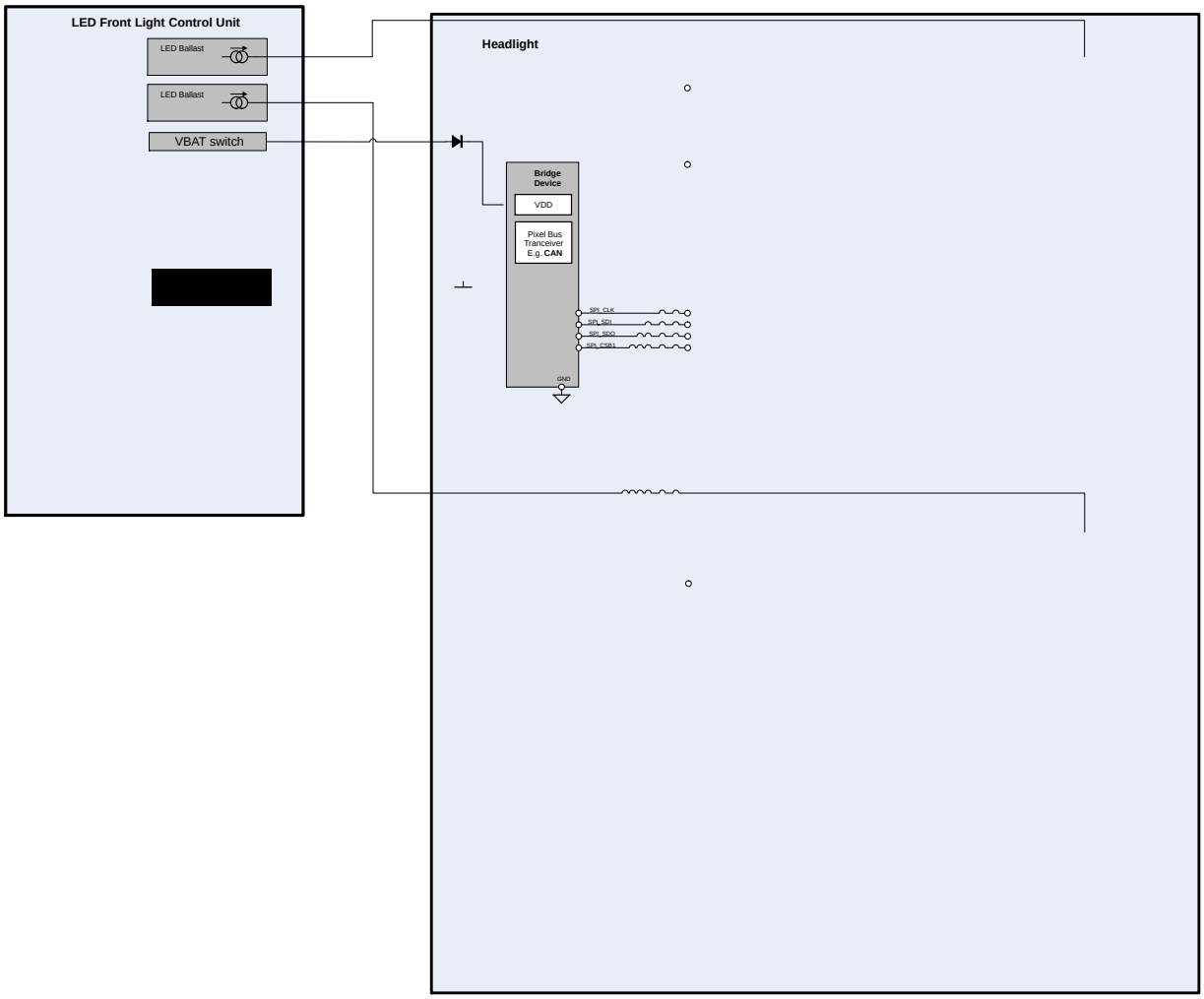


Figure 2. Pin Connections – SSOP36 EP (Top View)

Table 2. PIN DESCRIPTION

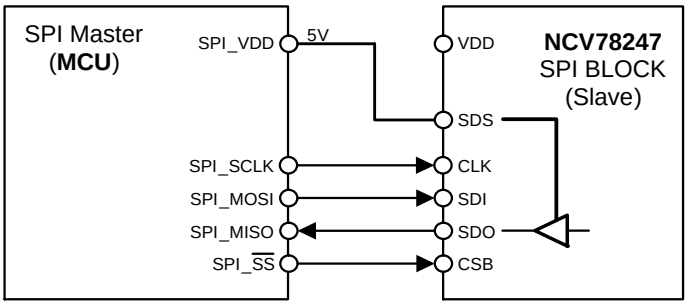
Pin No. SSOP36 EP	Pin Name	Description	I/O Type
1, 2	NC	Not used (to be left floating)	
3	C2P	Switch control capacitor connection	HV in/out
4	C2N	Switch control capacitor connection	HV in/out
5	NC	Not used (to be left floating)	
6	FAIL	Open drain output	HV60 out
7	TST1	Internal function. To be tied to GND or left floating	HV60 in/out
8	SYN	External clock for the dimming synchronization / synchronization between the chips	HV60 in/out
9	CSB	SPI chip select (chip select bar)	HV60 in
10	CLK	SPI clock	HV60 in
11	SDI	SPI data input	HV60 in
12	SDO	SPI data output, push−pull when active CSB otherwise in HiZ	HV60 out
13	SDS	External supply for SDO (can be tied to VDD)	HV60 supply
14	NC	Not used (to be left floating)	
15	VBB	Battery supply	HV60 supply
16	TST	Internal function. To be tied to GND	HV60 in
17	VDD	3V analog and logic supply	LV supply
18	GND	Ground	Ground
23,32	NC	Not used (to be left floating)	
19,24,28,33	SWx0	Power switch to short LED	HV in/out
20,25,29,34	SWx1	Power switch to short LED	HV in/out
21,26,30,35	SWx2	Power switch to short LED	HV in/out
22,27,31,36	SWx3	Power switch to short LED	HV in/out
EP	EP	To be tied to GND	

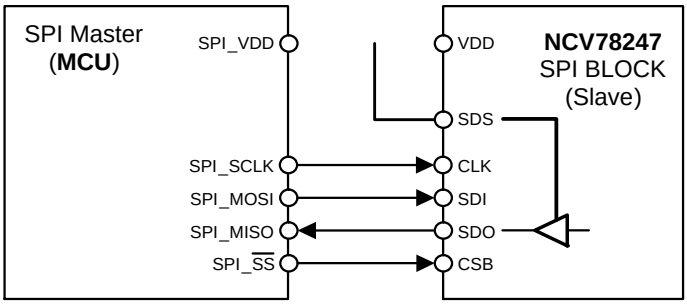
SYSTEM CONFIGURATION



SPI VOLTAGE OPTION

SPI：5V voltage level





SPI：3.3V voltage level (SDS by VDD)

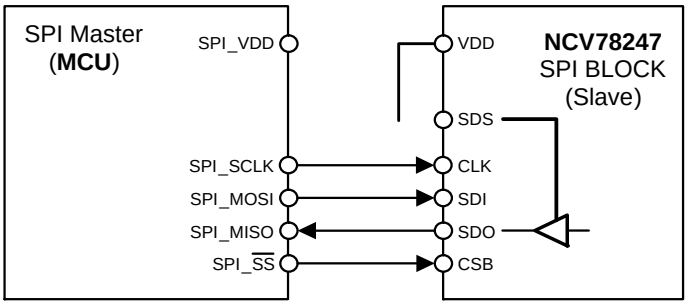


Table 3. ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Min	Max	Unit
Battery Supply voltage (Note 1)	V_{BB}	−0.3	60	V
Low voltage supply (Note 2)	V_{DD}	−0.3	3.6	V
High voltage control IO pins (Note 3)	I_{OHV60}	−0.3	60	V
High voltage IO pins (Note 4)	I_{OHV}	−0.3	68	V
Low voltage supply for switch control: V2 = C2P – C2N	V_2	−0.3	3.6	V
Switch differential voltage (Note 5)	V_{SWxx_DIFF}	−0.3	10	V
Storage Temperature (Note 6)	T_{strg}	−50	150	°C
Junction Temperature (Note 7)	$T_{junction}$	−45	170	°C
Electrostatic discharge on component level Human Body Model (Note 8)				

TYPICAL CURRENT DERATING CURVES

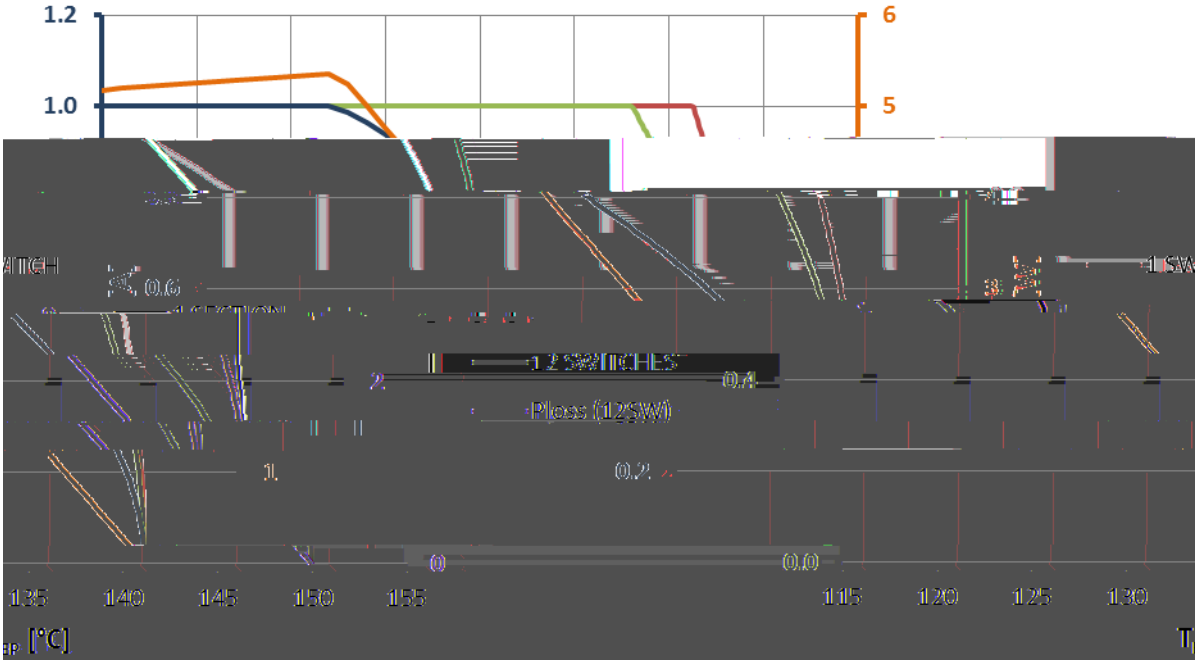


Figure 5. Current Derating Curves

TYPICAL SWITCHES RESISTANCE

Figure 6. Typical Switches Resistance

TYPICAL SECTIONS RESISTANCE

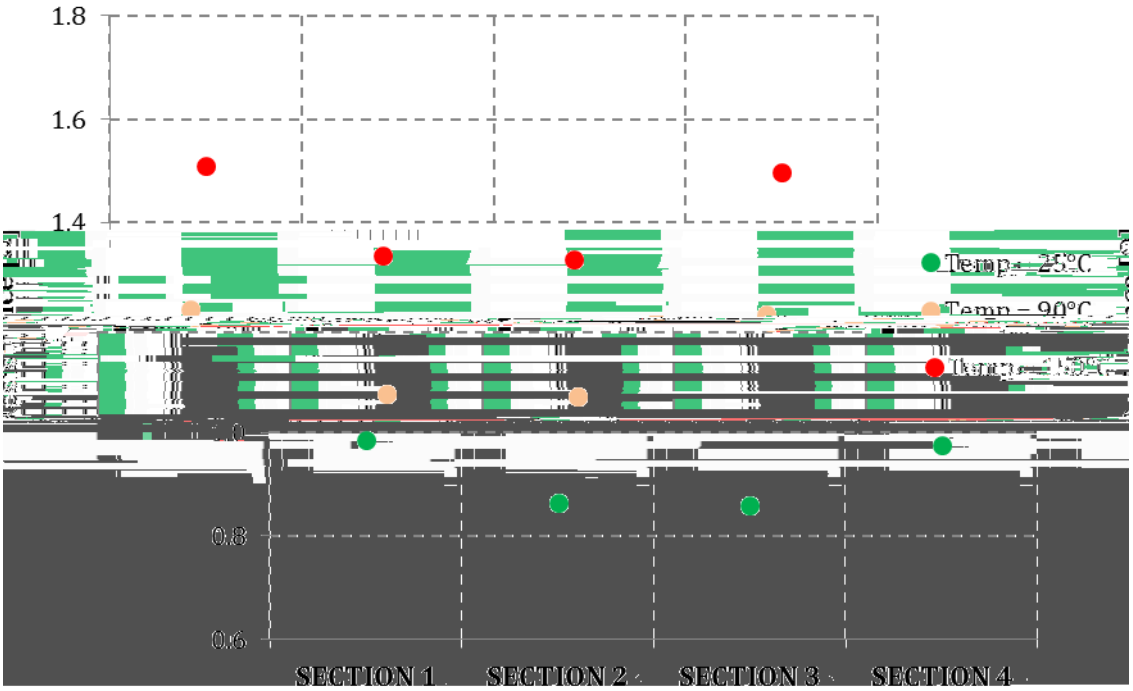
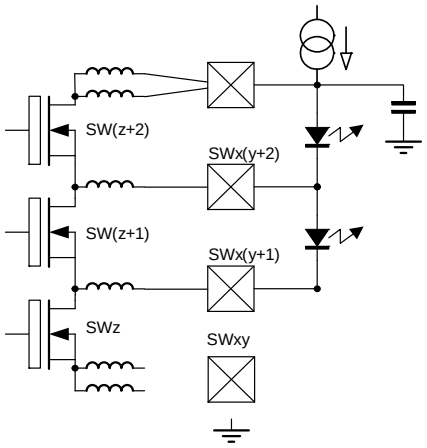


Figure 7. Typical Sections Resistance

EQUIVALENT SCHEMATICS



ELECTRICAL CHARACTERISTICS

DC Parameters

The DC parameters are guaranteed over junction temperature from −40 to 150°C and VBB in the operating range from 5 to 40 V, unless otherwise specified. Convention: currents flowing into the circuit are defined as positive.

Table 6. DC PARAMETERS

Symbol	Pin(s)	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY AND VOLTAGE REGULATOR							
I_{BB}		Total current consumption			6.5	10	mA
VDD		VDD regulator output voltage		3.15	3.45	3.6	V
VDD_ILIM		VDD regulator current limitation		30		150	mA
POR CHARACTERISTICS							
POR3V_H		VDD POR threshold, V_{DD} rising		2.7		2.95	V
POR3V_L		VDD POR threshold, V_{DD} falling		2.5		2.75	V
POR3V_HYST		VDD POR hysteresis			0.2		V
POR_VBB_H		VBB POR threshold, V_{BB} rising		3.8		4.3	V
POR_VBB_L		VBB POR threshold, V_{BB} falling					

Table 6. DC PARAMETERS

Symbol	Pin(s)	Parameter	Conditions	Min	Typ	Max	Unit
TEMPERATURE COMPARATOR							
T_{tc0}		Temperature comparator threshold	<TEMP_THR[2:0]> = 0	70	80	90	°C
T_{tc1}		Temperature comparator threshold	<TEMP_THR[2:0]> = 1	80	90	100	°C
T_{tc2}		Temperature comparator threshold	<TEMP_THR[2:0]> = 2	90	100	110	°C
T_{tc3}		Temperature comparator threshold	<TEMP_THR[2:0]> = 3	100	110	120	°C

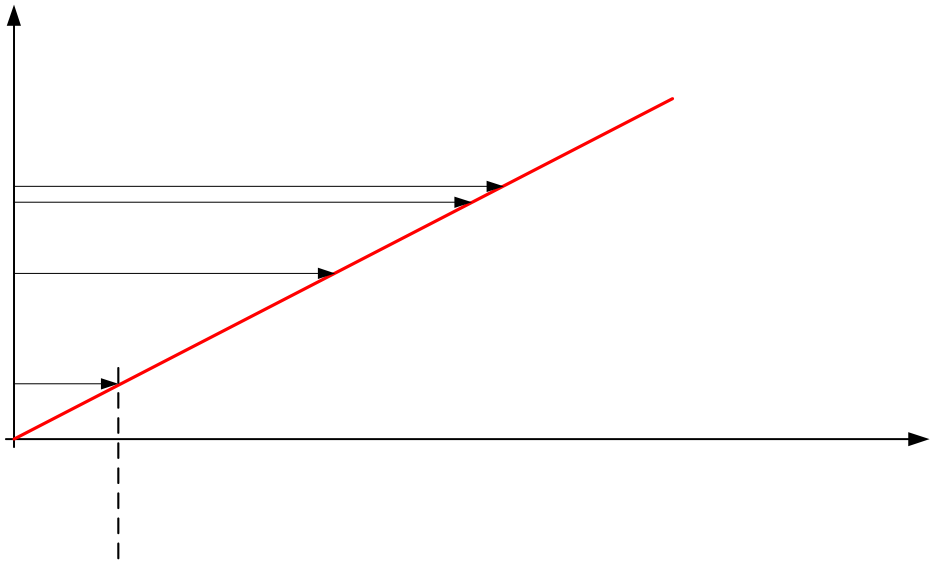
Table 8. SPI INTERFACE

Symbol	Parameter	Min	Typ	Max	Unit
t_{CSS}					

DETAILED OPERATING AND PIN DESCRIPTION

SUPPLY CONCEPT IN GENERAL

Low operating voltages become more and more required due to the growing use of start stop systems. In order to respond to this necessity, the NCV78247 is designed to support power−up starting from VBB = 4.5 V.



Pattern is updated when common PWM counter overflows (CTR[10] = ‘1’) and <MAPENA> = ‘1’. It can happen that switch on event is required on more switches at the same time. However, overlapping switch on events are forbidden, the NCV78247 needs time slot between switch activations (see Table 7), for this reason Transient Vectors are incorporated. When overlapping multiple switch on events are despite this invoked, the <DIMERR> error is raised causing that all switches are switched off, open drain FAIL output goes to HiZ state and processing of invalid pattern is stopped. When overlapping switch off events occurs, the <DIMWARN> status bit is set and processing of this pattern continues. However, it has to be taken into account, that overlapping switch off events can cause big fluctuations of LED string voltage.

The NCV78247 contains 12 channels, so with unique settings of <TRx[3:0]> for each switch 12 different Transient Vector values are needed in the worst case (“0x0” to “0xB”). When <TRx[3:0]> = ‘0xF’, ‘0xE’, ‘0xD’ or ‘0xC, the <TRx[3:0]> is ignored and transition vectors are not applied. In this case the switch status from previous PWM period is kept unchanged until next ON or OFF event into opposite direction.

Value “0xE” (“1110”) in <TR1[3:0]> register is reserved for entrance into Direct switch control mode (more details in Dimming controller chapter).

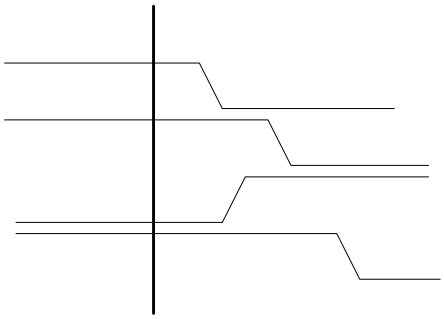


Table 9. SWITCH CONFIGURATIONS

CONF_SEL [3:0]	Conf. Code Name	Description
0000	1, 2, 3, 4	12 x PWM channels
0001	1+2, 3, 4	9 x PWM channels(PWM 1=2)
0010	1+2, 3+4	6 x PWM channels (PWM 1=2 & 3=4)
0011	1, 2+3, 4	9 x PWM channels(PWM 2=3)
0100	1, 2, 3+4	9 x PWM channels(PWM 3=4)
0101	1+2+3+4	3 x PWM channels(PWM 1=2=3=4)
0110	1+2+3, 4	6 x PWM channels(PWM 1=2=3)
0111	1, 2+3+4	6 x PWM channels(PWM 2=3=4)
1000	1+4, 2+3	6 x PWM channels (PWM 1=4 & 2=3)
1001	1+4, 2, 3	9 x PWM channels(PWM 1=4)
OTHERS	RESERVED	Same as 0000, 12 x PWM channels

In case of configurations with 2x, 3x, 4x current, PWM signals of sections with higher index are controlled with PWM signals from lower index sections. For example in case of configuration “0101”, which represents 4x current, the PWM signals of section 1 are controlling section 2, 3 and 4; control signals of section 2, 3 and 4 are ignored.

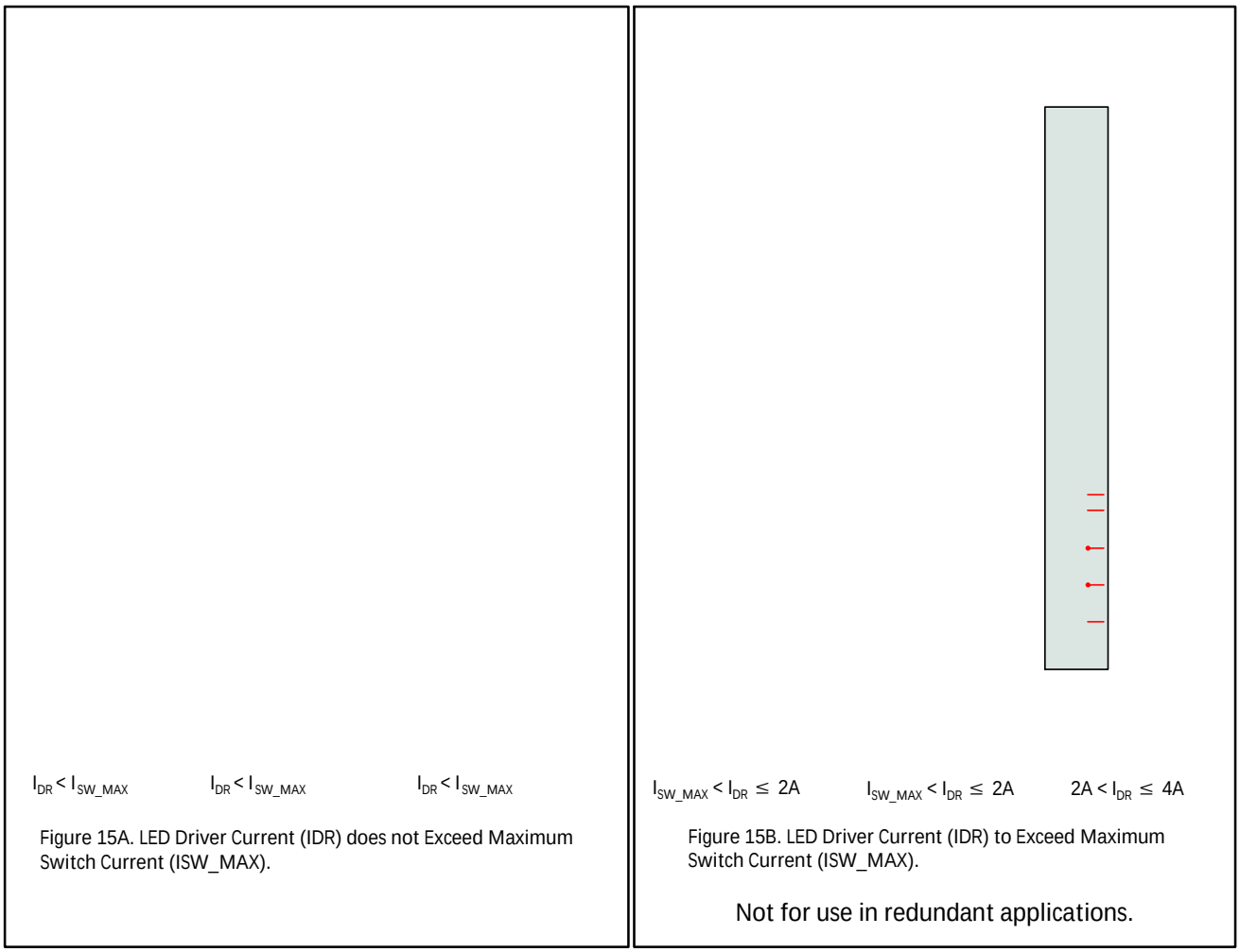


Figure 15A. LED Driver Current (IDR) does not Exceed Maximum Switch Current (ISW_MAX).

Figure 15B. LED Driver Current (IDR) to Exceed Maximum Switch Current (ISW_MAX).

Not for use in redundant applications.

Figure 15. Example of Switch Configurations

PIXEL SWITCHES

Switch ON Process

The switch is gradually opened with a defined slope during T1_CONF[1:0] time.

Short/Open Circuit Detection

Each switch is monitored by a voltage monitor. By monitoring the voltage, and comparing it with the activation status, the following error conditions can be detected:

- Switch OFF and SSH_VTH < V_{SW} < SOV_TH → OK_OFF
- Switch OFF and V_{SW} < SSH_VTH → NOK_SHORT switch is not connected to LED string or switch or LED is shorted.
- Switch OFF and V_{SW} > SOV_TH → NOK_OPEN LED string is opened or LED is broken. Then switch is automatically closed.

During the switching slopes, a blanking time is applied to the above detections of the respective switch in order to avoid false error messages.

The output of the overvoltage comparator is debounced with a debouncing time SOV_DB set by <CMP_DEB> register (see Table 7).

Switch Overvoltage Protection

If the LED pixel voltage is above SOV_TH threshold, the switch is automatically activated and the open switch status is set in the <SWx.STATUS> SPI register. This protects the switch and guarantees that the rest of the LED string still operates properly in case of a LED open failure. Switch is deactivated resp. controllable from PWM again only once open led flag (SWOPN) is cleared by dedicated clear request SPI command. The output of overvoltage comparator is debounced with debouncing time SOV_DB set by <CMP_DEB> register (see Table 7).

FAIL OUTPUT

The open drain FAIL output is forced to GND by the device and goes to HiZ state when the <TSD> is raised or when the device fails to operate (e.g. when V_{DD} supply does not work, etc...) or device is not powered. This guarantees that the LEDs in the LED string are not unintentionally switched on. An external FET must take care that it shorts the full string or that it interrupts the current to the LED string. In the latter case, pre

SPI Address Map

Table 10. SPI ADDRESS MAP

ADDR	R/W	BYTE2[7:0]								BYTE1[7:0]				BYTE0[7:0]
0x00	R/W	ON1.9	ON1.8	ON1.7	ON1.6	ON1.5	ON1.4	ON1.3	ON1.2	ON1.1	ON1.0	OFF1.9	OFF1.8	

Register Description

ONx[9:0] – time of ON event.

OFFx[9:0] – time of OFF event.

TRx[3:0] – Transition vector duration, it is prolonging the duration of ON resp. OFF value at the end of PWM period by <TRx[3:0]> x Time slot between switch activations (see Table 7). It is applied in case of pixel pattern update (when the common PWM counter overflows (CTR[10] = '1') and <MAP_ENA> = '1'). When <TRx[3:0]> = '0xF', '0xE', '0xD' or '0xC, the <TRx[3:0]> is ignored and transition vectors are not used. <TRx[3:0]> setting is unique for each switch. Transition vectors are applied only in case of 100% or 0% duty cycle when rising edge is detected on <SWENA> register or when duty cycle change from negative pulse (ON time > OFF time) to positive pulse (ON time < OFF time) resp. from positive pulse (ON time < OFF time) to negative pulse (ON time > OFF time) is detected. If <TRx[3:0]> is not applied, switch status from previous PWM period is kept unchanged until next ON resp. OFF event into opposite direction.

T1_CONF[1:0] – configuration of switch on time.

T1_CONF[0] bit configures the switch soft slope time (slope control), see parameter Switch soft slope time in Table 7).

T1_CONF[1] bit defines the switch on time (switching slope), see parameter Switch on time (switching slope) in Table 7).

Configuring of <T1_CONF[1:0]> register while <SWENA> = '1' should be avoided.

STRING_GND_DET_ENA[3:0] – these bits are enabling/ disabling the GND loss detection for the four switch strings. When <STRING_GND_DET_ENA[x]> = '1', GND loss detection is enabled for selected string<x>, otherwise GND loss detection for string<x> is disabled.

CTRL_FAIL_B – when <CTRL_FAIL_B> = '0', open drain FAIL output goes to HiZ state and all switches are switched off and <SWENA> = '0' independently of indicated failures. Open drain FAIL output goes to HiZ state immediately. Forcing of open drain FAIL output to GND is delayed by one full PWM period to avoid LED flickering during start−up or recovery from HW error.

CMP_DEB – defines the over−voltage (SOV_DB) comparator debounce times. Typical debounce time is 10 μs ("0") and 15 μs ("1"). Configuring of <CMP_DEB> register while <SWENA> = '1' should be avoided.

DIMFREQ[2:0] – defines the DIMCLK frequency when DIMSRC = '1', encoding is as defined below:

0x0 − 125 kHz
0x1 − 250 kHz
0x2 − 500 kHz
0x3 − 1 MHz

<DIMFREQ[2]> is spare, it is reserved for future extensions.

Configuring of <DIMFREQ[2:0]> register while <SWENA> = '1' should be avoided.

TEMP_THR[2:0] – temperature thresholds can be configured via register, encoding is as defined in Table 6.

CONF_SEL[3:0] – selects the switch configuration. NCV78247 supports the switch configurations listed in

TEMPOUT – output of temperature comparator (controlled by <TEMPTHR[2:0]>). TEMPOUT is high when Tj is above <TEMP_THR[2:0]>.

REVID[7:0] – NCV78247 revision ID to track silicon mask version.

Warning, Error Detection and Diagnostics Feedback

The NCV78247 offers a wide range of device−integrated diagnostic features. Their description follows.

Thermal Warning and Shutdown

Thermal warning is trimmed in production to 160°C. Thermal Warning (TW) detects a junction temperature which is very close to the Thermal Shutdown level. When Thermal Warning is detected (<TW> = '1'), the SPI register <TW> is set. SPI <TW> register is cleared once it has been read−out by SPI Master.

Thermal shutdown is trimmed in production to 170°C (±5°C). Thermal Shutdown (TSD) detects that a junction temperature has reached the Thermal Shutdown level. When Thermal Shutdown is detected (TSD = '1'), the TSD flag is latched in the SPI <TSD> register and stays set until the SPI <TSD> register is read by the SPI Master and condition for thermal shutdown disappear.

When Thermal Shutdown is detected, open drain FAIL output goes to HiZ state and all switches are switched off. Normal operation is restored when temperature decreases below thermal warning level and <TW> and <TSD> flags are cleared, hereby providing hysteresis for TSD recovery process.

On chip Temperature Measurement

On top of the TSD and the TW there is available temperature comparator output observable via SPI <TEMPOUT> flag. Temperature thresholds for this comparator can be configured via <TEMP_THR[2:0]> register. All possible settings of temperature thresholds are summarized in Table 6.

SPI Framing Error

The SPIERR is raised when SPI frame contains less than (or more than) expected number of data bits **(**number of bits other than 32) during active CSB or when SPI CRC error is detected.

Overlapping Switch ON/OFF Events

Overlapping switch on events is forbidden, the NCV78247 needs time slot between two switch on events (see Table 7). Superior system has to ensure that overlapping switch on events do not present in patterns.

When overlapping switch on events are despite this invoked, the NCV78247 incorporates protective feature, in which the <DIMERR> error is raised causing that open drain FAIL output goes to HiZ state, all switches are switched off and processing of invalid pattern is stopped.

When overlapping switch off events occur, the <DIMWARN> status bit is set and processing of this pattern continues. However, it has to be taken into account, that overlapping switch off events can lead to big fluctuations of LED string voltage.

Pixel Switches Diagnostic

Embedded diagnostic covers a wide range of possible failure situations on switches. Each switch contains two comparators – short comparator and over voltage comparator. With the help of these two comparators a several fail situations can be detected and distinguished on each switch individually, for more detail description see

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