NCV78663


VBB

Table 1. PIN DESCRIPTION

Pin#	Pin Name	IO Type	Function
29	VINBCK1	HV in	Buck 1 high voltage supply
30	IBCK1SENSE −	HV in	Buck 1 negative sense input
31	IBCK1SENSE+	HV in	Buck 1 positive sense input
32	N.C.		Not used (can be connected to GND)
33	VBOOST	HV supply	High voltage feedback input
34	VBOOSTM3V	HV IO	VBOOST −3V output
35	IBSTSENSE −	LV IO	Battery current negative feedback input
36	IBSTSENSE+	LV IO	Battery current positive feedback input

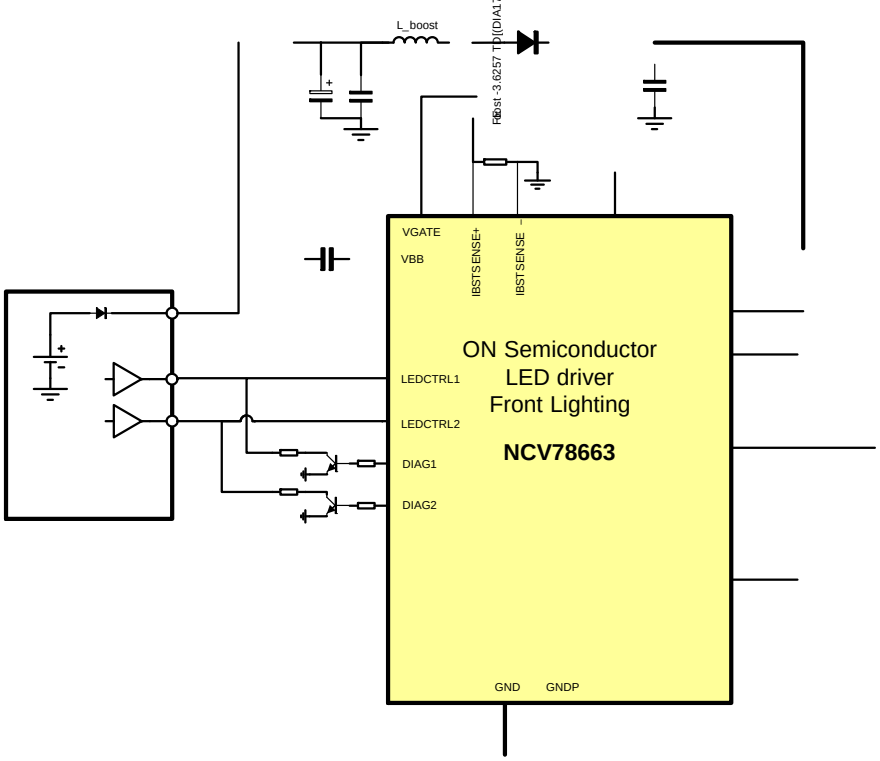


Figure 3. NCV78663 Application Circuit

1. As reported in the application diagram, the device pins TEST1 and TEST2 must be connected to ground.
2. For details about PCB layout, please refer to the dedicated section.
3. RF1 and RF2 resistors typical value is 2.2 kΩ and minimum required value is 1 kΩ. It is recommended not to exceed a value of 22 kΩ in order not to alter the VLED sampled value.

Table 4. THERMAL RESISTANCE

Characteristic	Package	Symbol	Max	Unit
Thermal resistance junction to exposed pad	SSOP36	θ_{JCbot}	3.49	KW [1]

ELECTRICAL CHARACTERISTICS

Table 8. VBOOSTM3V: HIGH SIDE AUXILIARY SUPPLY

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
VBSTM3 regulator output voltage	VBSTM3	Referenced to VBOOST	3.6	3.3	2.9	V
Output current limitation	Ilim_VBOOSTM3V				200	mA
Typical VBSTM3 decoupling capacitor	C_VBSTM3	Referenced to VBOOST		0.47	4.7	μF
	ESR	Referenced to VBOOST			200	mΩ

Table 9. OSC4M: SYSTEM OSCILLATOR CLOCK

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
System oscillator frequency	FOSC4M					

Table 11. BOOSTER

Name	Symbol	Conditions	SPI/OTP SETTING	Normal Regulation Window (Note 18)			SHUTDOWN	Unit
				NREGL	TRGT	NREGH	MAX	

Table 11. BOOSTER (continued)

Name	Symbol	Boost_ctrl_rate [2:0]				
		OTP Setting Only	Min	Typ	Max	Unit
Booster control rate	Boost_ctrl_rate	[011]	−12.5%	86	+12.5%	μs
		[010]		144		
		[001]		240		
		[000]		400		
		[111]		667		
		[110]		1111		
		[101]		31		
		[100]		52		

Table 12. BOOSTER PRE−DRIVER

Name	Symbol		Min	Typ	Max	Unit
High side switch impedance	RONHI			2.5	4	Ω
Low side switch impedance	RONLO			2.5	4	Ω

Table 13. BOOSTER − CURRENT LIMITATION

Name	Symbol		Min	Typ	Max	Unit
Current limitation threshold voltage	VLIMTH	Over full operating range	78	100	122	mV
	VLIMTH_hot	At T_J = 160 °C	85	100	115	mV
Threshold voltage hysteresis	VLIMHYS		5	10	20	mV
Sense voltage common mode range	CMVSENSE		−1		1	V

Table 14. ON−CHIP TEMPERATURE SENSOR

Name	Symbol		Min	Typ	Max	Unit
Thermal shut down level (junction temperature)	TSD		163	169	175	°C

Table 16. BUCK REGULATOR − CURRENT REGULATION

Name	Symbol		Min	Typ	Max	Unit
Current sense comparator threshold voltage setpoint (= end of the BUCK ON phase) MIN value	VThreshold_MIN	Name				

Table 22. DIMMING INTERFACE

Name	Symbol		Min	Typ	Max	Unit
Input dimming frequency	FDIMMING		50	1000	8000	Hz
Dimming signal input measurement and output reconstruction resolution	DIMres_IN_OUT			10		µs
Dimming Frequency Factor (= Output dimming frequency / input dimming frequency)	DFF[2:0]	SPI/OTP setting [100]		1		
		SPI/OTP setting [101]		2		
		SPI/OTP setting [110]		3		
		SPI/OTP setting [111]		4		
		SPI/OTP setting [000]		5		
		SPI/OTP setting [001]		6		
		SPI/OTP setting [010]		7		
		SPI/OTP setting [011]		8		

ADC

General

The built−in analog to digital converter (ADC) is an 8−bit capacitor based successive approximation register (SAR).

This embedded peripheral can be used to provide the following measurements to an external Micro Controller Unit (MCU):

- VBOOST voltage
- VBB voltage
- VLED1, VLED2 voltages
- VTEMP_AGP1, VTEMP_AGP2 voltages

The internal NCV78663 ADC state machine samples all the above channels automatically, taking care for setting the analog MUX and storing the converted values in memory. The device LED diagnostics and the digital boost controller make use of the values as inputs.

To remark that the VLEDx (1, 2) lines are sampled only when the respective LED output is activated and the last sampled value is kept, until it is overwritten (refreshed) by a new one.

An external MCU can read−out all measured values via the SPI interface in order to take application specific decisions. Please note that the MCU SPI commands do not interfere with the internal ADC state machine sample and conversion operations: the MCU will always get the last available data at the moment of the register read.

Each new boost voltage sample occurs at 17 μs worst case rate. VLED1 and VLED2 voltages are typically sampled at a rate of about 52 μs (when the buck switches are on), while VTEMP_AGP1 and VTEMP_AGP2 are continuously sampled at a rate of 4 ms. The battery voltage is sampled typically each 108 μs.

ADC Channel Selection

The ADC channel selection readout is done via the SPI-CR11 register (the part “ADC_Sel” behaves as a pointer to the requested data), while the SPI−SR3 registers will hold the data (see section SPI Address Map). When polling the same channel over time, there is no need to refresh the address field, as the SPI−SR3 register will be automatically refreshed with the latest available data.

ADC_SEL[2:0]	VBOOST	VBB	VLED1	VLED2	VTEMP_AGP1	VTEMP_AGP2
000	1	0	0	0	0	0
001	0	1	0	0	0	0
010	0	0	1	0	0	0
011	0	0	0	1	0	0
100	0	0	0	0	1	0
101	0	0	0	0	0	1
110	Do not select					
111	Do not select					

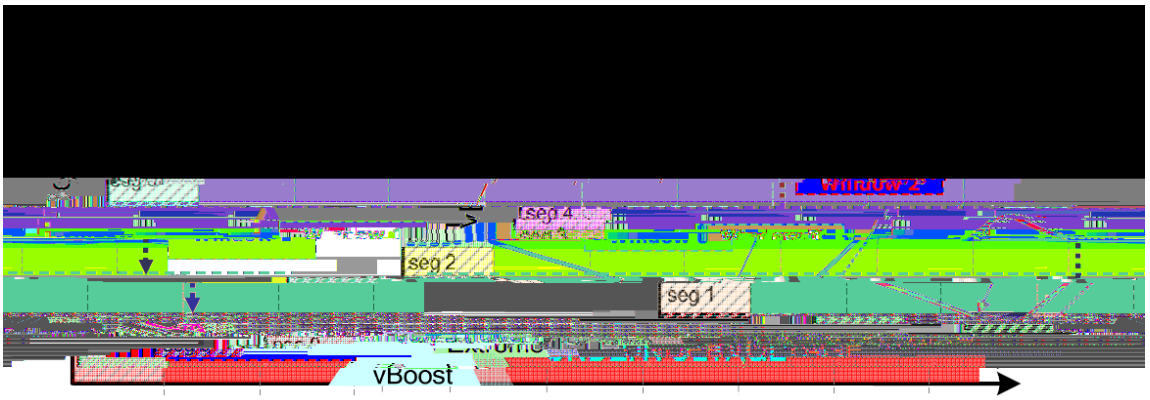


Figure 10. NCV78663: Boost Voltage Possible Behavior at First Full Power Load Activation

In order to guarantee the regulation in WINDOW 1 throughout operating conditions and dimming, a total boost capacitance Cboost ≥ 50 μF is recommended for medium to high application power. For further details about capacitance sizing, please refer to application notes.

Please note that the boost voltage regulation loop is not affected whether a continuous or discontinuous mode of operation (E.G. low dimming duty cycle) is taking place.

Booster PWM Frequency

The booster controller is working with a constant frequency and variable duty cycle to control the booster voltage.

The operating frequency is user selectable with three SPI/OTP setting bits (Section OSC16M Clock), in order to optimize the booster inductor's size and EMC aspects.

Booster Disable Function

In some cases, it is useful to disable the booster by means of the BOOSTER_DIS bit. For instance if:

-

$$f_{BUCK} = \frac{V_{BOOST} - V_{LED}}{V_{BOOST}} \cdot \frac{1}{T_{OFF}} =$$

$$= \frac{V_{BOOST} - V_{LED}}{V_{BOOST}} \times \frac{V_{LED}}{T_{OFF\_V\_BUCK}}$$

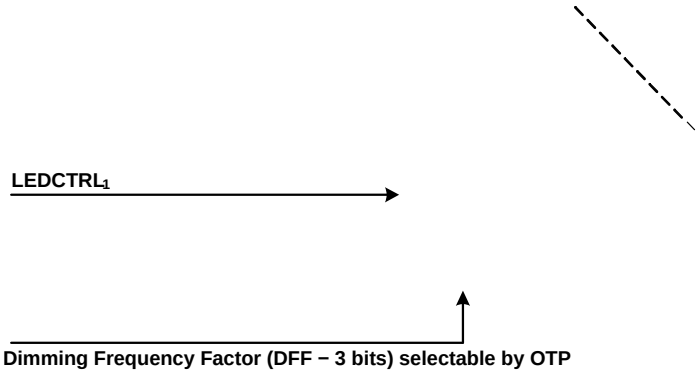
DIMMING

The chip supports both analog and digital or PWM dimming. Analog dimming is done by controlling the LED current during operation. This can be done by means of changing the peak current level and/or the Toff_V constants (see Buck Regulator − Current regulation) by SPI commands.

In this section, we only describe the PWM dimming as this is the preferred method to maintain the desired LED color temperature for a given current rating.

In digital dimming, the LED current waveform frequency is constant and the duty cycle is set according to the required light intensity. The two independent control inputs LEDCTRLx handle the dimming signals for the related channel. More details in the following section.

Dimming Control Scheme



required. Vice versa, starting from a 100% duty cycle condition, in order to detect a 0% input signal (LEDx

♦

SPI ADDRESS MAP

Table 26. SPI BANK REGISTER SUMMARY

SPI Address	POR Value	Access	7	6	5	4	3	2	1	0
0x00	0x00	–	NOP							
0x01	0x00	R/W	**Control Register 1**							
			Dimming Duty Factor LED string 1 [7:0]							
0x02	0x00	R/W	**Control Register 2**							
			Dimming Duty Factor LED string 2 [7:0]							
0x03	0x00	R/W**	**Control Register 3**							
			OTPLockInt**	Current setting LED string 1 [6:0]						
0x04	0x00	R/W**	**Control Register 4**							
			OTPLockExt**	Current setting LED string 2 [6:0]						
0x05	0x00	R/W	**Control Register 5**							
			LED string 1 diagnostics individual short threshold [7:0]							
0x06	0x00	R/W	**Control Register 6**							
			LED string 2 diagnostics individual short threshold [7:0]							
0x07	0x00	R/W	**Control Register 7**							
			BOOSTER_DIS	Booster oscillator frequency [2:0]			Booster output range [3:0]			
0x08	0x00	R/W	**Control Register 8**							
			Toff 1 range selection [3:0]				PWRDERATE_DIS	Dimming frequency factor [2:0]		
0x09	0x00	R/W (*TEST)	**Control Register 9 / OTP_Ctrl [7:0]**							
			OTP_Start*	OTP_Cmd [1:0]*		Reserved*	OTP_Addr [3:0]*			
0x0A	0x00	R/W (*TEST)	**Control Register 10**							
			OTP_Data [7:0]*							
0x0B	0x00	R/W (*TEST)	**Control Register 11 / AdcCtrl [7:0]**							
			Reserved*	Toff 2 range selection [3:0]				ADC_Sel [2:0]		
0x0C	0x00	R	**Status Register_1**							
			Parity bit	BoostUV	DCmax	PWRderate	OpenLED1	ShortLED1	IndShortLED1	OCLED1
0x0D	0x00	R	**Status Register_2**							
			Parity bit	TW	TSD	SpiErr	OpenLED2	ShortLED2	IndShortLED2	OCLED2
0x0E	0x00	R	**Status Register_3**							
			ADC [7:0]							
0x0F	0x00	R/W (*TEST)	**Test Command(write) / RevID(read)**							
			RevID [7:0] (Note 20)							

Mapped in both, SPI and OTP address maps (with different address)

*Registers with write possibility only in TEST mode (TEST1 pin = high)
**Read only registers as exception
A detailed description of the SPI registers follows in the next section.
20. RevID = 7dec (= [111] bin) for QAA silicon, RevID =6dec (= [110] bin) for PAA silicon (register 0x0F).

Name	Control Register 5 /CR5 : LED String 1 Diagnostics Individual Short Threshold						
7	6	5	4	3	2	1	0
Reset Value:							
0	0	0	0	0	0	0	0
Reset Source: nReset							
Address:	05h		Access:	R/W			
Bit	Name	Description					
7...0	ShortThr1[7:0]	LED String 1 diagnostics individual short threshold.					

Name	Control Register 6 /CR6 : LED String 2 Diagnostics Individual Short Threshold						
7	6	5	4	3	2	1	0
Reset Value:							
0	0	0	0	0	0	0	0
Reset Source: nReset							
Address:	06h		Access:	R/W			
Bit	Name	Description					
7...0	ShortThr2[7:0]	LED String 2 diagnostics individual short threshold.					

Name	Control Register 7 /CR7 : Booster Output Range / Booster Oscillator Frequency						
7	6	5	4	3	2	1	0
Booster DIS	Booster oscillator frequency						

Name	Control Register 9 /CR9/ : OTP Control						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OTP_Start	–	OTP_Cmd[1:0]		OTP_Addr[3:0]			
Reset Value:							
0	x	0	0	0	0	0	0
Reset Source: nReset/TEST							
Address:	**09h**		**Access:**	**R/W* (in Test mode)**			

Bit	Name	Description
7	OTP_Start	To write in this registers TEST pin needs to be set to ’1’. Set of OTP_Start bit executes the selected command written in OTPCtrl [1:0] bits.
6...5	OTP_Cmd[1:0]	To write in this registers TEST pin needs to be set to ’1’. “00” Point to OTP cell (read OTP without SPI registers refresh) “01” Read OTP. Refresh OTP/SPI and provides for reading from OTP_DATA [7:0] “10” Load OTP. Take data from OTP_DATA [7:0] and shift them in the OTP chain at the OTP_Addr [3:0] address, for emulation. “11” Zap OTP. Take data from OTP_DATA [7:0] and zaps! the OTP, one bit at a time at OTP_Addr [3:0] address.
4	Reserved	Reserved bit. To be kept to zero in the application.
3...0	OTP_Addr[3:0]	Pre defined OTP address to be accessed by the OTP_Cmd [1:0] command.

Name	Control Register 10 /CR10/ : OTP Data						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OTP_Data[7:0]							
Reset Value:							
0	0	0	0	0	0	0	0
Reset Source: nReset							
Address:	**0Ah**		**Access:**	**R/W**			

Bit	Name	Description
7...0	OTP_Data [7:0]	Data used in case of OTP Load/Zap operation. In case the register is accessed for reading, data is taken directly from OTP_Addr [3:0] address.

Name	Control Register 11 /CR11: ADC Control						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADC_Tst_En	Toff 2 range selection [3:0]				ADC_Sel [2:0]		
Reset Value:							
0	0	0	0	0	0	0	0
Reset Source: nReset							
Address:	**0Bh**		**Access:**	**R/W**			

Bit	Name	Description
7	Reserved	

Name	Status Register 2 /SR2: LED2 Status							
7	6	5	4	3	2	1	0	

OTP

Description

The OTP (One Time Programmable) Memory contains 109 bits; 37 bits are for trimming purposes and are programmed at the end of the silicon manufacturing line at ON Semiconductor. The remaining 72 bits are system dependent parameters and are user programmable via the SPI interface and the “ZAP!” operation: these should be considered as the power−up default operating parameters and are typically programmed at the end of the module manufacturing line.

The OTP−

P Lock

OTPLockExt allows the user to protect the system t parameters which are typically programmed at f the module manufacturing line. These parameters will be the system default parameters after power−up. We strongly recommend making use of this lock to avoid unwanted setting changes in the application and to keep TEST1 to GND.

OTP ADDRESS MAP

OTP Address	Bit N	7	6	5	4	37cc8p8 .907ef99n1of th06oPnb79283.408 660.526 71.774E

PCB LAYOUT RECOMMENDATIONS

This section contains instructions for the NCV78663 PCB layout application design. Although this guide does not claim to be exhaustive, these directions can help the developer to reduce application noise impact and insuring the best system operation.

The areas which are most critical for a layout point of view are highlighted in the following picture:

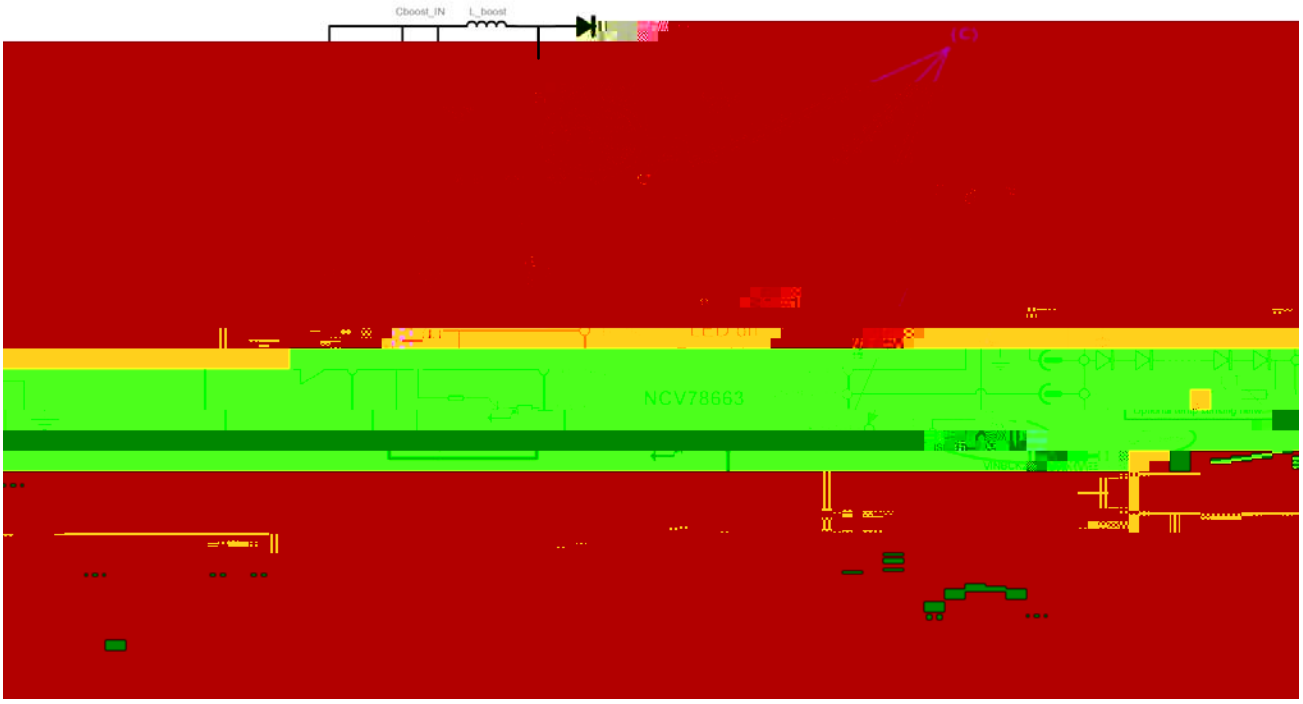


Figure 18. NCV78663: Application Critical Areas at PCB Level

Booster Current Limitation Circuit: AREA (A)

The booster limitation circuit relies on a low voltage comparator, which triggers with respect to the sense voltage across the external resistor Rboost_sense. In order to maximize power efficiency, the threshold voltage is set to a rather low value by design (typical 100 mV, see Table 13) and this area may be affected by the MOSFET switching noise if no specific care is taken. The following recommendations are given:

A. Use a four terminals current sense method as depicted in the figure below. The measurement PCB tracks should run in parallel and as close as possible to each other, trying to have the same length. The number of vias along the measurement path should be minimized;
B. Place Rboost_sense sufficiently close to the MOSFET source terminal;
C. The MOSFET's dissipation area should be stretched in a direction away from the sense resistor to minimize resistivity changes due to heating;
D. Possibly reduce to the least the distance between Rboost_sense and the NCV78663 boost limitation comparator's inputs (IBSTSENSE+ and IBSTSENSE−);
E. If the current sense measurement tracks are interrupted by series resistors or jumpers (once as a maximum) their value should be matched and low ohmic (pair of 0 Ω to 47 Ω max) to avoid errors due to the comparator input bias currents;
F. Avoid using the board GND as one of the measurement terminals as this would also introduce errors.

Figure 19. Four Wires Sensing Method for Boost Current Limitation Comparator

Buck Current Comparators: AREAs (B1) and (B2)

The blocks (B1) and (B2) control the buck peak currents by means, respectively, of the external sense resistors Rbuck_1_sense and R_buck_2_sense. As the regulation is performed with a comparator, the considerations explained in the previous section “Booster Current Limitation Circuit: AREA (A)” remain valid.

In particular, the use of a four terminals current sense method is required, this time applied on (IBCK1xSENSE+, IBCKxSENSE−). The sensing PCB tracks should be kept as short as possible, with the sense resistors close to the device, but preferably outside of its PCB heating area in order to limit measurement errors produced by temperature drifts.

Vboost Related Tracks: AREA (C)

The three NCV78663 device pins VBOOST, IBCK1SENSE+ and IBCK2SENSE+ must be at the same individual voltage potential to guarantee proper functioning of the internal buck current comparator (whose supply rails

GND Connection: AREA (D)

The NCV78663 GND and GNDP pins must be connected together. It is suggested to perform this connection directly close to the device, behaving also as the cross-junction between the signal GND (all low power related functions) and the power GND (related to all power switching areas). The device exposed pad should be connected to the GND plane for dissipation purposes.

ORDERING INFORMATION

Device	Package	Shipping†
NCV78663DQ0G	SSOP36 EP (Pb Free)	47 Units / Rail
NCV78663DQ0R2G	SSOP36 EP (Pb Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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