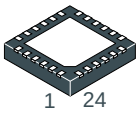
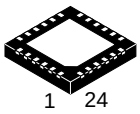
High Efficiency Buck Dual LED Driver with Integrated Current Sensing for Automotive Front Lighting

NCV78723

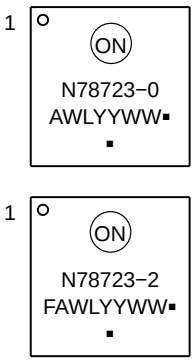


QFN24
CASE 485CS



QFNW24
CASE 484AF

MARKING DIAGRAMS



N78723−0	= Specific Device Code
N78723−2	= Specific Device Code
F	= Fab Indicator
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 31 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 31.

The NCV78723 is a single-chip and high efficient Buck Dual LED Driver designed for automotive front lighting applications like high beam, low beam, DRL (daytime running light), turn indicator, fog light, static cornering, etc. The NCV78723 is in particular designed for high current LEDs and provides a complete solution to drive 2 LED strings of up-to 60 V. It includes 2 independent current regulators for the LED strings and required diagnostic features for automotive front lighting with a minimum of external components – the chip doesn't need any external sense resistor for the buck current regulation. The available output current and voltages can be customized per individual LED string. When more than 2 LED channels are required on 1 module, then 2, 3 or more devices NCV78723 can be combined; also with NCV78713 device – the derivative of the NCV78723 incorporating Buck Single LED Driver. Thanks to the SPI programmability, one single hardware configuration can support various application platforms.

Features

- Single Chip
- Buck Topology
- 2 LED Strings up-to 60 V
- High Current Capability up to 1.6 A DC per Output
- High Overall Efficiency
- Minimum of External Components
- Integrated High Accuracy Current Sensing
- Integrated Switched Mode Buck Current Regulator
- Average Current Regulation through the LEDs
- High Operating Frequencies to Reduce Inductor Sizes
- Low EMC Emission for LED Switching and Dimming
- SPI Interface for Dynamic Control of System Parameters
- Fail Safe Operating (FSO) Mode, Stand-Alone Mode
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- High Beam
- Low Beam
- DRL
- Position or Park Light
- Turn Indicator
- Fog
- Static Cornering

TYPICAL APPLICATION SCHEMATIC

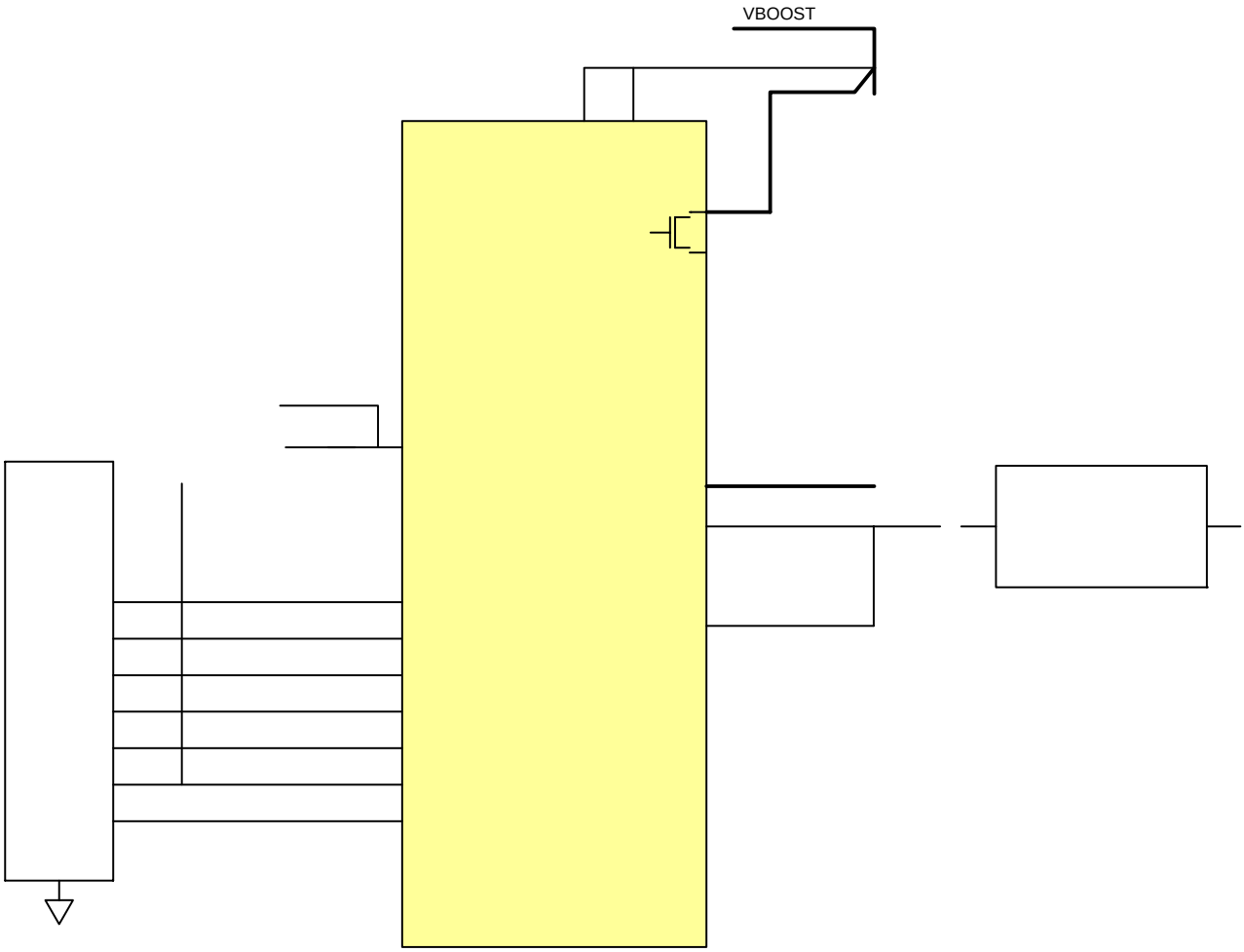


Figure 1. Typical Application Schematic

BLOCK DIAGRAM

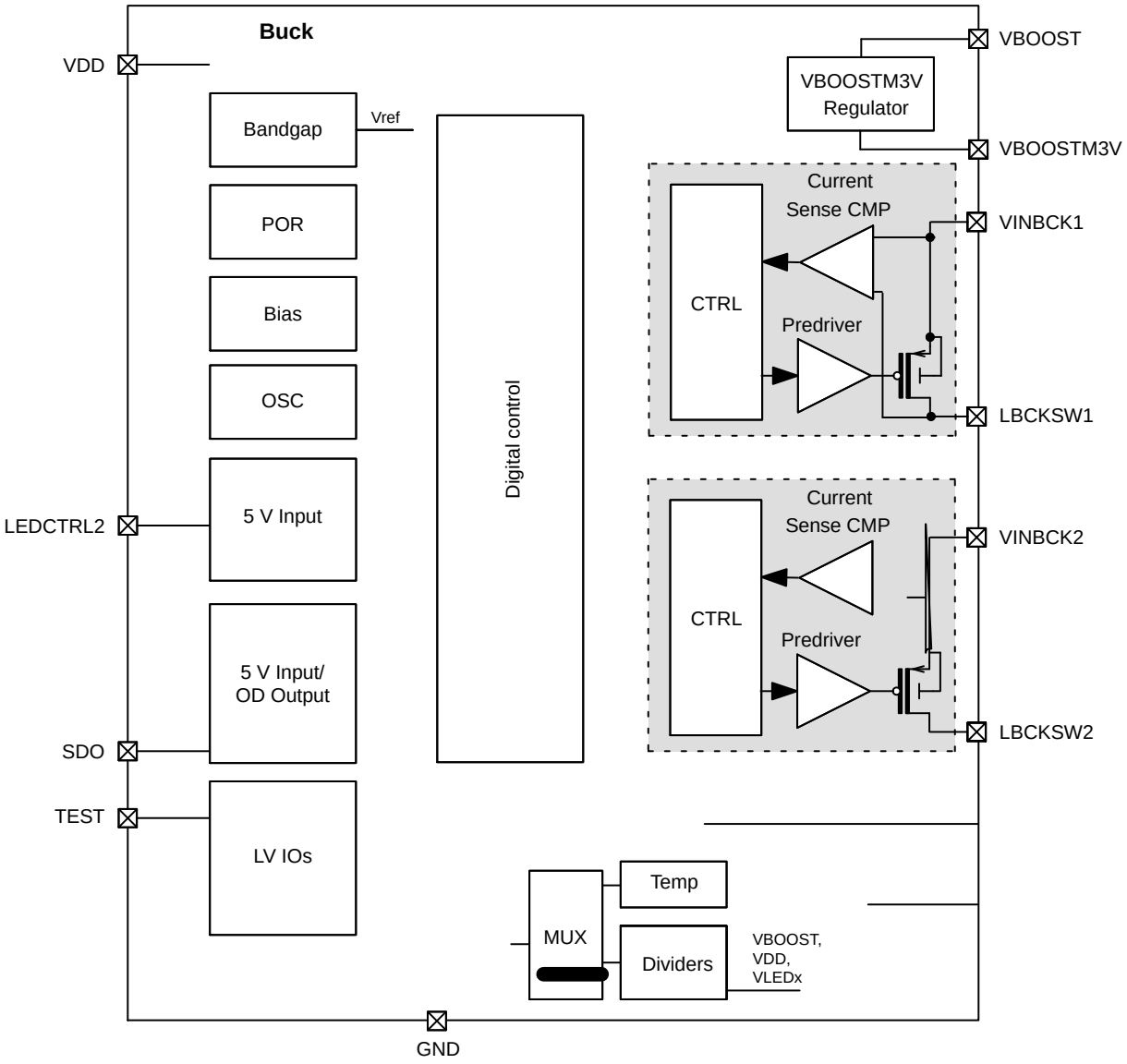


Figure 2. Block Diagram

PACKAGE AND PIN DESCRIPTION

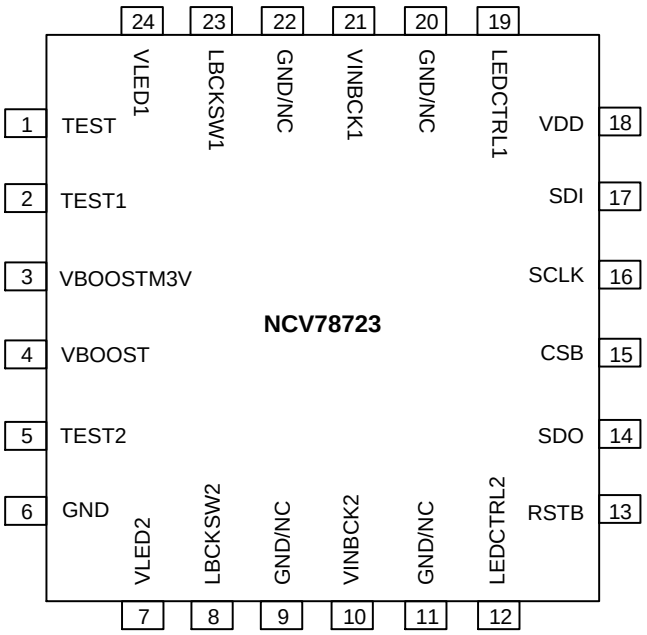


Figure 4. Pin Connections

Table 2. PIN DESCRIPTION

Pin No.	Pin Name	Description	I/O Type
1	TEST	Test Pin	LV In
2	TEST1	Test Pin	LV IN/OUT HV Tolerant
3	VBOOSTM3V	VBOOSTM3V Regulator Output Pin	HV OUT (Supply)
4	VBOOST	Booster Input Voltage Pin	HV Supply
5	TEST2	Test Pin	LV IN/OUT HV Tolerant
6	GND	Ground	Ground
7	VLED2	LED String 2 Forward Voltage Sense Input	HV IN
8	LBCKSW2	Buck 2 Switch Output	HV OUT
9, 11, 20, 22	GND/NC	GND/NC Connection in Application	NC
10	VINBCK2	Buck 2 High Voltage Supply	HV Supply
12	LEDCTRL2	LED String 2 Enable	MV IN
13	RSTB	External Reset Signal	MV IN
14	SDO	SPI Data Output	MV Open-Drain
15	CSB	SPI Chip Select (Chip Select Bar)	MV IN
16	SCLK	SPI Clock	MV IN
17	SDI	SPI Data Input	MV IN
18	VDD	3 V Logic Supply	LV Supply
19	LEDCTRL1	LED String 1 Enable	MV IN
21	VINBCK1	Buck 1 High Voltage Supply	HV Supply
23	LBCKSW1	Buck 1 Switch Output	HV OUT
24	VLED1	LED String 1 Forward Voltage Sense Input	HV IN

Table 3. ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Minimum	Maximum	Unit
VBOOST Supply Voltage	V_{BOOST}	−0.3	+68	V
VINBCKx Supply Voltage (Note 4)	VINBCKx	Max of VBOOSTM3V − 0.3, −0.3	Min of V_{BOOST} + 0.3, 68	V
VBOOSTM3V Supply Voltage (Note 5)	VBOOSTM3V	Max of V_{BOOST} − 3.6, −0.3	Min of V_{BOOST} + 0.3, 68	V
VLED Sense Voltage	VLEDx	−0.3	Min of V_{BOOST} + 0.3, 68	V
Logic Supply Voltage (Note 6)	V_{DD}	−0.3	3.6	V
Medium Voltage IO Pins (Note 7)	IOMV	−0.3	7.0	V
Test Pins (Note 8)	TESTx	−0.3	Min of V_{BOOST} + 0.3, 68	V
Buck Switch Low Side (Note 4)	LBCKSWx	−2.0	VINBCKx + 0.3	V
VLED Sink/Source Current	IVLEDx	−30	30	mA
Storage Temperature (Note 9)	T_{STRG}	−50	150	°C
The Exposed Pad (Note 10)	EXPAD	GND − 0.3	GND + 0.3	V
Electrostatic Discharge on Component Level (Note 11) Human Body Model Charge Device Model	 V_{ESD_HBM} V_{ESD_CDM}	 −2 −500	 +2 +500	 kV V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. V(VINBCKx − LBCKSWx) < 70 V, the driver in off state.
5. The VBOOSTM3V regulator in off state.
6. Absolute maximum rating for pins: VDD, TEST. Also valid for relative difference V_{BOOST} − VBOOSTM3V.
7. Absolute maximum rating for pins: SCLK, CSB, SDI, SDO, LEDCTRL1, LEDCTRL2, RSTB. The μC interface pins (the IOMV pins) accept 5 V while the device is in the power-off mode (V_{DD} = 0 V).
8. Absolute maximum rating for pins: TEST1, TEST2.
9. For limited time up to 100 hours. Otherwise the max storage temperature is 85°C.
10. The exposed pad must be hard wired to GND pin in an application to ensure both electrical and thermal connection.
11. This device series incorporates ESD protection and is tested by the following methods:
    ESD Human Body Model tested per AEC − Q100 − 002 (EIA/JESD22 − A114)
    ESD Charge Device Model tested per EIA/JESD22 − C101
    Latch-up Current Maximum Rating: ≤100 mA per JEDEC standard: JESD78

Operating ranges define the limits for functional operation and parametric characteristics of the device. A mission profile (Note 12) is a substantial part of the operation conditions; hence the Customer must contact **onsemi** in order to mutually agree in writing on the allowed missions profile(s) in the application.

Table 4. RECOMMENDED OPERATING RANGES

Characteristic	Symbol	Min	Typ	Max	Unit
Boost Supply Voltage N78723−0 Device N78723−2 Device	V_{BOOST}	 +8 +6		 +67 +67	V
VINBCKx Supply Voltage (Note 13)	VINBCKx	V_{BOOST} − 0.1	V_{BOOST}	V_{BOOST} + 0.1	V
Low Voltage Supply	V_{DD}	3.05	3.3	3.6	V
Buck Switch Output Current	I_LBCKSW			1.9	A
Functional Operating Junction Temperature Range (Note 14)	T_{JF}	−40		155	°C
Parametric Operating Junction Temperature Range (Note 15)	T_{JP}	−40		150	°C
The Exposed Pad Connection (Note 16)	EXPOSED_PAD	GND − 0.1	GND	GND + 0.1	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

12. A mission profile describes the application specific conditions such as, but not limited to, the cumulative operating conditions over life time, the system power dissipation, the system's environmental conditions, the thermal design of the customer's system, the modes, in which the device is operated by the customer, etc. No more than 100 cumulated hours in life time above T_{TW}.
13. Hard connection of VINBCKx to VBOOST on PCB.
14. The circuit functionality is not guaranteed outside the functional operating junction temperature range. Also please note that the device is verified on bench for operation up to 170°C but that the production test guarantees 155°C only.
15. The parametric characteristics of the circuit are not guaranteed outside the Parametric operating junction temperature range.
16. The exposed pad must be hard wired to GND pin in an application to ensure both electrical and thermal connection.

Table 5. THERMAL RESISTANCE

Characteristic	Package	Symbol	Min	Typ	Max	Unit
Thermal Resistance Junction to Exposed Pad (Note 17)	QFN24 5x5	R_{thjp}	−	5	−	°C/W

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$_{JP}$) range (−40°C; 150°C), unless otherwise specified)

Table 6. ELECTRICAL CHARACTERISTICS (continued)
(All Min and Max parameters are guaranteed over full junction temperature (T_{JP}) range (−40°C; 150°C), unless otherwise specified)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
BUCK REGULATOR − CURRENT REGULATION						
Current Sense Threshold Level, Range 1, Spec. Value	ITHR1_110	[BUCKx_VTHR = 01101110] End of the BUCK ON-Phase. Min. Value for Specified Precision	−	112.5	−	mA
Current Sense Threshold Level, Range 1, Max Value	ITHR1_255	[BUCKx_VTHR = 11111111] End of the BUCK ON-Phase	−	224.15	−	mA
Current Sense Threshold Level, Range 2, Min Value	ITHR2_000	[BUCKx_VTHR = 00000000] End of the BUCK ON-Phase	47.813	56.25	64.688	mA
Current Sense Threshold Level, Range 2, Spec. Value	ITHR2_110	[BUCKx_VTHR = 01101110] End of the BUCK ON-phase. Min. Value for Specified Precision	−	225	−	mA
Current Sense Threshold Level, Range 2, Max Value	ITHR2_255	[BUCKx_VTHR = 11111111] End of the BUCK ON-Phase	−	448.3	−	mA
Current Sense Threshold Level, Range 3, Min Value	ITHR3_000	[BUCKx_VTHR = 00000000] End of the BUCK ON-Phase	95.625	112.5	129.375	mA
Current Sense Threshold Level, Range 3, Spec. Value	ITHR3_110	[BUCKx_VTHR = 01101110] End of the BUCK ON-Phase. Min. Value for Specified Precision	−	450	−	mA
Current Sense Threshold Level, Range 3, Max Value	ITHR3_255	[BUCKx_VTHR = 11111111] End of the BUCK ON-phase	−	896.6	−	mA
Current Sense Threshold Level, Range 4, Min Value	ITHR4_000	[BUCKx_VTHR = 00000000] End of the BUCK ON-Phase	191.25	225	258.75	mA
Current Sense Threshold Level, Range 4, Spec. Value	ITHR4_110	[BUCKx_VTHR = 01101110] End of the BUCK ON-Phase. Min. Value for Specified Precision	−	900	−	mA
Current Sense Threshold Level, Range 4, Max Value	ITHR4_255	[BUCKx_VTHR = 11111111] End of the BUCK ON-Phase	−	1791.75	−	mA
Current Sense Threshold Increase per Code, Range 1	δITHR1	8 Bit, Linear Increase	−	0.77	−	mA
Current Sense Threshold Increase per Code, Range 2	δITHR2	8 Bit, Linear Increase	−	1.54	−	mA
Current Sense Threshold Increase per Code, Range 3	δITHR3	8 Bit, Linear Increase	−	3.08	−	mA
Current Sense Threshold Increase per Code, Range 4	δITHR4	8 Bit, Linear Increase	−	6.15	−	mA
Current Threshold Accuracy Only with Trimming Constant for the Highest Range (Note 23) N78723−0 N78723−2	ITHR_ERR_DD	Specified for BUCKx_VTHR ≥ 01101110, without the Delta of the Trimming Code and without Temp. Compensation	 −8 −9	 − −	 +8 +9	%
Current Threshold Accuracy without Temperature Compensation (Note 23) N78723−0 N78723−2	ITHR_ERR_D	Specified for BUCKx_VTHR ≥ 01101110, with the Delta of the Trimming Code and without Temp. Compensation	 −6 −7	 − −	 +6 +7	%
Current Threshold Accuracy (Note 23) N78723−0 N78723−2	ITHR_ERR	Specified for BUCKx_VTHR ≥ 01101110, the Delta of the Trimming Code and Temp. Compensation	 −3 −4	 − −	 +3 +4	%

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
23. Measured as comparator DC threshold value, without comparator delay and switch falling slope.

Table 6. ELECTRICAL CHARACTERISTICS (continued)
(All Min and Max parameters are guaranteed over full junction temperature (T_{JP}) range (−40°C; 150°C), unless otherwise specified)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
BUCK REGULATOR − CURRENT REGULATION						
Offset of Peak Current Comparator on N78723−2 Device	CMP_OFFSET		−10	−	+10	mV
Over-Current Detection Level, Range 1	OCDR1	Typ. 1.5 × ITHR1_255	286	−	388	mA
Over-Current Detection Level, Range 2	OCDR2	Typ. 1.5 × ITHR2_255	573	−	776	mA
Over-Current Detection Level, Range 3	OCDR3	Typ. 1.5 × ITHR3_255	1148	−	1553	mA
Over-Current Detection Level, Range 4	OCDR4	Typ. 1.5 × ITHR4_255	2295	−	3105	mA
Time Constant for Longest Off Time	TC_00	[BUCKx_TOFF = 00000]	−	50	−	µs·V
Time Constant for Shortest Off Time	TC_31	[BUCKx_TOFF = 11111]	−	5	−	µs·V
T_{OFF} Time Relative Error	TOFF_ERR	TC = T_{OFF} × V_{LED} @ VLED > 2 V, T_{OFF} > 350 ns	−10	−	+10	%
T_{OFF} Time Absolute Error	TOFF_ERR_ABS	TC = T_{OFF} × V_{LED} @ VLED > 2 V, T_{OFF} ≤ 350 ns	−35	−	+35	ns
Time Constant Decrease per Code	δTC	5 Bits, Exponential Decrease	−	7.16	−	%
Detection Level of V_{LED} to be Too Low	VLED_LMT		1.62	1.8	1.98	V
T_{OFF} Time for Low V_{LED} Voltages N78723−0 Device N78723−2 Device (Note 24)	TC_LOW	VLED < VLED_LMT	 78 72	 105 105	 120 140	µs
The Zero-cross Detection Threshold Level (Note 25)	TC_ZCD		−0.125	−	−0.005	V
The Zero-cross Detection Filter Time	TC_ZCD_FT		20	−	350	ns
OpenLEDx Detection Time	TON_OPEN		40	50	60	µs
Buck Minimum T_{ON} Time	TON_MIN	For VINBCKx – LBCKSWx < 2.4 V, No Failure at LBCKSWx Pin	50	−	250	ns
Delay from BUCKx ISENS Comparator Input Voltage Balance to BUCKx Switch Going OFF	ISENSCMP_DEL	ISENS Cmp. Over-Drive ramp > 1 mV/10 ns	−	70	−	ns

Table 6. ELECTRICAL CHARACTERISTICS (continued)
(All Min and Max parameters are guaranteed over full junction temperature (T_{JP}) range (−40°C; 150°C), unless otherwise specified)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
5 V TOLERANT OPEN-DRAIN DIGITAL OUTPUT (SDO)						
Low-Voltage Output Voltage	VOUTLO	I_{OUT}				

TYPICAL CHARACTERISTICS

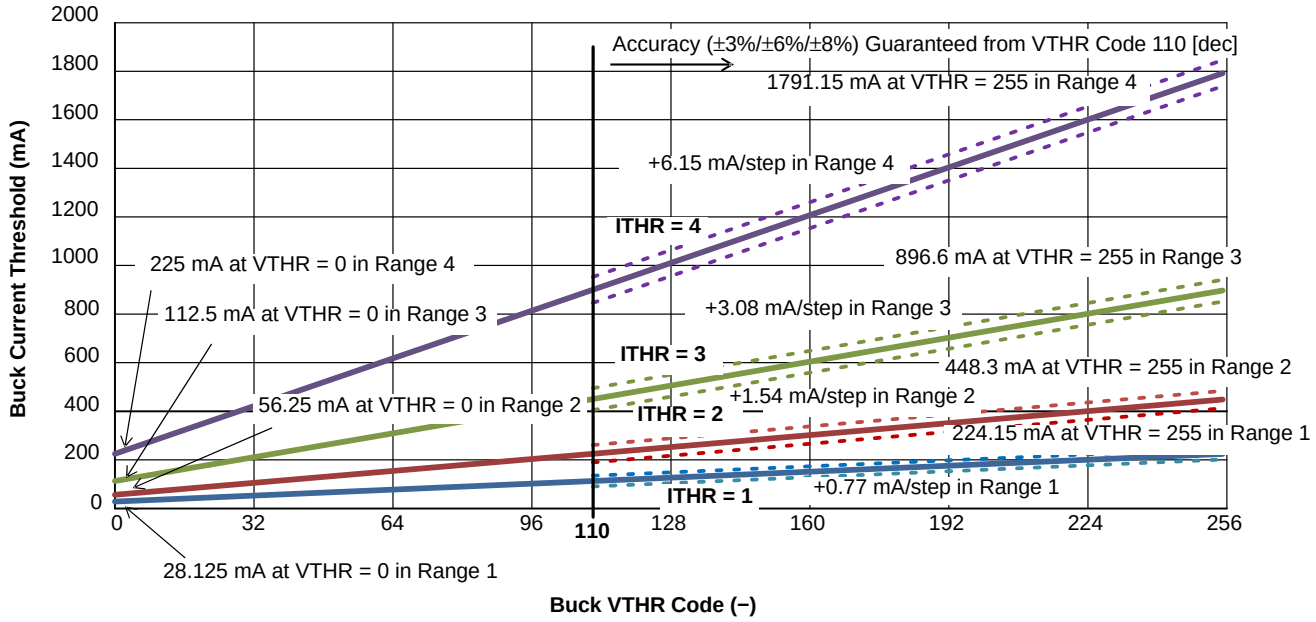


Figure 6. Buck Peak Current vs. Ranges and VTHR Code

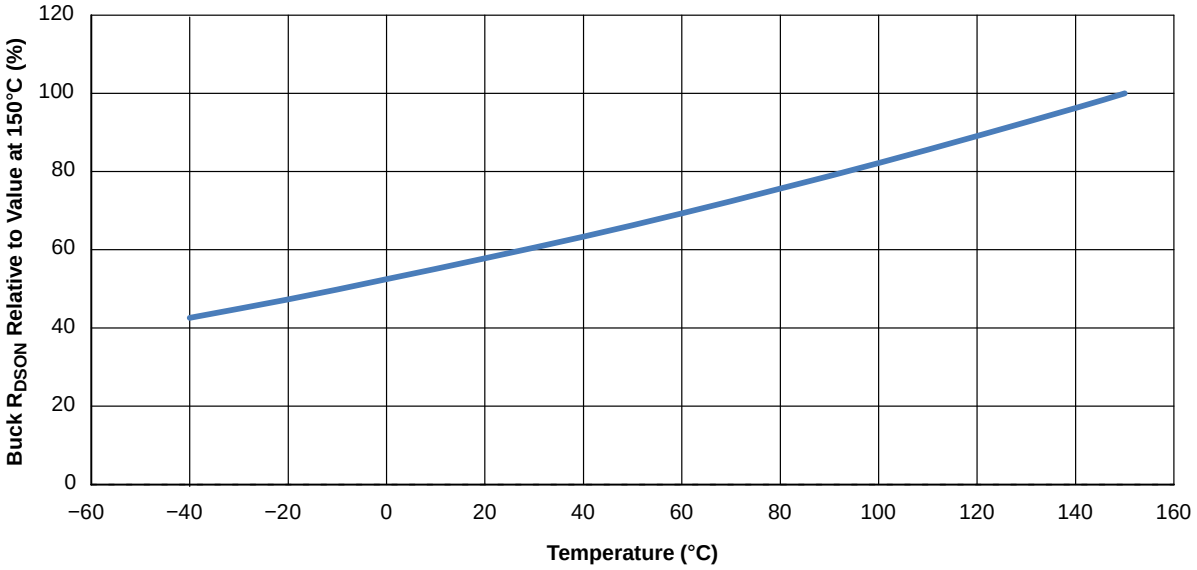


Figure 7. Typical Temperature Behavior of Buck Switch R_{DSON} Relative to the Value at 150°C

TYPICAL CHARACTERISTICS

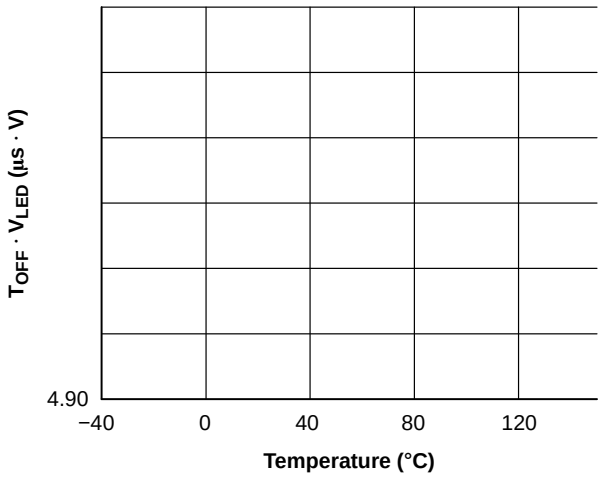


Figure 8. Typical Temperature Dependency of $T_{OFF} \cdot V_{LED}$ Constant (Shortest $T_{OFF} \cdot V_{LED}$ = 5 µs · V and Longest $T_{OFF} \cdot V_{LED}$ = 50 µs · V)

DETAILED OPERATING DESCRIPTION

Supply Concept in General

Two voltages have to be supplied to the NCV78723 chip – low voltage VDD logic supply and high voltage VBOOST for providing energy to the buck regulators. More detailed description follows.

VDD Supply

The VDD supply is the low voltage digital and analog supply for the chip. NCV78723 does not contain internal VDD regulator and this voltage is supposed to be provided externally by a dedicated voltage regulator that fulfills specified voltage and current needs or can be supplied from the NCV78702/NCV78703 VDD pin.

The Power-On-Reset circuit (POR) monitors the VDD voltage and RSTB pin to control the out-of-reset and reset entering state. At power-up, the chip will exit from reset state when VDD > POR3V_H and RSTB pin is in “log. 1”. No SPI communication is possible in reset state.

VBOOST Supply

The VBOOST supply voltage is the main high voltage supply for the chip. The voltage is supposed to be provided by booster chip such as NCV78702/NCV78703 or NCV878763 in an application. VINBCKx pins have to be connected by low impedance track to this supply to ensure proper buck performance.

The VBOOST voltage is monitored by under-voltage comparator to check sufficient zapping voltage at VBOOST pin during OTP programming operation.

VBOOSTM3V Supply

The VBOOSTM3V is the high side auxiliary supply for the gate drive of the buck regulators’ integrated high-side P-MOSFET switches. This supply receives energy directly from the VBOOST pin.

Internal Clock Generation – OSC10M

An internal RC clock named OSC10M is used to run all the digital functions in the chip. The clock is trimmed in the factory prior to delivery. Its accuracy is guaranteed under full operating conditions and is independent from external component selection (refer to Table 6 − OSC10M: System Oscillator Clock for details). All timings depend on OSC10M accuracy.

Buck Regulator

General

The NCV78723 contains two high-current integrated buck current regulators, which are the sources for the LED strings. The bucks are powered from the external booster regulator.

Buck Current Regulation Principle

Each buck controls the individual inductor peak current ($I_{BUCKpeak}$) and incorporates a constant ripple ($\Delta I_{BUCKpkpk}$) control circuit to ensure also stable average current through the LED string, independently from the string voltage. The buck average current is in fact described by the formula:

$$I_{BUCK_{AVG}} = I_{BUCK_{peak}} - \frac{\Delta I_{BUCK_{pkpk}}}{2}$$

The LED average current in time (DC) is equal to the buck time average current. Therefore, to achieve a given LED current target, it is sufficient to know the buck peak current and the buck current ripple. A rule of thumb is to count a

SW Compensation of the Buck Current Accuracy

In order to ensure buck current accuracy as specified in Table 6 − Buck Regulator – Current Regulation, set of constants trimmed during manufacturing process is available. Microcontroller should use them in the following way:

To Reach ±8% (±9% for N78723−2) Accuracy (±6% for Range 4) Over Whole Temperature Operating Range:

All ranges: ***BUCKx_ISENS_TRIM[6:0] = BUCKx_ISENS_RNG[6:0]***

BUCKx_ISENS_RNG[6:0] is trimming constant for the highest current range (Range 4) at hot temperature.
BUCKx_ISENS_RNG[6:0] constant is loaded into BUCKx_ISENS_TRIM[6:0] register automatically after the reset of the device.

To Reach ±6% (±7% for N78723−2) Accuracy Over Whole Temperature Operating Range:

BUCKx_ISENS_Dx[3:0] registers, meaning delta of the trimming constant with respect to the higher current range at hot temperature, have to be used. Trimming constant for the particular range at hot temperature can be then calculated as:

Range 4: ***BUCKx_R4_trim_hot = BUCKx_ISENS_RNG[6:0]***,
Range 3: ***BUCKx_R3_trim_hot = BUCKx_ISENS_RNG[6:0] + BUCKx_ISENS_D3[3:0]***,
Range 2: ***BUCKx_R2_trim_hot = BUCKx_ISENS_RNG[6:0] + BUCKx_ISENS_D3[3:0] + BUCKx_ISENS_D2[3:0]***,
Range 1: ***BUCKx_R1_trim_hot = BUCKx_ISENS_RNG[6:0] + BUCKx_ISENS_D3[3:0] + BUCKx_ISENS_D2[3:0] + BUCKx_ISENS_D1[3:0]***,

where:

delta of the trimming constant BUCKx_ISENS_Dx[3:0] is signed, coded as two's complement. Range of this constant is decadic <−8; 7>, binary <1000; 0111>.

Calculated trimming constant has to be then written into trimming SPI register:
BUCKx_ISENS_TRIM[6:0] = BUCKx_Ry_trim_hot

To Reach ±3% (±4% for N78723−2) Accuracy Over Whole Temperature Operating Range:

In addition to BUCKx_ISENS_Dx[3:0] registers, the BUCK_ISENS_TCx[3:0] registers, meaning temperature coefficients for the appropriate ranges, have to be used.

When TC_VERSION = 0, trimming value for a certain temperature should be calculated as:

Range 4: $BUCKx\_R4\_trim = BUCKx\_R4\_trim\_hot + k_{L3} \cdot (Tj - Thot) + k_Q \cdot (Tj - Thot)^2$,
Range 3: $BUCKx\_R3\_trim = BUCKx\_R3\_trim\_hot + k_{L2} \cdot (Tj - Thot) + k_Q \cdot (Tj - Thot)^2$,
Range 2: $BUCKx\_R2\_trim = BUCKx\_R2\_trim\_hot + k_{L1} \cdot (Tj - Thot) + k_Q \cdot (Tj - Thot)^2$,
Range 1: $BUCKx\_R1\_trim = BUCKx\_R1\_trim\_hot + k_{L0} \cdot (Tj - Thot) + k_Q \cdot (Tj - Thot)^2$,

When TC_VERSION = 1, trimming value for a certain temperature should be calculated as:

Range 4: $BUCK2\_R4\_trim = BUCK2\_R4\_trim\_hot + k_{L3} \cdot (Tj - Thot) + k_Q \cdot (Tj - Thot)^2$,
Range 3: $BUCK2\_R3\_trim = BUCK2\_R3\_trim\_hot + k_{L3} \cdot (Tj - Thot) + k_Q \cdot (Tj - Thot)^2$,
Range 2: $BUCK2\_R2\_trim = BUCK2\_R2\_trim\_hot + k_{L2} \cdot (Tj - Thot) + k_Q \cdot (Tj - Thot)^2$,
Range 1: $BUCK2\_R1\_trim = BUCK2\_R1\_trim\_hot + k_{L2} \cdot (Tj - Thot) + k_Q \cdot (Tj - Thot)^2$,
Range 4: $BUCK1\_R4\_trim = BUCK1\_R4\_trim\_hot + k_{L1} \cdot (Tj - Thot) + k_Q \cdot (Tj - Thot)^2$,
Range 3: $BUCK1\_R3\_trim = BUCK1\_R3\_trim\_hot + k_{L1} \cdot (Tj - Thot) + k_Q \cdot (Tj - Thot)^2$,
Range 2: $BUCK1\_R2\_trim = BUCK1\_R2\_trim\_hot + k_{L0} \cdot (Tj - Thot) + k_Q \cdot (Tj - Thot)^2$,
Range 1: $BUCK1\_R1\_trim = BUCK1\_R1\_trim\_hot + k_{L0} \cdot (Tj - Thot) + k_Q \cdot (Tj - Thot)^2$,

where:

buck temperature coefficient BUCK_ISENS_TCx[3:0] is signed, coded as two's complement. Range of this constant is decadic <−8; 7>, binary <1000; 0111>,

k_{Lx} is linear coefficient for each current range calculated: k_{Lx} = (BUCK_ISENS_TCx[3:0] – $k_Q \cdot (170°C)^2$)/(−170°C) [code/°C] when TC_VERSION = 0

k_{Lx} is linear coefficient for each current range calculated: k_{Lx} = (BUCK_ISENS_TCx[3:0] – $k_Q \cdot (200°C)^2$)/(−200°C) [code/°C] when TC_VERSION = 1

k_Q is quadratic constant for all current ranges: $k_Q = 2.18 \cdot 10^{-4}$ [code/(°C)^2]

Tj is junction temperature in °C calculated from VTEMP[7:0] SPI register value according to the equation defined in chapter *ADC:* Device Temperature ADC: V_{TEMP}

Thot temperature is constant equal to 125°C when TC_VERSION = 0

Thot temperature is constant equal to 155°C when TC_VERSION = 1.

Calculated trimming constant has to be then written into trimming SPI register**:**
BUCKx_ISENS_TRIM[6:0] = BUCKx_Ry_trim

Note: The BUCKx_ISENS_TRIM[6:0] SPI register allows compensation of the peak current app. in range ±40 % from actual value according to the following equation:

$$IBUCKx = (ITHRx\_000 + \delta ITHRx \cdot BUCKx\_VTHR[7:0]) \cdot (1 + 0.4 \cdot ((BUCKx\_ISENS\_TRIM[6:0] - 63)/63)),$$

where:
ITHRx_000 is current for VTHR code 0 in ITHRx range (see Table 6 − *Buck Regulator – Current Regulation*),
δITHRx code step in range ITHRx (see Table 6 − Buck Regulator – Current Regulation).

Paralleling the Bucks for Higher Current Capability

Different buck channels can be paralleled at the module output (after the buck inductors) for *higher current capability* on a unique channel, summing up together the individual DC currents.

Buck Overcurrent Protection

Being a current regulator, the NCV78723 buck is by nature preventing overcurrent in all normal situations. However, in order to protect the system from overcurrent even in case of failures, protection mechanism is available.

This protection is based on internal sensing over the buck

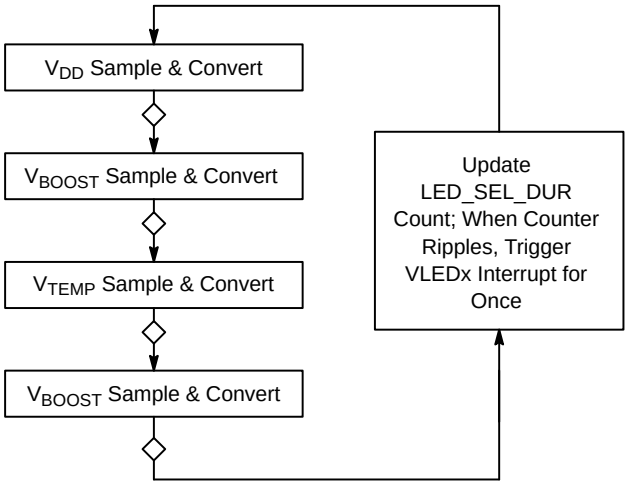


Figure 15. ADC Sample and Conversion Main Sequence

Referring to the figure above, the typical rate for a full SAR plus digital conversion per channel is 8 μs (Table 6 − ADC for Measuring VBOOST, VDD, VLED1, VLED2, TEMP). For instance, each new VBOOST ADC converted sample occurs at 16 μ

VTEMP[7:0] is the value read out directly from the related 8bit-SPI register (please refer to the SPI map). The value is also used internally by the device for the *thermal warning* and *thermal shutdown* functions. More details on these two can be found in the dedicated sections in this document. The value is protected by ODD parity bit.

detection of transition period during which the BUCKx output current decreases due to the change of BUCKx_VTHR code or BUCKx_ISENS_THR range.

- *Buckx TON Time Duration:* SPI register BUCKx_TON_DUR[7:0] reflects the last measured Buckx TON time (1LSB = 200 ns) on the corresponding channel. When Buckx runs with TON time < typ. 200 ns, the BUCKx_TON_DUR[7:0] SPI register returns value 0x00. When Buckx is stopped, the BUCKx_TON_DUR[7:0] register keeps the last measured TON time.
- *HW Reset:* the out of reset condition is reported through the HWR bit (latched). This bit is set only at each Power On Reset (POR) and indicates the device is ready to operate.

A short summary table of the main diagnostic bits related to the LED outputs follows.

Table 7. LED OUTPUT DIAGNOSTIC SUMMARY

Diagnose		Detection Level	LED Output	Latched
Flag	Description			
TW	Thermal Warning	SPI Register Programmable	Not Disabled (If No TSD, otherwise Disabled)	Yes
TSD	Thermal Shutdown	Factory Trimmed	Disabled (Automatically Re-Enabled when Temp Falls below TW and BUCKx_TSD_AUT_RCVR_EN = 1)	Yes
SPIERR	SPI Error	(See SPI Section)	Not Disabled	Yes
OPENLEDx	LED String Open Circuit	Buck on Time > TON_OPEN	Not Disabled	Yes
SHORTLEDx	LED String Short Circuit	VLEDx < VLED_LMT	Not Disabled (Fixed Buck TOFF or Zero Cross TOFF Applied when output is On)	Yes
OCLEDx	LED String Overcurrent	Ibuckx > OCDR{1..4}	Disabled	Yes

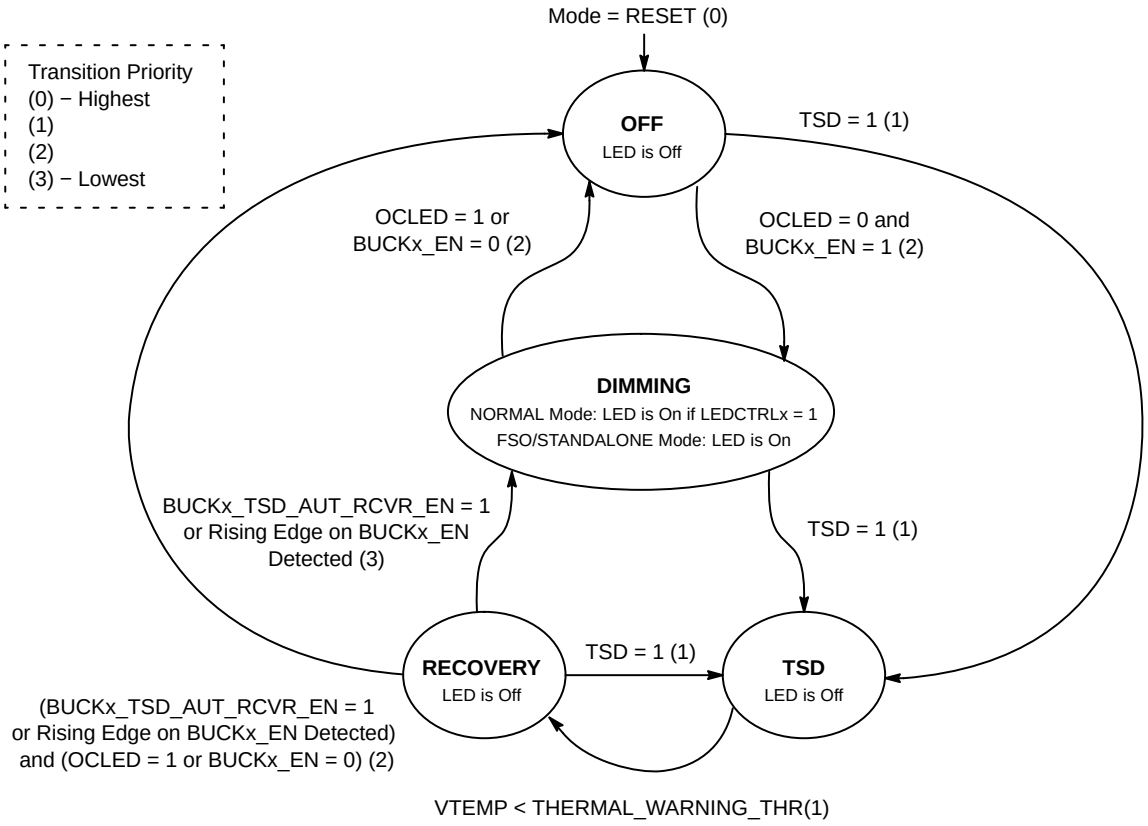


Figure 17. LED Dimming State Diagram

Functional Mode Description

Overview of all functional modes is in accordance to the state diagram on Figure 18. Individual states are described below.

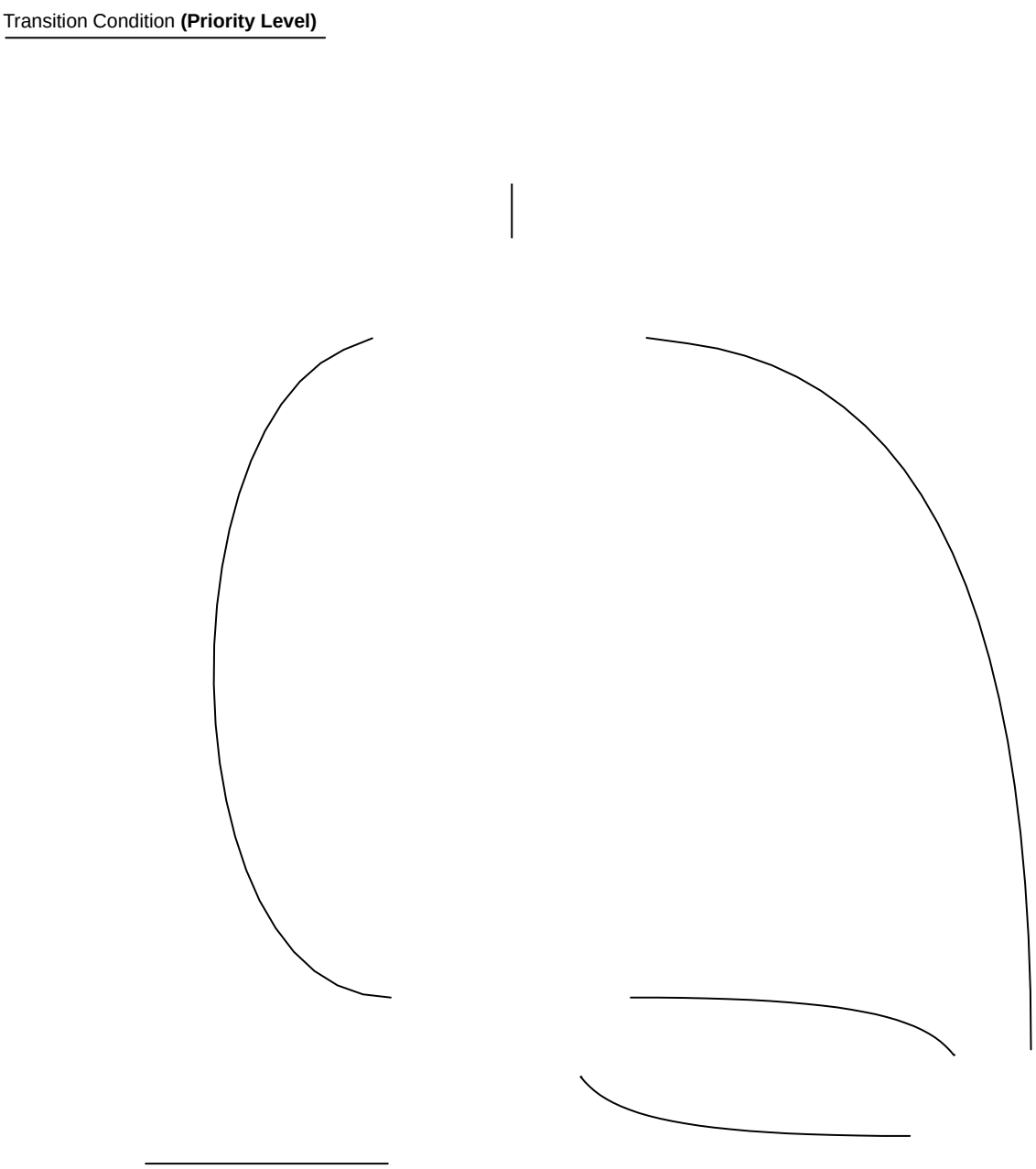


Figure 18. Functional Modes State Diagram

Reset

Asynchronous reset is caused either by POR (POR always causes asynchronous reset − transition to reset state) or by falling edge on RSTB pin (in normal/stand-alone mode, when FSO_MD[2:0] = 000 or 001 or 110 or 111).

Init and Normal Mode

Normal mode is entered through Init state after internal delay of 150 μs. In Init state, OTP refresh is performed. If OTP bits for FSO_MD[2:0] register and *OTP Lock Bit* are programmed, transition to FSO/SA mode is possible.

FSO/Stand-Alone Mode

FSO (Fail-Safe Operation)/Stand-Alone modes can be used for two main purposes:

- Default power-up operation of the chip (**Stand-Alone** functionality without external microcontroller or preloading of the registers with default content for default operation before microcontroller starts sending SPI commands for chip settings)
- **Fail-Safe** functionality (chip functionality definition in fail-safe mode when the external microcontroller functionality is not guaranteed)

FSO/stand-alone function is controlled according to Table 8. Entrance into FSO/Stand-alone mode is possible only after customer OTP zapping when *OTP Lock Bit* is set. After FSO mode activation, the FSO bit in status register is set. FSO register is cleared by read register.

When FSO/Stand-Alone mode is activated, content of the following SPI registers is preloaded from OTP memory:

BUCK1_VTHR[7:0],
BUCK1_ISENS_THR[1:0],
BUCK2_VTHR[7:0],
BUCK2_ISENS_THR[1:0],
BUCK1_TOFF[4:0],
BUCK2_TOFF[4:0],
BUCK1_EN,
BUCK2_EN,
FSO_MD[2:0],
BUCK1_TSD_AUT_RCVR_EN,
BUCK2_TSD_AUT_RCVR_EN,

(‘0’e)until, thefirst vnalds SPI operationits finshsdn te
activatiot dfuock reulatoeisammeivatlye
POR to prvtentun defisdn state ofLEDCTRLxB pisn in
MCU clevdes PORlateor tcan(NCV78721).)]TJ-.8957 -1.1962 TD0 Tc.127 Tw[In(FSO and/Stand-Alone mode, thelogic clveal(t()]TJ/TT8 1 Tf-.8

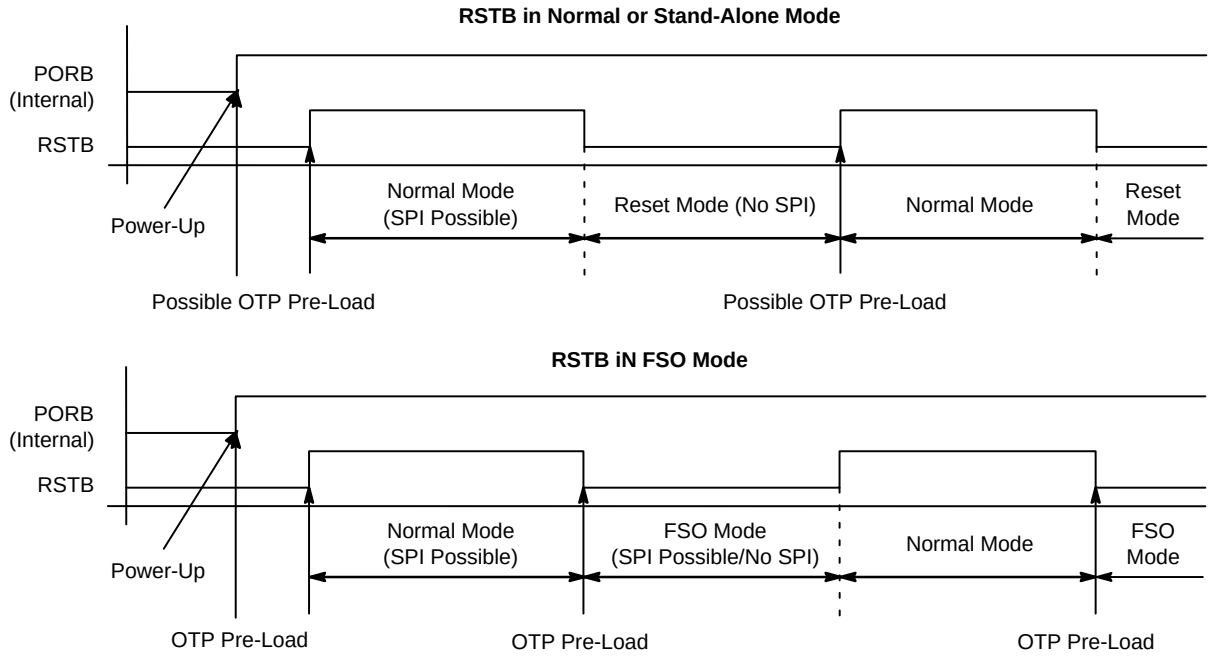


Figure 19. RSTB Pin Functionality in Normal, Stand-Alone and FSO Modes

Table 8. FSO MODES

FSO_MD[2:0]	Description
000_b = 0	**FSO Mode Disabled, Registers are Loaded with Safe Value = 0x00h after POR, Default** • After the reset, control registers are loaded with 0x00h value. • Entrance into FSO mode is not possible unless dedicated SPI write command to change FSO_MD[2:0] value is sent • RSTB pin has **reset** functionality • LEDCTRLx pins are functional (buck enable/disable, digital PWM dimming available)
001_b = 1	**FSO Mode Disabled, Registers are Loaded with Data from OTP Memory after POR** • After the reset, control registers are loaded with data stored in OTP memory (device's OTP memory has to be programmed, has to be set). It reduces number of SPI transfers needed to configure the device after the reset. • Entrance into FSO mode is not possible • RSTB pin has **reset** functionality • LEDCTRLx pins are functional (buck enable/disable, digital PWM dimming available)
010_b = 2	**FSO Entered after Falling Edge on RSTB Pin, Registers (except FSO_MD[2:0]) are Loaded with Safe Value = 0x00h after POR** • After FSO mode activation, control registers are loaded with data stored in OTP memory.

Table 8. FSO MODES (continued)

FSO_MD[2:0]	Description
101_b = 5	**FSO Entered after Falling Edge on RSTB Pin, Registers are Loaded with Data from OTP Memory after POR** • After FSO mode activation, control registers are loaded with data stored in OTP memory. • SPI register update (SPI write/read operation) in FSO mode is **enabled** • FSO mode can be exited by writing FSO_MD[2:0] = 000 or 001 • RSTB pin serves to enter/exit FSO mode. • LEDCTRLx pins are not functional (buck enable/disable only by means of BUCKx_EN SPI/OTP bits, digital PWM dimming not available).
110_b = 6	**SA (Stand-Alone)/FSO Entered after POR (RSTB Pin Rising Edge), Registers are Loaded with Data from OTP Memory** • After FSO/SA mode activation, control registers are loaded with data from OTP memory • SPI register update (SPI write/read operation) in SA/FSO mode is **disabled** (SPI write operation is blocked; clearing of SPI registers is blocked; in case of invalid SPI frame, SPIERR flag is set). • RSTB pin has **reset**

the 16-bit command frame on the data input line transmitted by the Master, shifting via the chips' shift registers through the daisy chain. The chips interpret the command once the chip select line rises.

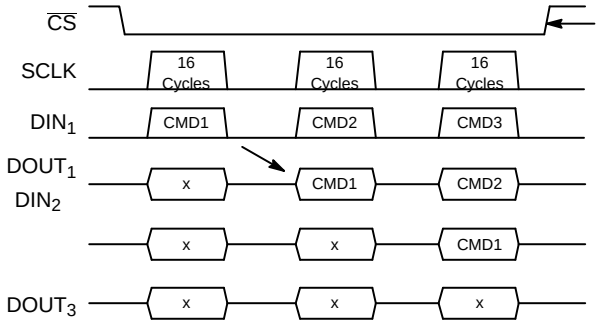


Figure 21. SPI Daisy Chain Data Shift between Slaves. The Symbol 'x' Represents the Previous Content of the SPI Shift Register Buffer

Bit 3	Bit 2	Bit 1
	[4:0]	
		BUCK1_EN
		OTP_OPER
	2	SHORTLED2
		TSD
		BUCK1_ STATUS

Table 10. BIT DEFINITION

Symbol	MAP Position	Description
REGISTER 0X00 (CR): NOP REGISTER, RESET VALUE (POR) = 0000000000_2		
NOP	Bits [9:0] – ADDR_0x00	NOP Register (Read/Write Operation Ignored)
REGISTER 0X01 (CR): BUCK 1 PEAK CURRENT SETTINGS, RESET VALUE (POR) = 0000000000_2		

Table 10. BIT DEFINITION (continued)

Symbol	MAP Position	Description
REGISTER 0X0C (SR): VLED1, RESET VALUE (POR) = 0100000000_2		
ODD PARITY	Bit 8 – ADDR_0x0C	Odd Parity over Data
VLED1[7:0]	Bits [7:0] – ADDR_0x0C	Output of VLED 1 ADC
REGISTER 0X0D (SR): VLED2, RESET VALUE (POR) = 0100000000_2		
ODD PARITY	Bit 8 – ADDR_0x0D	Odd Parity over Data
VLED2[7:0]	Bits [7:0] – ADDR_0x0D	Output of VLED 2 ADC
REGISTER 0X0E (SR): VTEMP, RESET VALUE (POR) = $0XXXXXXXXX_2$		
ODD PARITY	Bit 8 – ADDR_0x0E	Odd Parity over Data
VTEMP[7:0]	Bits [7:0] – ADDR_0x0E	Output of VTEMP ADC
REGISTER 0X0F (SR): VBOOST, RESET VALUE (POR) = $0XXXXXXXXX_2$		
ODD PARITY	Bit 8 – ADDR_0x0F	Odd Parity over Data
VBOOST[7:0]	Bits [7:0] – ADDR_0x0F	Output of VBOOST ADC
REGISTER 0X10 (SR): VDD, RESET VALUE (POR) = $0XXXXXXXXX_2$		
ODD PARITY	Bit 8 – ADDR_0x10	Odd Parity over Data
VDD[7:0]	Bits [7:0] – ADDR_0x10	Output of VDD ADC
REGISTER 0X11 (SR): BUCK1_TON_DUR, RESET VALUE (POR) = 0100000000_2		
ODD PARITY	Bit 8 – ADDR_0x11	Odd Parity over Data
BUCK1_TON_DUR[7:0]	Bits [7:0] – ADDR_0x11	Buck 1 Ton Duration
REGISTER 0X12 (SR): BUCK2_TON_DUR, RESET VALUE (POR) = 0100000000_2		
ODD PARITY	Bit 8 – ADDR_0x12	Odd Parity over DataON_144.983 107.603 .90707 ref11.189 432.34 9071 436.4788

Table 10. BIT DEFINITION (continued)

Symbol	MAP Position	Description
REGISTER 0X16: BUCK TRIMMING, RESET VALUE (POR) = $0X0XXXXXX_2$		
ODD PARITY	Bit 8 – ADDR_0x16	Odd Parity over Data
BUCK1_ISENS_RNG[6:0]	Bits [6:0] – ADDR_0x16	Trimming Constant for Highest Range on Hot for Buck 1 Peak Current
REGISTER 0X17: BUCK TRIMMING, RESET VALUE (POR) = $0X0XXXXXX_2$		
ODD PARITY	Bit 8 – ADDR_0x17	Odd Parity over Data
BUCK2_ISENS_RNG[6:0]	Bits [6:0] – ADDR_0x17	Trimming Constant for Highest Range on Hot for Buck 2 Peak Current
REGISTER 0X18: BUCK TRIMMING, RESET VALUE (POR) = $0XXXXXXXX_2$		
ODD PARITY	Bit 8 – ADDR_0x18	Odd Parity over Data
BUCK2_ISENS_D1[3:0]	Bits [7:4] – ADDR_0x18	Delta Trimming Constant for Buck 2 Peak Current
BUCK1_ISENS_D1[3:0]	Bits [3:0] – ADDR_0x18	Delta Trimming Constant for Buck 1 Peak Current
REGISTER 0X19: BUCK TRIMMING, RESET VALUE (POR) = $0XXXXXXXX_2$		
ODD PARITY	Bit 8 – ADDR_0x19	Odd Parity over Data
BUCK2_ISENS_D2[3:0]	Bits [7:4] – ADDR_0x19	Delta Trimming Constant for Buck 2 Peak Current
BUCK1_ISENS_D2[3:0]	Bits [3:0] – ADDR_0x19	Delta Trimming Constant for Buck 1 Peak Current
REGISTER 0X1A: BUCK TRIMMING, RESET VALUE (POR) = $0XXXXXXXX_2$		
ODD PARITY	Bit 8 – ADDR_0x1A	Odd Parity over Data
BUCK2_ISENS_D3[3:0]	Bits [7:4] – ADDR_0x1A	Delta Trimming Constant for Buck 2 Peak Current
BUCK1_ISENS_D3[3:0]	Bits [3:0] – ADDR_0x1A	Delta Trimming Constant for Buck 1 Peak Current
REGISTER 0X1B: BUCK TRIMMING, RESET VALUE (POR) = $0XXXXXXXX_2$		
ODD PARITY	Bit 8 – ADDR_0x1B	Odd Parity over Data
BUCK_ISENS_TC1[3:0]	Bits [7:4] – ADDR_0x1B	Temperature Coefficient Trimming Constant for Buck Peak Current
BUCK_ISENS_TC0[3:0]	Bits [3:0] – ADDR_0x1B	Temperature Coefficient Trimming Constant for Buck Peak Current
REGISTER 0X1C: BUCK TRIMMING, RESET VALUE (POR) = $0XXXXXXXX_2$		
ODD PARITY	Bit 8 – ADDR_0x1C	Odd Parity over Data
BUCK_ISENS_TC3[3:0]	Bits [7:4] – ADDR_0x1C	Temperature Coefficient Trimming Constant for Buck Peak Current
BUCK_ISENS_TC2[3:0]	Bits [3:0] – ADDR_0x1C	Temperature Coefficient Trimming Constant for Buck Peak Current
REGISTER 0X1D: BUCK TRIMMING, RESET VALUE (POR) = $0X0000000X_2$		
ODD PARITY	Bit 8 – ADDR_0x1D	Odd Parity over Data
TC_VERSION	Bit 0 – ADDR_0x1D	Usage of BUCK_ISENS_TCx[3:0] Constants
REGISTER 0X1E: OTP DATA, RESET VALUE (POR) = 0000000000_2		
OTP_DATA[9:0]	Bits [9:0] – ADDR_0x1E	OTP Data
REGISTER 0X1F: REVID, RESET VALUE (POR) = $00000XXXXXX_2$		
REVID[7:0]	Bits [7:0] – ADDR_0x1F	Revision ID

POR values of status registers are shown in situation that FSO mode is not entered after POR. All latched flags are “cleared by read”. ‘x’ means that value after reset is defined during reset phase (diagnostics) or is trimmed during manufacturing process.

SPI register SPI_REVID[7:0] is used to track the silicon version, following encoding mechanism is used:

- SPI_REVID[7:6]: Constant 00 [binary]
- SPI_REVID[5]: 713/723 Distinguishing Bit (REVID[5] = 0 means 723)
- SPI_REVID[4:3]: Full Mask Version <0 to 3>
- SPI_REVID[2]: N78723−0/N78723−2 Distinguishing Bit (REVID[2] = 0 means N78723−0)
- SPI_REVID[1:0]: Metal Tune <0 to 3>

REVID[7:0] for N78723−0 device is 11hex (723 = 0, Full Mask Version = 2, N78723−0 = 0, Metal Tune = 1)

REVID[7:0] for N78723−2 device is 14hex (723 = 0, Full Mask Version = 2, N78723−2 = 1, Metal Tune = 0)

Table 12. ORDERING INFORMATION

Device**	Marking	Package*	Shipping†
NCV78723MW2R2G	N78723−2	QFNW24 5 × 5 with Step-cut Wettable Flank (Pb-Free)	5,000 / Tape & Reel
NCV78723MW2AR2G***	N78723−2	QFNW24 5 × 5 with Step-cut Wettable Flank (Pb-Free)	5,000 / Tape & Reel

DISCONTINUED (Note 32)

NCV78723MW0CR2G	N78723−0	QFN24 5 × 5 with Wettable Flank (Pb-Free)	5,000 / Tape & Reel
NCV78723MW0R2G	N78723−0	QFN24 5 × 5 with Wettable Flank (Pb-Free)	5,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

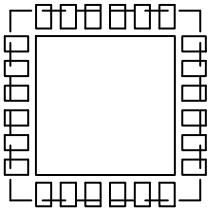
32. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

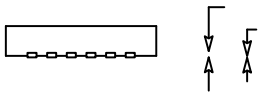
** NCV78723MW2 & NCV78723MW0 have different package mold compound. Please contact **onsemi** for technical details.

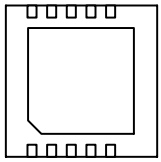
*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

*** NCV78723MW2AR2G is recommended for new designs.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.







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