High Efficienc 2 Pha e Boo e LED D i e fo A omo i e F on Ligh ing

NCV78902

The NCV78902 is a single−chip and high efficient two phase Booster designed for automotive front lighting applications like high beam, low beam, DRL (daytime running light), turn indicator, fog light, static cornering, etc. The NCV78902 is in particular designed for high current LEDs and with NCV78935 (triple channel Buck) or NCV78925 (dual channel Buck) provides a complete solution to drive multiple LED strings of up−to 60 V.

The device integrates a current-mode voltage booster controller, realizing a unique input current filter with a limited BOM. The available output voltage can be customized. Two devices NCV78902 can be combined and the booster circuits can operate together to function as a multiphase booster (2-phase, 3-phase, 4-phase) in order to further optimize the filtering effect of the booster and allow cost effective dimensioning for mid to high power LED systems.

Thanks to the SPI programmability, one single hardware configuration can support various application platforms.

- Single Chip Two−Phase Booster
- Current Sensing on Shunt Resistors or MOSFETs’ RDSon
- Stand−Alone/Limp Home Mode
- Built−in Programmaable Soft−

Publication Order Number:

L_BST_21

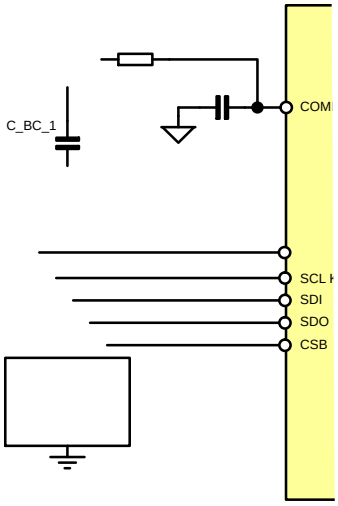
CIN_BST

T_BST_2

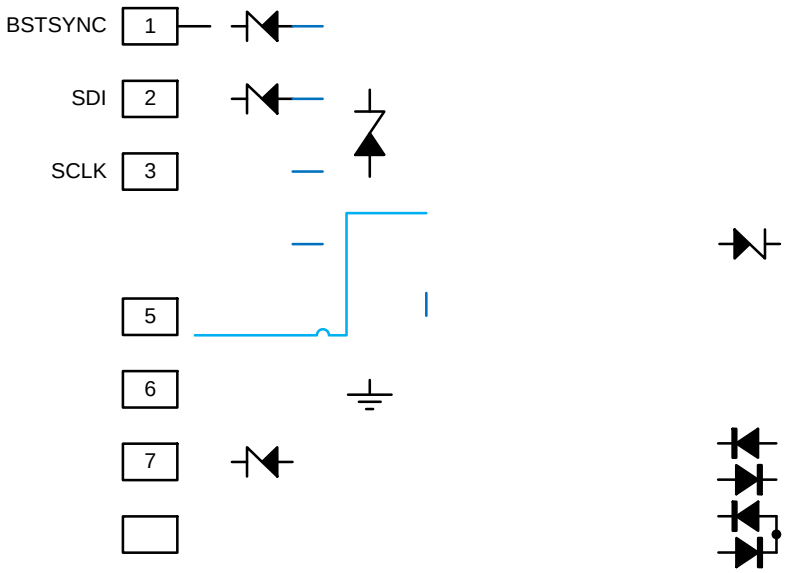
L_BST_22

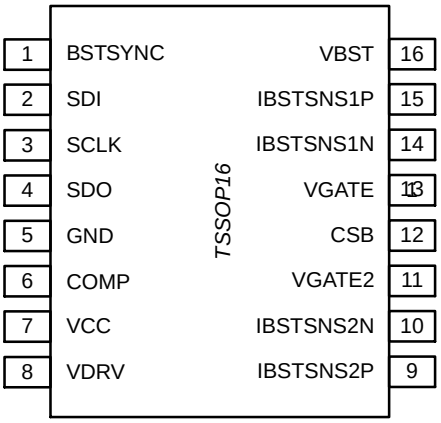
2 phase booster

NCV78902



µC


BSTSYNC
1
SDI
2
SCLK
3
5
6
7



1	BSTSYNC	External clock for the booster	DI, 5V
2	SDI	SPI data in pin	DI, 5V
3	SCLK	SPI clock pin	DI, 5V
4	SDO	SPI data out pin	DO, 5V
5	GND	Ground	Ground
6	COMP	Compensation for the boost regulator	MV Analog
7	VCC	3.3 V/5 V voltage supply	MV Supply
8	VDRV	5 V voltage supply	MV Supply
9	IBSTSNS2P	Booster current positive feedback input (phase 2)	HV Analog
10	IBSTSNS2N	Booster current negative feedback input (phase 2)	HV Analog
11	VGATE2	Booster MOSFET gate pre-driver (phase 2)	MV Analog, DO
12	CSB	SPI chip select pin	DI, 5 V
13	VGATE1	Booster MOSFET gate pre-driver (phase 1)	MV Analog, DO
14	IBSTSNS1N	Booster current negative feedback input (phase 1)	HV Analog
15	IBSTSNS1P	Booster current positive feedback input (phase 1)	HV Analog
16	VBST	Booster voltage feedback input	HV Analog

Ground Voltage	GND	0	0	V
Boost Voltage Feedback Input	VBST	−0.3	66 (Note 2)	V
VCC Supply Voltage	VCC	−0.3	6	V
VDRV Supply Voltage	VDRV	−0.3	6	V
SPI Clock Signal	SCLK	−0.3	6	V
SPI Chip Select Signal	CSB	−0.3	6	V
SPI Data Input Signal	SDI	−0.3	6	V
SPI Data Output Signal	SDO	−0.3	VCC + 0.3	V
BSTSYNC Signal	BSTSYNC	−0.3	6	V
Boost Current Sensing Positive Input	IBSTSNSxP	−1	68 (Note 2)	V
Boost Current Sensing Negative Input	IBSTSNSxN	−1	68 (Note 2)	

Thermal Resistance Junction to Ambient (Note 10)	TSSOP16	Rthja	−	175	−	°C/W

10. 4 layer PCB 50 x 50 x 1.5 mm, Cu layer thickness: Outer layers: 53 μm thickness, Inner layers: 35 μm thickness, Outer layers: 20% Cu coverage, Inner layers: 80% Cu coverage.

(All Min and Max parameters are guaranteed over full junction temperature (T_{JP}) range (−40 °C; 145 °C), unless otherwise specified.)

(All Min and Max parameters are guaranteed over full junction temperature (T_{JP}) range (−40 °C; 145 °C), unless otherwise specified.) (continued)

(All Min and Max parameters are guaranteed over full junction temperature (T_{JP}) range (−40 °C; 145 °C), unless otherwise specified.) (continued)

Booster Voltage Feedback Fail Detection Threshold	BST_FBFAIL		1.15	1.21	1.27	V
Booster Regulation Level	BST_REG_127					

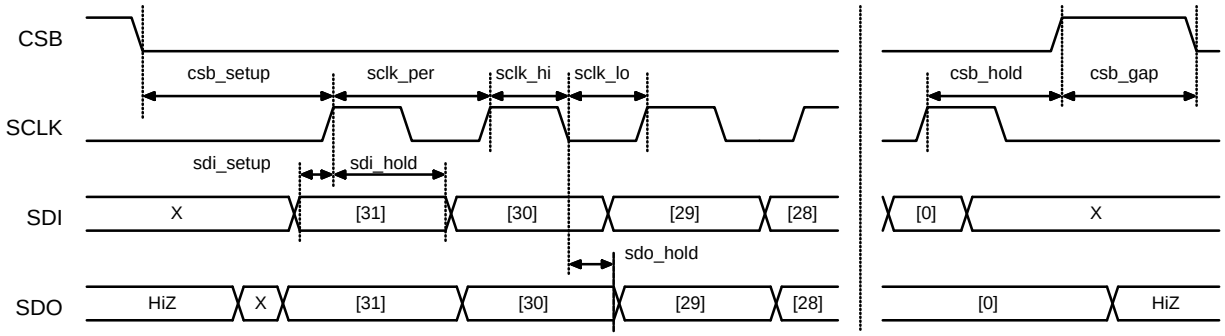
(All Min and Max parameters are guaranteed over full junction temperature (T_{JP}) range (−40 °C; 145 °C), unless otherwise specified.) (continued)

(All Min and Max parameters are guaranteed over full junction temperature (T_{JP}) range (−40 °C; 145 °C), unless otherwise specified.) (continued)

CSB Setup Time	csb_setup	CSB setup time before first SCLK rising edge	375	−	−	ns
CSB Hold Time	csb_hold	CSB hold time after last SCLK rising edge	150	−	−	ns
CSB High Time	csb_gap	Gap between two CSB low pulses	500	−	−	ns
SCLK Clock Period	sclk_per		250	−	−	ns
SCLK Low Time	sclk_lo		0.4 x sclk_per	−	0.6 x sclk_per	ns
SCLK High Time	sclk_hi		0.4 x sclk_per	−	0.6 x sclk_per	ns
SDI Setup Time before Each SCLK Rising Edge	sdi_setup		45	−	−	ns
SDI Hold Time after Each SCLK Rising Edge	sdi_hold		45	−	−	ns
SDO Hold Time	sdo_hold	Depends on parasitic capacitance of SDO line	0	−	62.5 + Max (DO5_DEL)	ns

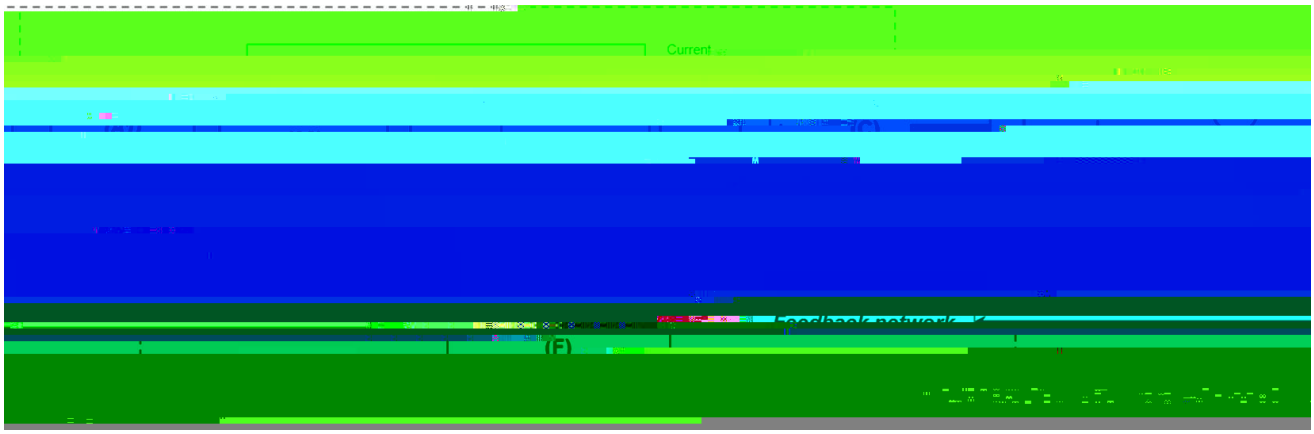
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

11. Sum of currents from, VBST, IBSTSNSxP, SDI, SCLK, CSB, and BSTSYNC pin.
12. User has to take care that sum of selected Booster regulation level BST_REG and Booster overvoltage shutdown BST_OV including accuracy and overshoots does not to exceed Absolute Maximum ratings 66 V for Buck Input voltage VINx and Boost voltage feedback input VBST.
13. Pull-down resistance for SCLK, SDI, BSTSYNC; pull-up resistance to VINT for CSB.



The built-in analog to digital converter (ADC) is an 9-bit

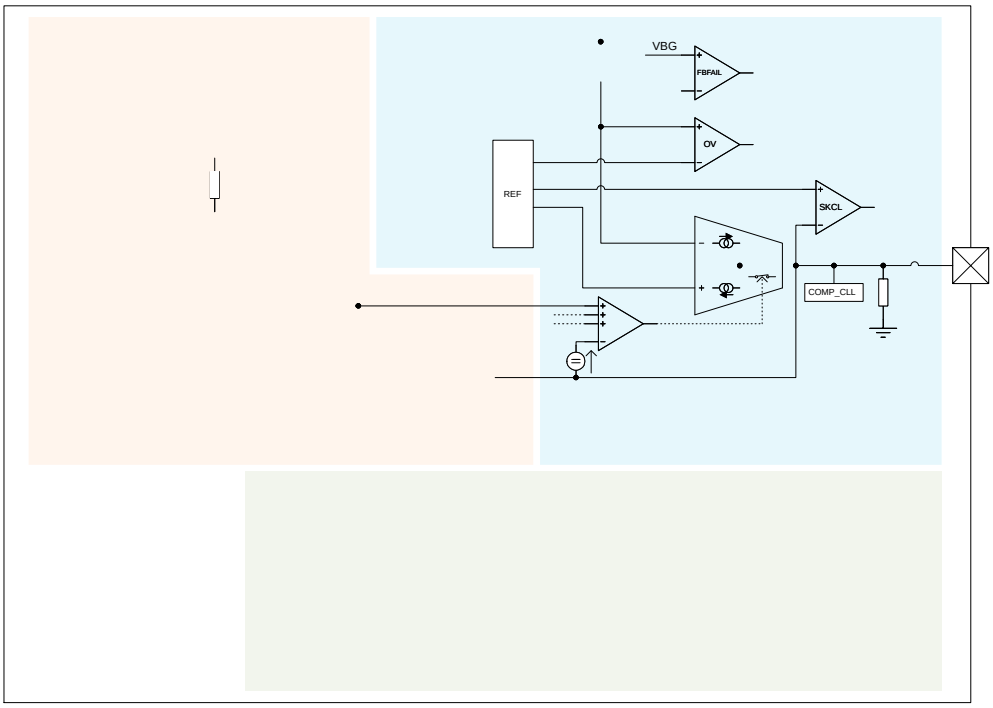
controlled variable is the boost voltage, measured directly at the device VBST pin with a unity gain feedback (block F). The picture highlights as block G all the elements contained inside the device. The regulation parameters are flexibly set by a series of SPI commands. A detailed internal boost controller block diagram is presented in the next section.



Boost Controller Detailed Internal Block Diagram

A detailed NCV78902 boost controller block diagram is provided in this section. The main signals involved are indicated, with a particular highlight on the SPI programmable parameters.

The blocks referring to the principle block diagram are also indicated. In addition, the protection specific blocks can be found (see dedicated sections for details).

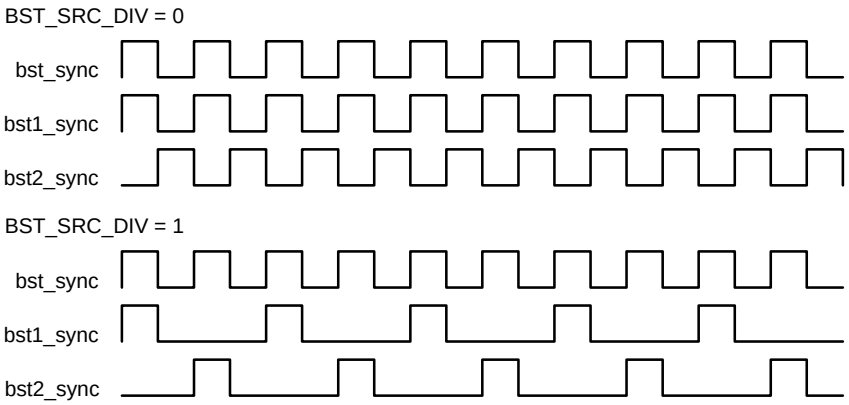

VBG
FBFAIL
OV
REF
SKCL
COMP_CLL

The maximum current must be set in order to allow the total desired booster power for the lowest battery voltage. Warning: setting the current limit too low may generate unwanted system behavior as uncontrolled de-rating of the LED light due to insufficient power.

Current limitation mode is mostly stable operating mode without subharmonic oscillations what allows to deliver maximum power to the load. Stable operation is achieved by regulating and tracking current limit threshold by dedicated algorithm. When booster phase regulates in this mode, ripple corresponding to regulation step BST_CBUF_STEP can be observed at inductor peak current. In certain border conditions some instabilities can occur, in such situation programming of longer PWM minimum on−time (BST_MIN_TON[1:0]) can help.

Booster PWM Internal Generation

This mode activated by BST_SRC = 1, creates the PWM frequency



Booster PWM Source Automatic Selection

When register BST_SRC = 3, the automatic booster PWM clock selection is activated. Switch sequence to internal clock is initialized when no rising edge on external source (bstsync_int on Figure 17) is detected within 3 consecutive rising edges of internal bst_sync clock. For this purpose, internal clock should be set to similar frequency as external source to ensure smooth transitions. Switch sequence to external clock is initialized when rising edge on external source (bstsync_int) is detected.

0	Off
1	Internal
2	External
3	Auto External/Internal

Status bit BST_SYNCFAIL set to 1 indicates that there is an issue with booster external PWM clock. Bit is set when booster is

0	100
1	150
2	200
3	300

Booster Compensator Model

A linear model of the booster controller compensator (block “A” Figure 13) is provided in this section. The protection mechanisms around are not taken into account. A type “2” network is taken into account at the VCOMP pin. The equivalent circuit is shown below:

In the Figure, e(t) represents the control error, equals to the difference $V_{BST\_VSETPOINT}(t) - V_{BST}(t)$. “” is the trans-conductance error amplifier gain (see Table 6 − BOOST CONTROLLER − VOLTAGE REGULATION PARAMETERS section), while “R_{OUT}” is the amplifier internal output resistance (parameter EA_BLR in Table 6 − BOOST CONTROLLER − VOLTAGE REGULATION PARAMETERS section). By solving the circuit in Laplace domain the following error to V_{COMP} transfer function is obtained:

$$H_{COMP} = \frac{V_{COMP}(s)}{e(s)} = G_m R_{OUT} \frac{\tau_1 s + 1}{\tau_1 \tau_p s^2 + (\tau_p + \tau_{1p}) s + 1} \quad \text{(eq. 5)}$$

The explanation of the parameters stated in the equation above follows:

$\tau_1 = R_1 C_1$
$\tau_p = R_1 C_p$
$\tau_{1p} = (R_1 + R_{OUT})\, C_1$

This transfer function model can be used for closed loop stability calculations.

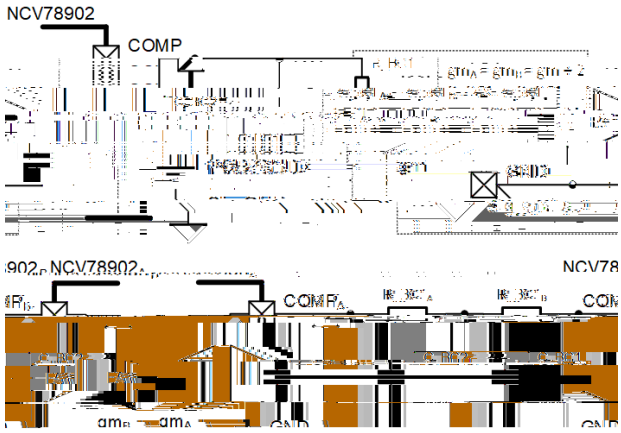
Booster PWM Skip Cycles

In case of light booster load, it is useful to reduce the number of effective PWM cycles in order to get a decrease of the input current inrush bursts and a less oscillating boost voltage. This can be obtained by using the “skip cycles” feature, programmable by SPI via BST_SKCL_THR[1:0] (see Table 6 − BOOST CONTROLLER − VOLTAGE REGULATION PARAMETERS section).

The selection defines the VCOMP voltage threshold below which the PWM is stopped, thus avoiding VBOOST oscillations in a larger voltage window.

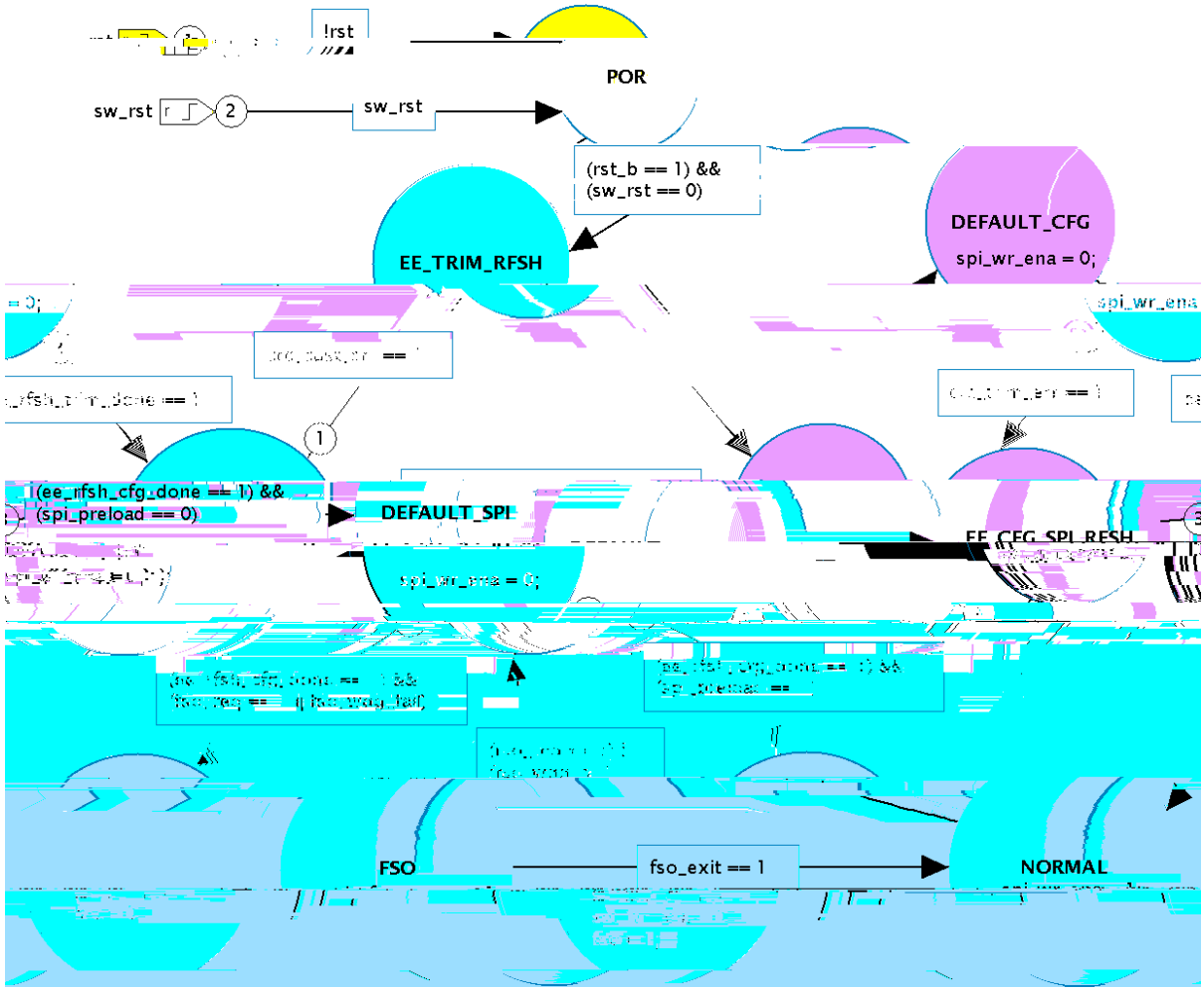
Booster Multiphase Mode Principles

The NCV78902 device supports two booster phases, which are connected together to the same VBST node,


NCV78902
COMP

invalid SPI frame. Resolution of the register is 1LSB = 62.5 ns. If CSB low pulse is longer than maximum what can be held by CSB_DUR[19:0] register (~65.5 ms), the register will keep maximum value.

Overview of all functional modes is in accordance to the state diagram on Figure 22. Individual states are described below.



Asynchronous reset is caused either by POR (POR always causes asynchronous reset − transition to reset state) or by SWRESET SPI bit being written to 1.

After the Reset, Trimming and Calibration constants are loaded from EEPROM into shadow registers and CRC check is performed. CRC check of trimming and calibration constants in shadow registers is performed also after each VTEMP measurement.

When EEPROM preload and CRC check of trimming constants in shadow registers fails also after the second trial, the CRC_EEPROM_TRIM (trimming data CRC check) error is raised and default trimming values are loaded into trimming shadow registers.

When CRC_EEPROM_TRIM (trimming data CRC check) or CRC_EEPROM_CAL (calibration data CRC check) error is detected, SPI flag TRIMERR at address 0x20 is set to 1.

Configuration registers FSO_ENTER, FSO_WDG_ENA[1:0] and FSO_WDG_CFG[1:0] are loaded from EEPROM into SPI registers after the reset before entrance into FSO or Normal mode.

SPI bit FSO_ENTER controls entrance into FSO mode; if register value is 1, FSO mode will be entered, otherwise Normal mode will be entered.

Configuration register SPI_PRELOAD (EEPROM address 0x04), which is loaded from EEPROM after the reset, controls whether in Normal mode SPI registers will be loaded with values from EEPROM or with default SPI values. When SPI_PRELOAD is 1, SPI registers will be preloaded from EEPROM and this mode can be referred as Stand-Alone mode.

Customer EEPROM data are protected by CRC_EEPROM_CUST CRC check. When CRC_EEPROM_CUST (customer data CRC check) error is detected, SPI register EEPROM_READFAIL is set to 1 and default values will be loaded into SPI control registers.

FSO (Fail-Safe Operation) mode can be used for the purpose of **Fail-Safe** functionality (chip functionality definition in fail-safe mode when the external microcontroller functionality is not guaranteed).

FSO mode is entered in the following situations:

- After POR when control registers are preloaded and FSO_ENTER contains 1,
- From Normal mode when rising edge on FSO_ENTER SPI bit is detected and at the same moment SPI bit FSO_EXIT is 0,
- From Normal mode when Watchdog time-out elapses (indicated by FSO_WDG_FAIL).

When transitioning into FSO mode, the EEPROM refresh is performed. Please note, that when CRC error has been detected, SPI register EEPROM_READFAIL is set to 1, FSO mode is not entered and default values are loaded into SPI registers.

FSO mode can be exited when rising edge on FSO_EXIT SPI bit is detected and at the same moment SPI bit FSO_ENTER is 0.

FSO bit in status register 0x20 (and its mirror in SPI frame) is set to 1 when device is inside the FSO mode. FSO status bit is 0 outside the FSO mode.

In FSO mode write operations are allowed to SWRESET, FSO_ENTER, FSO_EXIT, FSO_WDG_ENA[1:0] and FSO_WDG_CFG[1:0] control registers at address 0x1D.

Stand-Alone modes can be used for the purpose of default power-up operation of the chip (**Stand-Alone** functionality without external microcontroller or preloading of the registers with default content for default operation before microcontroller starts sending SPI commands for chip settings).

Stand-Alone mode is in fact Normal mode where SPI registers were preloaded from EEPROM after the reset and is entered in the following situation:

- After POR when configuration register SPI_PRELOAD, which is loaded from EEPROM, contains 1.

During SPI preload, the EEPROM refresh is performed. Please note, that when CRC error has been detected, SPI register EEPROM_READFAIL is set to 1 and default values are loaded into SPI registers.

In Stand-Alone mode, when SPI bus is not used, the SDO pin can be configured as failure indicator. See the following chapter for more details. Other unused SPI pins should be tied to GND.

SDO pin can be used as failure indicator (active low) when bit BST_FAIL_OUT at address 0x1D is set to 1.

SDO output will be asserted low when the following condition persists for more than 49 ms:

not SDO = (CSB pin = 1) and (and BST_FAIL_OUT)

Please note that is used also in SPI read frame in FAILURE_FLAGS[5:0] section, please see SPI Read Frame description for more details.

Meaning of the is the following:

BSTERR = (not BST1_RUNNING and BST1_EN) or (not BST2_RUNNING and BST2_EN) or TSD or ((BSTx_REGSTATUS = 1 or BSTx_REGSTATUS = 2) and BST_ILIM_FMASK)

Watchdog is restarted each time the valid SPI frame is received. When Watchdog is not properly restarted and time−out elapses, transition into FSO mode is started.

The watchdog can be configured and activated according to Table 14:

The NCV78902 SPI transfer size is 32 bits. Maximum communication SPI speed supported by NCV78902 is 4 MHz.

During an SPI transfer, the data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line (CLK) synchronizes shifting and sampling of the information on the two serial data lines: DO and DI. The DO signal is the output from the Slave (NCV78902), and the DI signal is the output from the Master.

Referring to the previous picture, the read frame coming from the master (into the SDI) is composed from the following fields:

- Bit[31] (MSB): CMD bit = 0 for read operation,
- Bits[30:25]: 6 bits READ ADDRESS field,
- Bits[24:4]: 21 bits zeroes field,
- Bits[3:0]: 4 bits CRC field computed over CMD, READ_ADDR and IGNORED in shown order from MSB to LSB.

Device in the same frame provides to the master (on the DO):

- Bit[31] (MSB): SPI ERROR bit set in case last received SPI frame was invalid,
- Bits[30:25]: FAILURE_FLAGS[5:0] field composed from:
  - HWR flag (mirror of HWR SPI flag),
  - TW flag (mirror of TW SPI flag),
  - FSO flag (mirror of FSO SPI flag),
  - BSTERR fail status; please see Failure Output chapter to see details from which bits these fail status indicators are composed,
- Bits[24:4]: actual data from address READ_ADDR,
- Bits[3:0]: ECRC (extended CRC) computed over SPIERR, FAILURE_FLAGS, READ_DATA, CMD (which has to be extended to 2 bits by one zero from left) and READ_ADDR in shown order from MSB to LSB.

Read frame provides data from the required address to the output within the same frame (in frame response), thus achieving the lowest communication latency.

Received and transmitted frames are protected by CRC with following parameters:

- CRC length is 4 bits,
- CRC polynomial 0x9 (Koopman’s notation; x4+x+1),
- CRC initialization value 0xF.

SPI communication framing error is detected by the NCV78902 in the following situations:

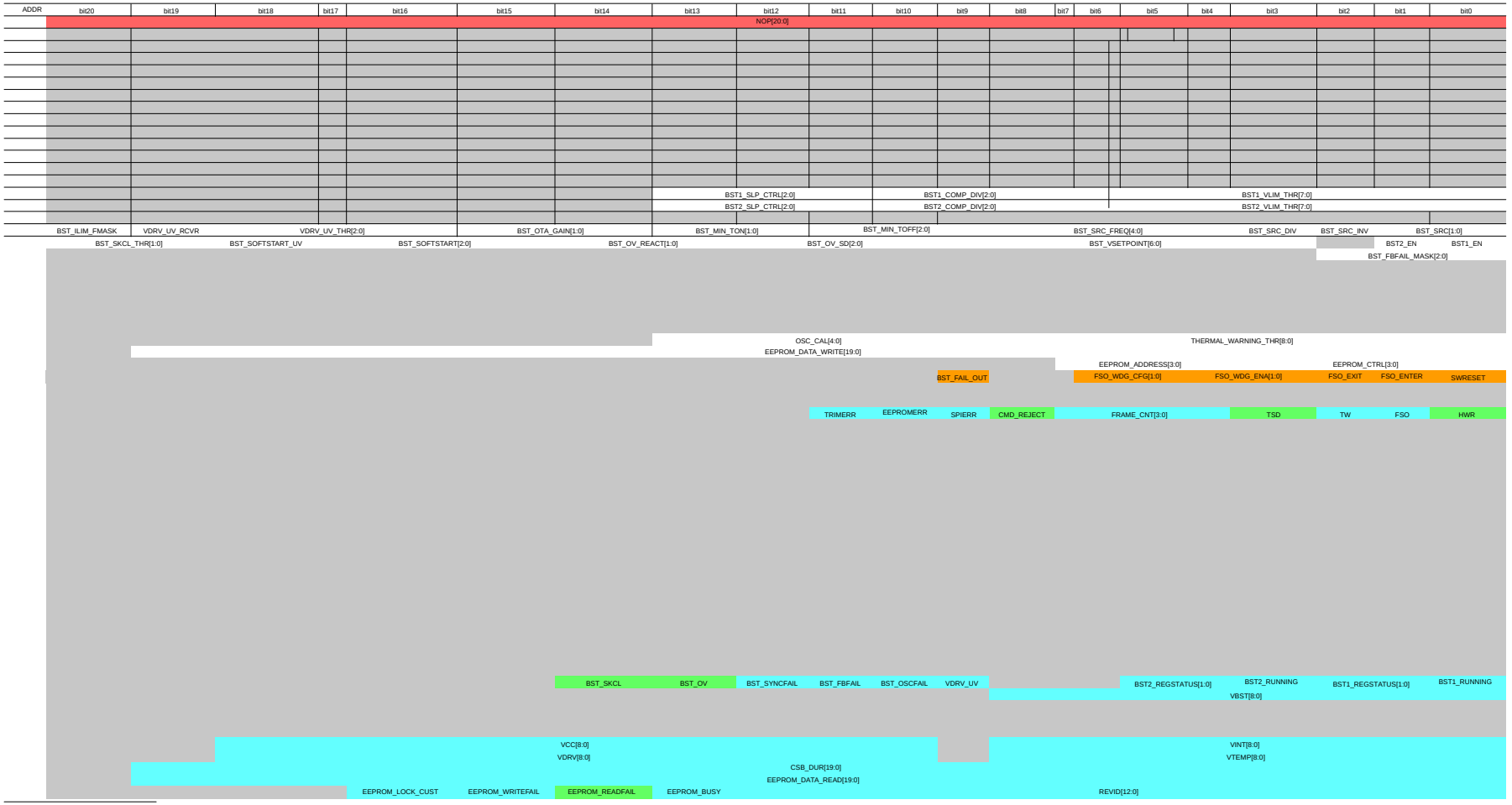
- Not zero or 32 CLK pulses are received during the active-low CSB signal;
- CRC calculated from all received bits is not equal to zero;
-

```
#

//          4                      "   "                "   ".        4
      CalcCRCfromByteArray(        * data,          length)
                    CRC_POLY = 0 03   //         4 +   + 1 (0 03        , 0 0        )
                    CRC_INIT = 0 0    //

      crc = 0                         //
      bit = 0                         //

  //
  (       byteIdx = 0                    ++)
     (          == 0)
         //                                      2
```


ADDR
bit20
bit19
bit18
bit17
bit16
bit15
bit14
bit13
bit12
bit11
bit10
bit9
bit8
bit7
bit6
bit5
bit4
bit3
bit2
bit1
bit0
NOP[20:0]
BST1_SLP_CTRL[2:0]
BST1_COMP_DIV[2:0]
BST1_VLIM_THR[7:0]
BST2_SLP_CTRL[2:0]
BST2_COMP_DIV[2:0]
BST2_VLIM_THR[7:0]
BST_ILIM_FMASK
VDRV_UV_RCVR
VDRV_UV_THR[2:0]
BST_OTA_GAIN[1:0]
BST_MIN_TON[1:0]
BST_MIN_TOFF[2:0]
BST_SRC_FREQ[4:0]
BST_SRC_DIV
BST_SRC_INV
BST_SRC[1:0]
BST_SKCL_THR[1:0]
BST_SOFTSTART_UV
BST_SOFTSTART[2:0]
BST_OV_REACT[1:0]
BST_OV_SD[2:0]
BST_VSETPOINT[6:0]
BST2_EN
BST1_EN
BST_FBFAIL_MASK[2:0]
OSC_CAL[4:0]
THERMAL_WARNING_THR[8:0]
EEPROM_DATA_WRITE[19:0]
EEPROM_ADDRESS[3:0]
EEPROM_CTRL[3:0]
BST_FAIL_OUT
FSO_WDG_CFG[1:0]
FSO_WDG_ENA[1:0]
FSO_EXIT
FSO_ENTER
SWRESET
TRIMERR
EEPROMERR
SPIERR
CMD_REJECT
FRAME_CNT[3:0]
TSD
TW
FSO
HWR
BST_SKCL
BST_OV
BST_SYNCFAIL
BST_FBFAIL
BST_OSCFAIL
VDRV_UV
BST2_REGSTATUS[1:0]
BST2_RUNNING
BST1_REGSTATUS[1:0]
BST1_RUNNING
VBST[8:0]
VCC[8:0]
VINT[8:0]
VDRV[8:0]
VTEMP[8:0]
CSB_DUR[19:0]
EEPROM_DATA_READ[19:0]
EEPROM_LOCK_CUST
EEPROM_WRITEFAIL
EEPROM_READFAIL
EEPROM_BUSY
REVID[12:0]

Default value of all SPI registers after POR is 0x00 if not

(continued)

EEPROM ADDRESS[3:0]	Bits [7:4] – ADDR_0x1C	
EEPROM_CTRL[3:0]	Bits [3:0] – ADDR_0x1C	EEPROM CommandE

(continued)

CSB_DUR[19:0]	Bits [19:0] – ADDR_0x3D	Measured Duration of CSB low pulse

EEPROM_DATA_READ[19:0]	Bits [19:0] – ADDR_0x3E	EEPROM Read Data

EEPROM_LOCK_CUST	Bit 16 – ADDR_0x3F	EEPROM Customer Data Locked
EEPROM_WRITEFAIL	Bit 15 – ADDR_0x3F	EEPROM Data Write Failure
EEPROM_READFAIL	Bit 14 – ADDR_0x3F	EEPROM Data CRC check Failure, Latched
EEPROM_BUSY	Bit 13 – ADDR_0x3F	EEPROM Busy
REVID[12:0]	Bits [12:0] – ADDR_0x3F	Revision ID of the Device

ADDR	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x04			BST_FAIL_OUT			FSO_WDG_CFG[1:0]		FSO_WDG_ENA[1:0]		FSO_ENTER	SPI_PRELOAD	THERMAL_WARNING_THR[8:0]								
0x05		BST_SOFTSTART_UV	BST_ILIM_FMASK	BST_OTA_GAIN[1:0]		BST_SOFTSTART[2:0]			BST_OV_REACT[1:0]		BST_OV_SD[2:0]	BST_VSETPOINT[6:0]								
0x06	VDRV_UV_RCVR	VDRV_UV_THR[2:0]			BST_SKCL_THR[1:0]		BST_MIN_TON[1:0]		BST_MIN_TOFF[2:0]			BST_SRC_FREQ[4:0]					BST_SRC_DIV	BST_SRC_INV	BST_SRC[1:0]	
0x07			BST_FBFAIL_MASK[2:0]			BST1_SLP_CTRL[2:0]			BST1_COMP_DIV[2:0]			BST1_VLIM_THR[7:0]								BST1_EN
0x08						BST2_SLP_CTRL[2:0]			BST2_COMP_DIV[2:0]			BST2_VLIM_THR[7:0]								BST2_EN
0x09	EEPROM_LOCK_CUST				CRC_EEPROM_CUST[15:0]															

	Customer
	unused

EEPROM memory serves as persistent storage for Customer configuration and for **onsemi** calibration, trimming and test data. EEPROM memory is organized as 51 words, each 20 bits wide. The access to the memory is word-based.

The NCV78902 supports following operations with EEPROM memory:

- EEPROM_CTRL[3:0] = 0xxx [binary]: EEPROM in Power-down state (no operation)
- EEPROM_CTRL[3:0] = 1xxx [binary]: **Enable**
- EEPROM_CTRL[3:0] = 1001 [binary]: **Read** − data addressed by SPI register EEPROM_ADDRESS[3:0]

This section contains instructions for the NCV78902 PCB layout application design. Although this guide does

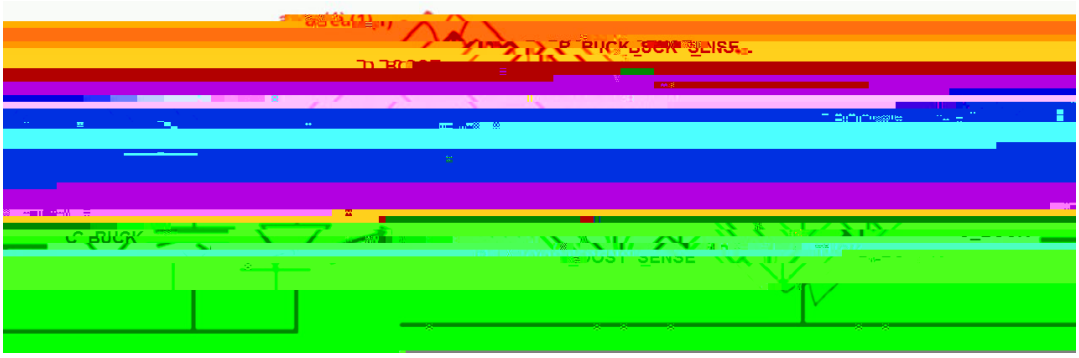
connected directly to the chip ground pin to avoid noise coming from other portions of the PCB ground. In addition a ground ring shall provide extra shielding ground around.

It has to be ensured that VGATE signals do not interfere with other signals like COMP or input of the IMAX or IREG comparators.

The VDD decoupling capacitor has to be connected directly to the VDD and ground pins with separate PCB tracks to avoid coupling of the ground shift on the PCB into the chip.

It is suggested in general to have a good metal connection to the ground and to keep it as continuous as possible, not interrupted by resistors or jumpers. In additions, PCB loops for power lines should be minimized. A simplified application schematic is shown in the next figure to better focus on the theoretical explanation. When a DC voltage is applied to the VBB, at the left side of the boost inductor L_BOOST, a DC voltage also appears on the right side of L_BUCK and on the C_BUCK. However,

due to the switching operation (boost and buck), the applied voltage generates AC currents flowing through the red area (1). These currents also create time variable voltages in the area marked in green (2). In order to minimize the radiation due to the AC currents in area 1, the tracks' length between L_BOOST and the pair L_BUCK plus C_BUCK must be kept low. At the contrary, if long tracks would be used, a bigger parasitic capacitance in area 2 would be created, thus increasing the coupled EMC noise level.

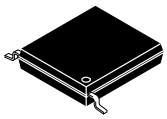


In case of typical application with current sensing over sensing resistor RSN_BST_1/2, high voltage pin VBST (pin 16) is located directly next to the pin with low voltage IBSTSNS1P (pin 15). In case of sensing over MOSFET RDSon, switching signal with levels between high booster voltage and GND will appear on pin IBSTSNS1P (pin 15) which is located between high voltage pin VBST (pin 16) and low voltage pin IBSTSNS1N (pin 14). In either case, if there is a need to improve spacing between high and low voltage pins due to requirements of IPC2221 or similar standard, it can be considered to design soldering footprint with narrower pads than recommended in Soldering footprint.

			†
NCV78902DE0R2G	N78902-1	TSSOP−16 WB (Pb-Free)	4000 / Tape & Reel

*For additional information on our Pb−Free strategy and soldering details, please download the Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



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