D , 300 A, D J G .H C 8164

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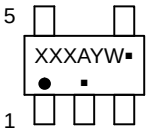
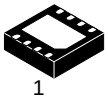
MARKING DIAGRAMS

TSOP−5
CASE 483



WDFNW6 2x2, 0.65P
CASE 511DW



DFNW8 3x3, 0.65P
CASE 507AD

XXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
M = Month Code
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

Features

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- ±2% Accuracy Over Load and Temperature
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Typical Applications

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- –
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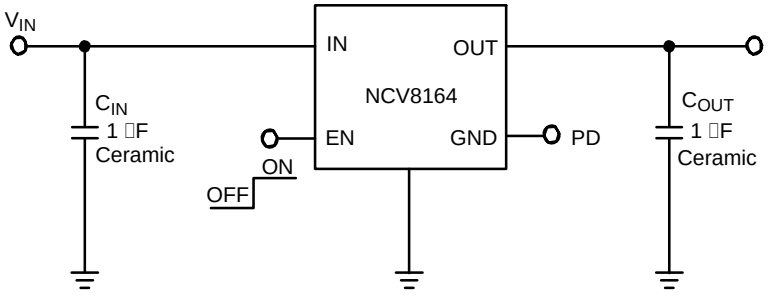

Figure 1. Typical Application Schematics

PIN FUNCTION DESCRIPTION

Pin No. TSOP−5	Pin No. WDFNW6	Pin No. DFNW8	Pin Name	Description
1	6	8	IN	Input voltage supply pin
5	1	1	OUT	Regulated output voltage. The output should be bypassed with small 1 □F ceramic capacitor
3	4	7	EN	Chip enable: Applying V_{EN} < 0.25 V disables the regulator, Pulling V_{EN} > 0.7 V enables the LDO
4 / –	3	3	PG	Power Good, open collector. Use 10 k□ to 100 k□ pull−up resistor connected to output or input voltage
2	5	6	GND	Common ground connection
– / 4	2	2	ADJ	Adjustable output feedback pin (for adjustable version only)
–	2	2	SNS	Sense feedback pin. Must be connected to OUT pin on PCB (for fixed versions only)
–	–	4, 5	N/C	Not connected, pin can be tied to ground plane for better power dissipation
–	EPAD	EPAD	EPAD	Expose pad should be tied to ground plane for better power dissipation

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 to 6	V
Output Voltage	V_{OUT}	−0.3 o V_{IN}+0.3, ma . 6	V
Chip Enable Input	V_{CE}	−0.3 to 6	V
Power Good Voltage	V_{PG}	−0.3 to 6	V
Power Good Current	I_{PG}	30	mA
Output Short Circuit Duration	t_{SC}	unlimited	s
Maximum Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Charged Device Model (Note 2)	ESD_{CDM}	1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
THERMAL CHARACTERISTICS, TSOP−5 PACKAGE			
Thermal Resistance, Junction−to−Ambient (Note 3)	R□JA	158	°C/W
Thermal Resistance, Junction−to−Case (top)	R□JC(top)	155	°C/W
Thermal Resistance, Junction−to−Case (bottom) (Note 4)	R□JC(bot)	102	°C/W
Thermal Resistance, Junction−to−Board	R□JB	197	°C/W
Characterization Parameter, Junction−to−Top	□JT	40	°C/W
Characterization Parameter, Junction−to−Board	□JB	82	°C/W
THERMAL CHARACTERISTICS, WDFNW6−2X2, 0.65 PITCH PACKAGE			
Thermal Resistance, Junction−to−Ambient (Note 3)	R□JA	51	°C/W
Thermal Resistance, Junction−to−Case (top)	R□JC(top)	142	°C/W
Thermal Resistance, Junction−to−Case (bottom) (Note 4)	R□JC(bot)	2.0	°C/W
Thermal Resistance, Junction−to−Board	R□JB	117	°C/W
Characterization Parameter, Junction−to−Top	□JT	1.9	°C/W
Characterization Parameter, Junction−to−Board	□JB	7.7	°C/W
THERMAL CHARACTERISTICS, DFNW8−3X3, 0.65 PITCH PACKAGE			
Thermal Resistance, Junction−to−Ambient (Note 3)	R□JA	50	°C/W
Thermal Resistance, Junction−to−Case (top)	R□JC(top)	142	°C/W
Thermal Resistance, Junction−to−Case (bottom) (Note 4)	R□JC(bot)	7.9	°C/W
Thermal Resistance, Junction−to−Board	R□JB	125	°C/W
Characterization Parameter, Junction−to−Top	□JT	2.0	°C/W
Characterization Parameter, Junction−to−Board	□JB	7.5	°C/W

3. The junction−to−ambient thermal resistance under natural convection is obtained in a simulation on a high−K board, following the JEDEC51.7 guidelines with assumptions as above, in an environment described in JESD51−2a.
4. The junction−to−case (bottom) thermal resistance is obtained by simulating a cold plate test on the IC exposed pad. Test description can be found in the ANSI SEMI standard G30−88.

TYPICAL CHARACTERISTICS

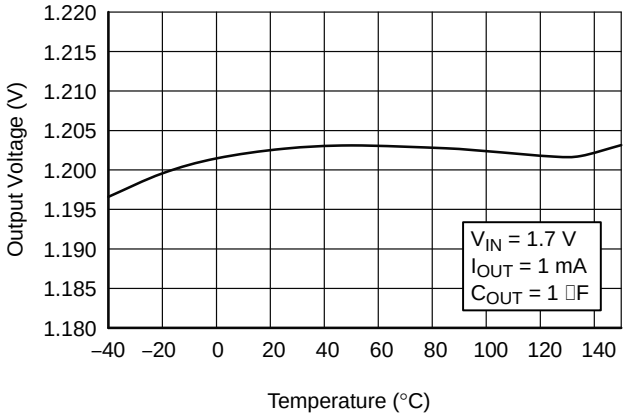

Figure 2. Output Voltage vs. Temperature − V_{OUT} = 1.2 V

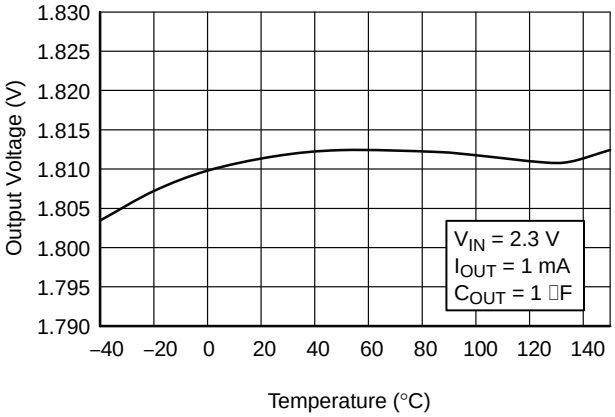

Figure 3. Output Voltage vs. Temperature − V_{OUT} = 1.8 V

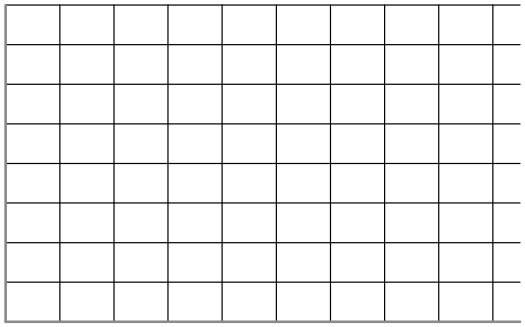

Figure 4. Output Voltage vs. Temperature − V_{OUT} = 3.3 V

Figure 5. Dropout Voltage vs. Temperature − V_{OUT} = 1.2 V

Figure 6. Dropout Voltage vs. Temperature − V_{OUT} = 1.8 V

Figure 7. Dropout Voltage vs. Temperature − V_{OUT} = 3.3 V

Adjustable Version

$$V_{OUT} = V_{FIX} \times (1 + R1/R2) \quad \text{(eq. 4)}$$

□.

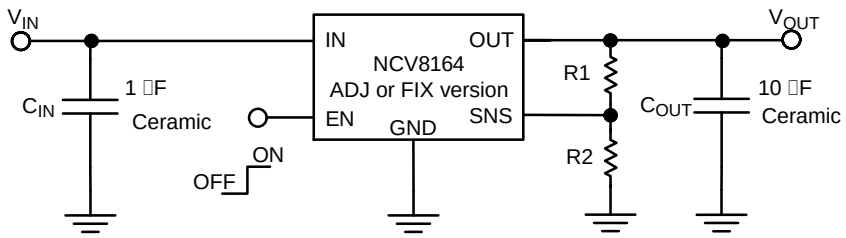

Figure 16. Adjustable Variant Application

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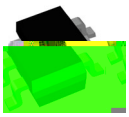
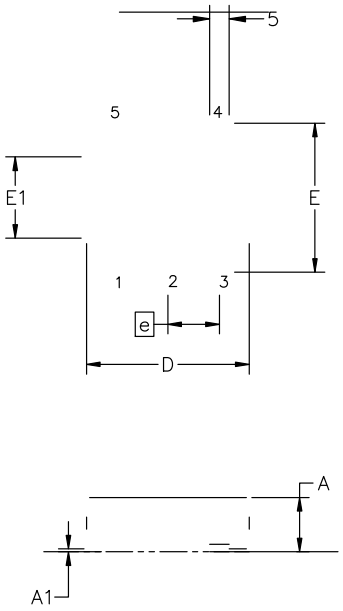
ORDERING INFORMATION

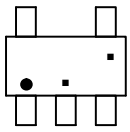
Device part no.	Voltage Option	Marking	Option	Package

TSOP−5 3.00x1.50x0.95, 0.95P

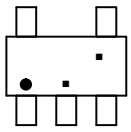




GENERIC
MARKING DIAGRAM*



Analog



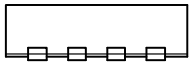
Discrete/Logic

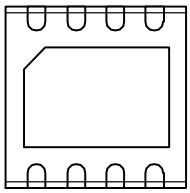
DFNW8 3x3, 0.65P
CASE 507AD
ISSUE A

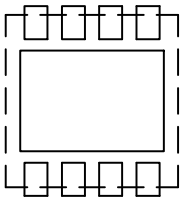
SCALE 2:1

DATE 15 JUN 2018

NOTES:







WDFNW6 2x2, 0.65P