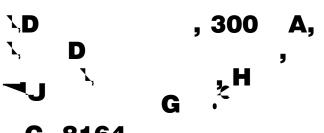
onsemi



C 8164

The NCV8164 is a 300 mA LDO, next generation of high PSRR, ultra-low noise and low dropout regulators with Power Good open collector output. Designed to meet the requirements of RF and sensitive analog circuits, the NCV8164 device provides ultra-low noise, high PSRR and low quiescent current. The device also offer excellent load/line transients. The NCV8164 is designed to work with a 1 F input and a 1 F output ceramic capacitor. It is available in industry standard TSOP-5, WDFNW6 0.65P, 2 mm x 2 mm and DFNW8 0.65P, 3 mm x 3 mm.

Features

- Operating Input Voltage Range: 1.6 V to 5.5 V
- Available in Fixed Voltage Option: 1.2 V to 5.0 V
- Adjustable Version Reference Voltage: 1.2 V
- $\pm 2\%$ Accuracy Over Load and Temperature
- Ultra Low Quiescent Current Typ. 30 A
- Standby Current: Typ. 0.1 A
- Very Low Dropout: 110 mV at 300 mA for 3.3 V Variant
- Ultra High PSRR: Typ. 85 dB at 10 mA, f = 1 kHz
- Ultra Low Noise: 9 V_{RMS} (Fixed Version)
- Stable with a 1 F Small Case Size Ceramic Capacitors
- Available in TSOP–5 3 mm x 1.5 mm x 1 mm CASE 483
 - WDFNW6 2 mm x 2 mm x 0.75 mm CASE 511DW
 DFNW8 3 mm x 3 mm x 0.9 mm CASE 507AD
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Communication Systems
- In-Vehicle Networking
- Telematics, Infotainment and Clusters
- General Purpose Automotive

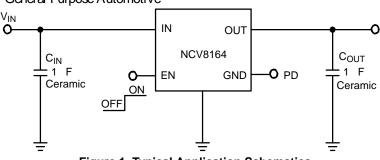
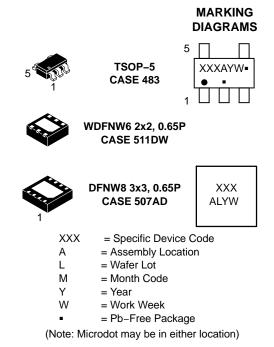


Figure 1. Typical Application Schematics



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PIN FUNCTION DESCRIPTION

Pin No. TSOP-5	Pin No. WDFNW6	Pin No. DFNW8	Pin Name	Description			
1	6	8	IN	Input voltage supply pin			
5	1	1	OUT	Regulated output voltage. The output should be bypassed with small 1 F ceramic capacitor			
3	4	7	EN	Chip enable: Applying V_{EN} < 0.25 V disables the regulator, Pulling V_{EN} > 0.7 V enables the LDO			
4 / -	3	3	PG	Power Good, open collector. Use 10 k to 100 k pull-up resistor connected to output or input voltage			
2	5	6	GND	Common ground connection			
- / 4	2	2	ADJ	Adjustable output feedback pin (for adjustable version only)			
-	2	2	SNS	Sense feedback pin. Must be connected to OUT pin on PCB (for fixed versions only)			
-	-	4, 5	N/C	Not connected, pin can be tied to ground plane for better power dissipation			
_	EPAD	EPAD	EPAD	Expose pad should be tied to ground plane for better power dissipation			

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V _{IN}	-0.3 to 6	V
Output Voltage	V _{OUT}	-0.3 oV _{IN} +0.3, ma .6	V
Chip Enable Input	V _{CE}	-0.3 to 6	V
Power Good Voltage	V _{PG}	-0.3 to 6	V
Power Good Current	I _{PG}	30	mA
Output Short Circuit Duration	tsc	unlimited	s
Maximum Junction Temperature	TJ	150	°C
Storage Temperature	T _{STG}	-55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD _{HBM}	2000	V
ESD Capability, Charged Device Model (Note 2)	ESD _{CDM}	1000	V

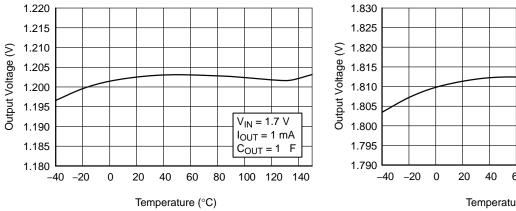
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

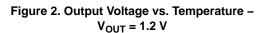
THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
THERMAL CHARACTERISTICS, TSOP-5 PACKAGE			•
Thermal Resistance, Junction-to-Ambient (Note 3)	R ja	158	°C/W
Thermal Resistance, Junction-to-Case (top)	R JC(top)	155	°C/W
Thermal Resistance, Junction-to-Case (bottom) (Note 4)	R JC(bot)	102	°C/W
Thermal Resistance, Junction-to-Board	Rјв	197	°C/W
Characterization Parameter, Junction-to-Top	JT	40	°C/W
Characterization Parameter, Junction-to-Board	JB	82	°C/W
THERMAL CHARACTERISTICS, WDFNW6-2X2, 0.65 PITCH PACKAG	βE		
Thermal Resistance, Junction-to-Ambient (Note 3)	R ja	51	°C/W
Thermal Resistance, Junction-to-Case (top)	R JC(top)	142	°C/W
Thermal Resistance, Junction-to-Case (bottom) (Note 4)	R JC(bot)	2.0	°C/W
Thermal Resistance, Junction-to-Board	Rјв	117	°C/W
Characterization Parameter, Junction-to-Top	JT	1.9	°C/W
Characterization Parameter, Junction-to-Board	JB	7.7	°C/W
THERMAL CHARACTERISTICS, DFNW8-3X3, 0.65 PITCH PACKAGE			
Thermal Resistance, Junction-to-Ambient (Note 3)	R JA	50	°C/W
Thermal Resistance, Junction-to-Case (top)	R JC(top)	142	°C/W
Thermal Resistance, Junction-to-Case (bottom) (Note 4)	R JC(bot)	7.9	°C/W
Thermal Resistance, Junction-to-Board	RJB	125	°C/W
Characterization Parameter, Junction-to-Top	JT	2.0	°C/W
Characterization Parameter, Junction-to-Board	JB	7.5	°C/W

The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a high-K board, following the JEDEC51.7 guidelines with assumptions as above, in an environment described in JESD51-2a.
 The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the IC exposed pad. Test description can be found in the ANSI SEMI standard G30-88.

TYPICAL CHARACTERISTICS





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		1		

Figure 4. Output Voltage vs. Temperature - $V_{OUT} = 3.3 V$

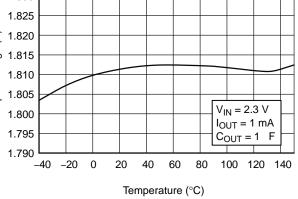


Figure 3. Output Voltage vs. Temperature -V_{OUT} = 1.8 V

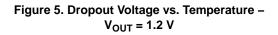


Figure 6. Dropout Voltage vs. Temperature -V_{OUT} = 1.8 V

Figure 7. Dropout Voltage vs. Temperature -V_{OUT} = 3.3 V

Adjustable Version

Not only adjustable version, but also any fixed version can be used to create adjustable voltage, where original fixed voltage becomes reference voltage for resistor divider and feedback loop. Output voltage can be equal or higher than original fixed option, while possible range is from 1.2 V up to 5.0 V. Figure 16 shows how to add external resistors to increase output voltage above fixed value.

Output voltage is then given by equation

$$V_{OUT} = V_{FIX} \times (1 + R1/R2)$$
 (eq. 4)

where V_{FIX} is voltage of original fixed version (from 1.2 V up to 5.0 V) or adjustable version (1.2 V). Do not operate the device at output voltage about 5.2 V, as device can be damaged.

In order to avoid influence of current flowing into SNS pin to output voltage accuracy (SNS current varies with voltage option and temperature, typical value is 300 nA) it is recommended to use values of R1 and R2 below 500 k.

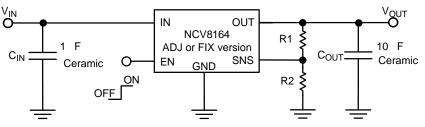


Figure 16. Adjustable Variant Application

Please note that output noise is amplified by V_{OUT} / V_{FIX} ratio. For example, if original 1.2 V fixed variant is used to create 3.6 V output voltage, output noise is increased 3.6 / 1.2 = 3 times and real value will be 3×9 Vrms = 27 Vrms. For noise sensitive applications it is

recommended to use as high fixed variant as possible – for example in case above it is better to use 3.3 V fixed variant to create 3.6 V output voltage, as output noise will be amplified only $3.6/3.3 = 1.09 \times (9.8$ Vrms).

Marking

ORDERING INFORMATION

Device part no.

Voltage Option

Option

Package

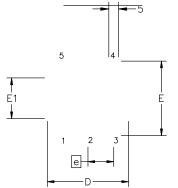


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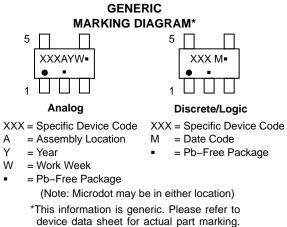
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TSOP-5 3.00x1.50x0.95, 0.95P **CASE 483** ISSUE P

DATE 01 APR 2024







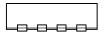
- *This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

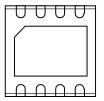
DFNW8 3x3, 0.65P CASE 507AD ISSUE A

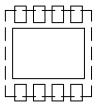
SCALE 2:1

DATE 15 JUN 2018

NOTES:







WDFNW6 2x2, 0.65P C

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