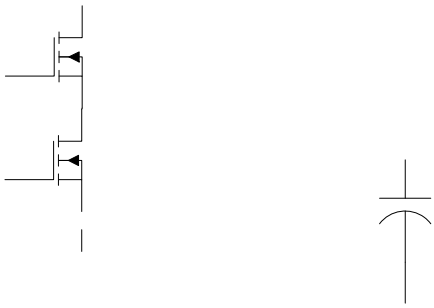


Figure 1. 5 V Application Schematic Example

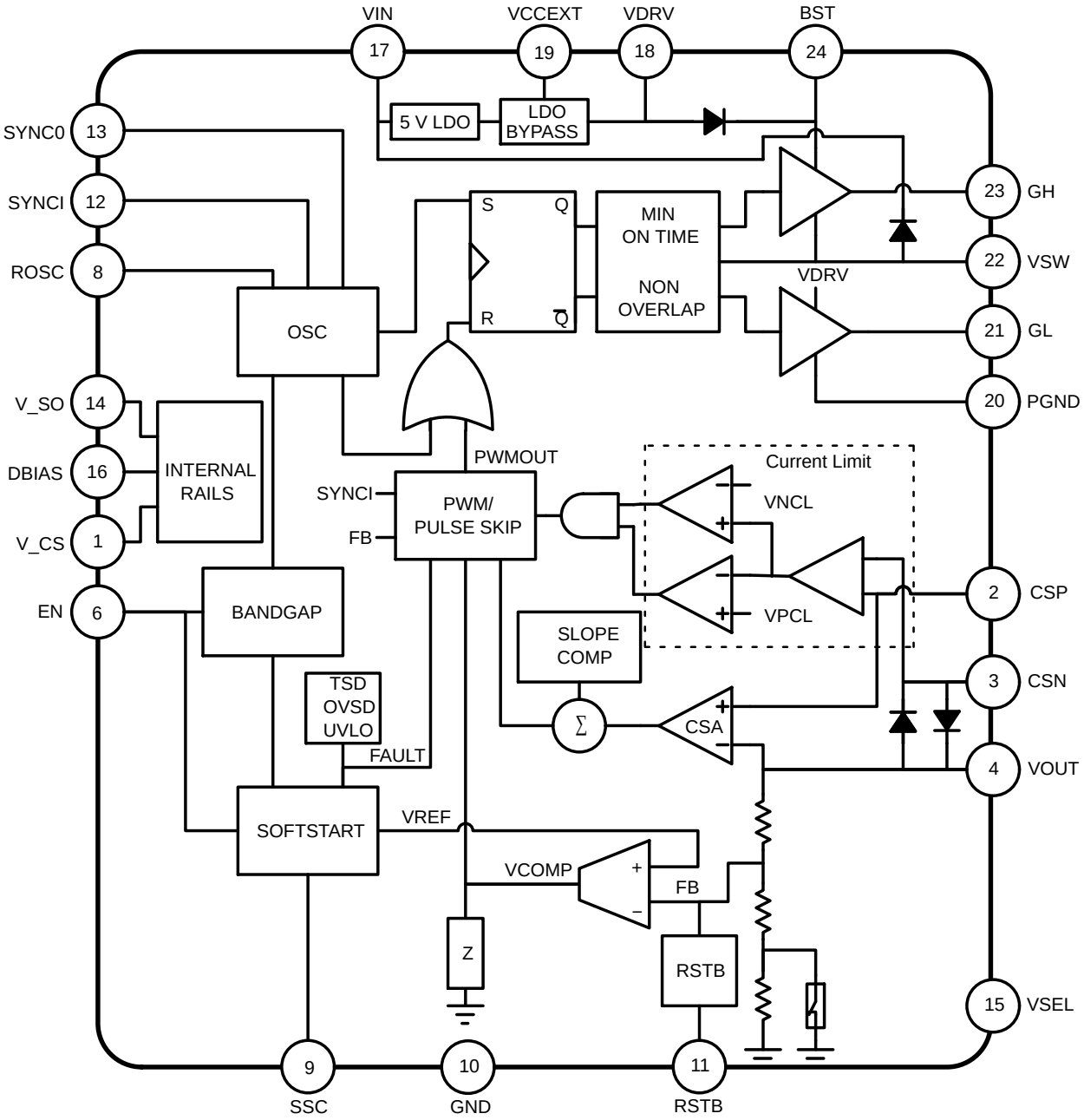


Figure 3. Simplified Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No. QFN24	Pin Name	Description
1	V_CS	Supply input for the internal current sense amplifier. Not intended for external use. Application board requires a 0.1 μF decoupling capacitor located next to IC referenced to quiet GND.
2	CSP	Differential current sense amplifier non−inverting input.
3	CSN	Differential current sense amplifier inverting input.
4	VOUT	SMPS's voltage feedback. Inverting input to the voltage error amplifier. Connect VOUT to nearest point−of−load.
5	NC	No connection (Note 1)
6	EN	Logic level inputs for enabling the controller. May be connected to battery.
7	NC	No Connection (Note 1)
8	ROSC	Use a resistor to ground to raise the frequency above default value.
9	SSC	Soft−start current source output. A capacitor to ground sets the soft−start time.
10	GND	Signal ground. Ground reference for the internal logic, analog circuitry and the compensators.
11	RSTB	Reset with adjustable delay. Goes low when the output is out of regulation.
12	SYNCI	A logic low enables Low I_Q capable operating mode. External synchronization is realized with an external clock. A logic high enables continuous synchronous operating mode (low I_Q mode is disabled). Ground this pin if not used.
13	SYNCO	Synchronization output active in synchronous operation mode. Refer to table for activation delay when coming out of low I_Q mode. Connecting to the SYNCI pin of a downstream NCV881930 results in synchronized operation.
14	V_SO	Supply voltage for the SYNCO output driver. Not intended for external use. Application board requires a 0.1 μF decoupling capacitor located next to IC referenced to quiet GND.
15	VSEL	Output programmed to VSEL_LO when connected to ground or when pin is not connected. Output programmed to VSEL_HI when connected to DBIAS via a 10 kΩ resistor (optional). Voltage setting option will be latched prior to PWM soft−start. Latch will be reset whenever the EN pin is toggled or during a UVLO event.
16	DBIAS	IC internal power rail. Not intended for external use other than for VSEL. Application board requires a 0.1 μF decoupling capacitor located next to IC referenced to quiet GND.
17	VIN	Input voltage for controller, may be connected to battery.
18	VDRV	5 V linear regulator supply for powering NFET gate drive circuitry and supply for bootstrap capacitor.
19	VCCEXT	External 5 V bias supply. Overrides internal high voltage LDO when used. Application board requires a 1 μF decoupling capacitor located next to IC referenced to PGND.
20	PGND	Power ground. Ground reference for the high−current path including the N−FETs and output capacitor.
21	GL	Push−pull driver output that swings between VDRV and PGND to drive the gate of an external low side N−FET of the synchronous buck power supply.
22	VSW	Terminal of the high side push−pull gate driver connected to the source of the high side N−FET of the synchronous buck power supply.
23	GH	Push−pull driver output that swings between SW and BST to drive the gate of an external high side N−FET of the synchronous buck power supply.
24	BST	The BST pin is the supply rail for the gate drivers. A 0.1 μF capacitor must be connected between this pin and the VSW pin. Bootstrap pin to be connected with an external capacitor for powering the high side NFET gate with SW + (VDRV – 0.5 V) and PGND. Blocking diode is internal to the IC.
EPAD		Connect to pin 20 (electrical ground) and to a low thermal resistance path to the environment.

1. True no connect. Printed circuit board traces are allowable.

Table 2. MAXIMUM RATINGS (Voltages with respect to GND unless otherwise indicated)

Rating	Symbol	Value	Unit
DC Supply Voltage (Note 2)	EN, VIN, V_CSg		

Table 4. ELECTRICAL CHARACTERISTICS
(V_{EN} = V_{BAT} = V_{IN} = 4.5 V to 37 V, V_{BST} = V_{SW} + (V_{DRV} – 0.5 V), C_{BST} = 0.1 μF, C_{DRV} = 1 μF. Min/Max values are valid for the temperature range −40°C < T_J < 150°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
VIN OVERVOLTAGE SHUTDOWN MONITOR						
Overvoltage stop threshold		V_{OVSP}	37.0	38.0	39.0	V
Overvoltage hysteresis		V_{OVHY}	0.5	1.0	1.5	V
QUIESCENT CURRENT						

Table 4. ELECTRICAL CHARACTERISTICS
(V_{EN} = V_{BAT} = V_{IN} = 4.5 V to 37 V, V_{BST} = V_{SW} + (V_{DRV} – 0.5 V), C_{BST} = 0.1 μF, C_{DRV} = 1 μF. Min/Max values are valid for the temperature range −40°C < T_J < 150°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
RESET						
Reset output low level	I_{RSTB} = 1 mA	V_{RESL}	–	–	0.4	V
Reset threshold 2 (as a function of VOUT)	VOUT increasing VOUT decreasing	K_{OVRIS} K_{OVFAL}	105 104			

Table 4. ELECTRICAL CHARACTERISTICS
(V_{EN} = V_{BAT} = V_{IN} = 4.5 V to 37 V, V_{BST} = V_{SW} + (V_{DRV} – 0.5 V), C_{BST} = 0.1 μF, C_{DRV} = 1 μF. Min/Max values are valid for the temperature range −40°C < T_J < 150°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
SOFT−START CURRENT						
Soft−start delay	From EN = 1 until start of charging of soft−start capacitor (DBIAS external capacitor = 0.1 μF)	t_{SSDLY}	−	240	−	μs
PEAK CURRENT LIMITS						
Positive current limit threshold voltage	0 ≤ (CSP – CSN) ≤ 200 mV 1.2 V ≤ CSN ≤ 10.0 V, VIN < VIN_HIGH	$V_{PCL,N}$	45	50	55	mV
	0 ≤ (CSP – CSN) ≤ 200 mV 1.2 V ≤ CSN ≤ 10.0 V, VIN > V_{INH} (Guaranteed by design)	$V_{PCL,H}$	48	53.3	58.7	mV
Current limit response time	Comparator tripped until GH falling edge, (V_{CSP} – V_{CSN}) = $V_{CL(typ)}$ + 5 mV	t_{CL}	−	39	125	ns
Negative current limit threshold voltage	−200 mV ≤ (CSP – CSN) ≤ 0 1.2 V ≤ CSN ≤ 10.0 V	V_{NCL}	−20.5	−35.0	−52.0	mV
Common−mode range			−	VOUT	−	V
CSP input bias source current			−	0.1	1.0	μA
CSN input bias source current		$I_{BIAS,CSN}$	−	30	−	μA
GATE DRIVERS						
GH sourcing ON resistance	V_{BST} – V_{GH} = 2 V	$R_{GHSOURCE}$	1.6	2.5	5.3	Ω
GH sinking ON resistance	V_{GH} – V_{SW} = 2 V	R_{GHSINK}	1.3	2.5	4.3	Ω
GH−VSW resistance						

Table 5. FUNCTIONALITY INFORMATION TABLE

VIN (V)	SYNCI Pin	Behavior	Frequency	SYNCI Function	SYNCO	Spread Spectrum	ROSC
VIN < Vin_low	Logic−0	Synchronous mode, recirculation FET turns−off when −35 mV current sense voltage is detected. Pulse skip not allowed when VIN < Vin_low.	410 kHz* or less. Minimum off−time may be skipped depending on VIN, output voltage option and operating current.	Disabled	Enabled, 410 kHz	Disabled	Disabled
	Logic−1						
	F_{sync}		F_{sync} if minimum off−time is not skipped	Enabled	F_{sync}		
Vin_low < VIN < Vin_high (No Pulse Skip Condition)	Logic−0	Synchronous mode, recirculation FET turns−off when when < 0 V current sense voltage is detected.	f_{ROSC} with spread spectrum. Upon exiting Pulse Skip mode, first 1−3 pulses 103 kHz followed by 410 kHz pulses.	Disabled	Enabled, follows spread spectrum	Enabled (When exiting Pulse Skip mode, function resumes within 14 410 kHz pulses)	Enabled (Disabled during 1−3 103 kHz pulses upon exiting Pulse Skip mode)
	Logic−1	Forced PWM mode, recirculation FET turns−off when −35 mV current sense voltage is detected.	f_{ROSC} with spread spectrum	Disabled	Enabled	Enabled	Enabled
	F_{sync}		F_{sync}	Enabled	F_{sync}	Disabled	Disabled
Vin_low < VIN < Vin_high (Pulse Skip Condition)	Logic−0	Pulse skip mode	Disabled	Disabled	Disabled	Disabled	Disabled
VIN > Vin_high	X	Synchronous mode, recirculation FET turns−off when −35 mV current sense voltage is detected. Pulse skip not allowed when VIN > Vin_high.	410 kHz	Disabled	Enabled, 410 kHz	Disabled	Disabled
Soft−start	X	Forced PWM mode with pulse skip allowed, recirculation FET turns−off when when < 0 V current sense voltage is detected.	410 kHz	Disabled	Disabled	Disabled	Disabled
Vout undervoltage (K_{UV})	X	RSTB activated	410 kHz	No change in behavior	No change in behavior	Disabled	No change in behavior
Vout overvoltage (K_{OV})	X	RSB activated	No PWM	No PWM	No Change in behavior	No PWM	No PWM

*GH off pulses will be skipped to maintain output voltage regulation whenever GH t_{off} is less than $t_{off,MIN}$ occurs.

THERMAL CHARACTERISTICS

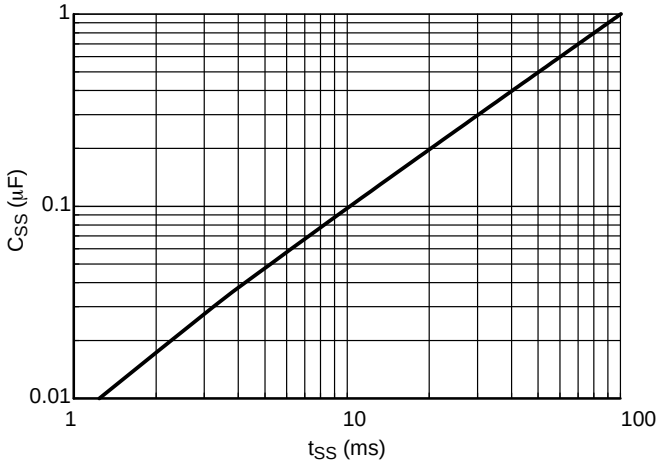


Figure 4. Soft−Start Time vs Capacitance

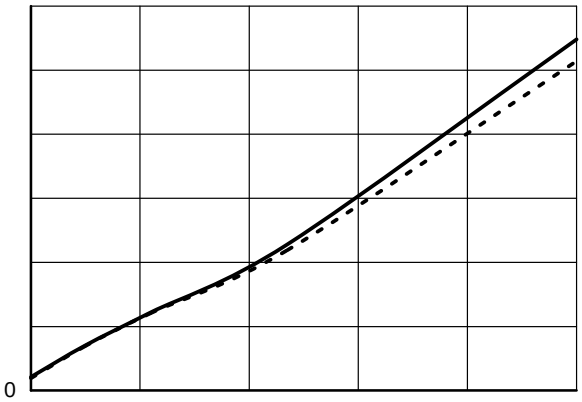


Figure 5. Driver Rise Time vs Load Capacitance

THERMAL CHARACTERISTICS

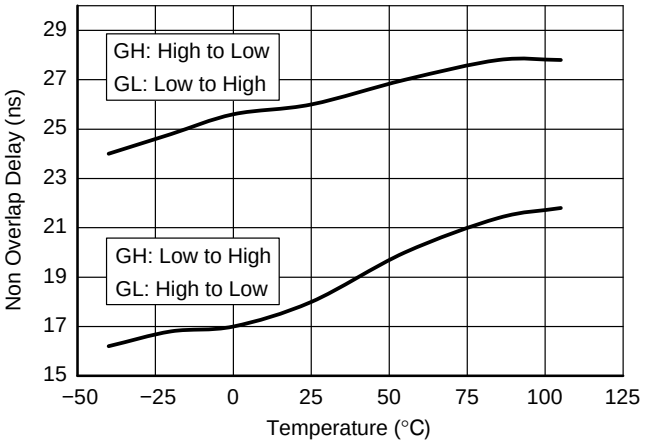


Figure 12. Non−Overlap Delay vs Temperature

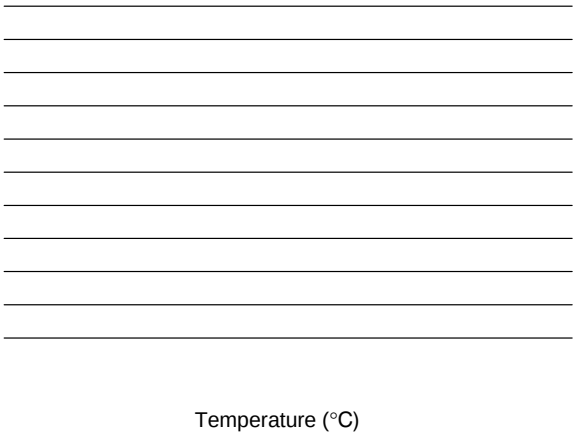


Figure 13. UVLO vs Junction Temperature

DETAILED OPERATING DESCRIPTION

General

Preset internal slope and feedback loop compensation results in predetermined values for current sense resistors and output filtering.

A capacitor technology mix of ceramic and aluminum polymer or solid aluminum electrolytic capacitors results in a cost effective solution. Non−solid aluminum electrolytic capacitors are not recommended due to their large cold temperature ESR properties. An all ceramic solution filter implementation using 22 μF capacitor (like the

- VIN < VIN_low threshold
- VIN > frequency foldback threshold voltage

VCCEXT

VIN supplies VDRV and logic power via the IC's internal LDO. VCCEXT pin is ignored if connected to a voltage less than 5 V or is left unconnected. For improved efficiency, an external 5 V source may be connected to VCCEXT to permit bypassing of the internal LDO (Table 7). The LDO bypass efficiency improvement is reduced at lower currents when the IC enters pulse−skip mode. An IC power consumption reduction of about 100 mW has been measured on a demo board configured with NVMFS5C460NL power transistors at an input voltage of 13 V.

Table 7. NCV881930MW00R2G/AR2G 5 V DEMO BOARD TYPICAL IC POWER CONSUMPTION IMPROVEMENT

VCCEXT = VOUT vs VCCCEXT = OPEN, I_{OUT} > 1 A							
VIN (V)	6	8	10	12	14	16	18
mW	8.7	33.7	58.6	83.3	108	131	156

When the NCV881930MW00R2G/AR2G is configured for a 5 V output (VSEL connected to DBIAS) and VCCEXT is connected to the power supply's output, VFB and CSN traces must be independent from the VCCEXT power trace. VDRV circuitry gate drive current pulses circulate through the VCCEXT PCB trace. Voltage disturbance from the trace parasitic layout inductance will distort CSN and IC−VOUT measurements.

The IC structure has a 2 series anode−

Peak Current Mode Control

The NCV881930 incorporates a current mode control scheme, in which the PWM ramp signal is derived from the power switch current. This ramp signal is compared to the output of the error amplifier to control the on−time of the power switch. The oscillator is used as the frequency clock to ensure a PWM switching operation. The resulting control scheme features several advantages over conventional voltage mode control. First, derived directly from the inductor, the ramp signal responds immediately to line voltage transients. This eliminates the delay caused by the output filter and the error amplifier, which is commonly found in voltage mode controllers. The second benefit comes from inherent pulse−by−pulse current limiting by merely clamping the peak switching current. Finally, since current mode commands an output current rather than voltage, the filter offers only a single pole to the feedback loop. This permits simpler internal compensation.

A fixed slope compensation signal is generated internally and added to the sensed current to avoid increased output voltage ripple due to bifurcation of inductor ripple current at duty cycles above 50%. The fixed amplitude of the slope compensation signal requires the inductor to be less than a maximum value, depending on output voltage, in order to avoid sub−harmonic oscillations. Recommended inductor values are described in Table 6. Other values may be possible.

Current Sensing (CSP−CSN):

V_CS is derived from VIN. It is a supply input for the internal current sense amplifier and should never be used to power external circuitry. The V_CS ceramic decoupling capacitor a minimum of 50 V voltage rating. Ground this pin if not used.

Kelvin connections to current sense resistor (RSNS) are required. CSP−CSN feedback nodes must not be in−line with the power path. An example of a good design practice is to connect the sense lines at the center of the inside edge of the sense resistors (Figure 22).

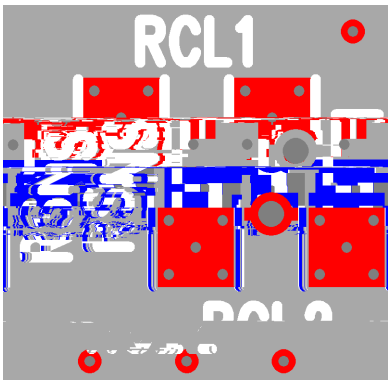


Figure 22. Kelvin Sense Location for Parallel Current Sense Resistors

As a result of the IC's CSP−CSN high input impedance, noise reduction measures should be used for effective noise immunity from the current sense feedback traces.

- Current sense resistors have a small inherent parasitic inductance that will result in a small voltage excursion equaling $L_{RSNS} \bullet \delta I_L/\delta t$ distortion superimposed on the triangular current sense waveform. The differential noise resulting from such a distortion can be minimized with the use of parallel sense resistors. The amplitude of such a distortion is difficult to predict (data not normally provided in resistor datasheets), validation of current limit response during power supply bench evaluation is required.
- Trace routing must not be adjacent to a switch node or other high noise trace.
- Traces should be coincident with of each other on inner layers to minimize coupling from external radiated fields. Traces should be shielded by a top or bottom ground layer (use both layers when possible).
- On layers having the feedback traces, there should be a ground poor next on each side of the traces for additional shielding.
- It is recommended that an output filter ceramic capacitor be located near RSNS/RSNS1 to help mitigate output switching noise at RSF2.
- An optional R−C−R π−filter on the IC's CSP/CSN pins (Figure 23) is sometimes used to filter differential and common mode noise.
- To avoid creating a common−mode noise filter imbalance at the IC current sense pins, simple RC differential filters are not recommended.
- The π−filter must be adjacent to the IC to minimize field induced noise sensitivity on the high impedance side (IC side) of the filter.
- If used, a π−filter −3 dB roll−off frequency > 1 MHz is recommended to prevent the filter transfer function zero from influencing the feedback loop response. RSF1 = RSF2 = 49.9 Ω and CSF1 =100 pF is a recommended starting point.

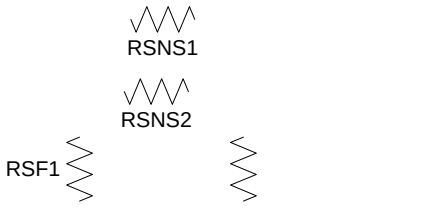
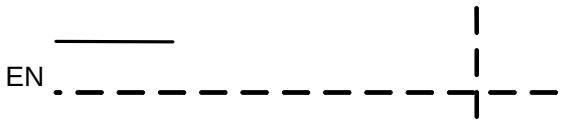


Figure 23. Current Sense Resistor π −Filter

soft−start activity on pin SSC. There is an approximately 15 μs delay between the EN command entering a logic−low state and cessation of PWM activity.



efficiency, which minimizes power dissipation, by minimizing the body diode conduction time, while protecting against cross−conduction (shoot−through) of the MOSFETs. A block diagram of the non−overlap and gate drive circuitry used in the chip and related external components are shown in Figure 29.

The GL driver is enabled when VSW is less than the non−overlap detection comparator threshold of 0.4 V. The GL driver response time is dependent on the comparator differential voltage that develops below the 0.4 V detection threshold; approximately 25 ns response time may be expected when operating in continuous conduction mode.

To maintain output voltage regulation when SYNCI = 0 V (or open) and VINLx < VIN < VIN_HIGH, GH on−time may be as low as 0 ns during non−pulse skipping mode operation. MOSFET response will depend on its Q_g(tot) characteristics.

If the SW pin voltage is still greater than 0.4 V 70 ns following the rising edge of the SYNCI pulse, the IC logic will send a GL pulse to force a recharge of the bootstrap capacitor. The GL pulse width will be no greater than the SYNCI pulse width minus 70 ns. The GL pulse width must be of sufficient duration to fully turn−on the low side MOSFET. The time duration required to turn−on the low side MOSFET will be dependent on the MOSFET's gate charge specification.

The GH driver is enabled when GL voltage is less than the non−overlap detection comparator threshold of 2 V. The GH driver response time is dependent on the comparator differential voltage that develops below the 0.4 V detection threshold; response time is approximately 40 ns.

- When VCOMP reaches a predetermined lower voltage threshold, the IC control logic enters pulsed−skip mode to maintain regulation. Some output voltage ripple associated with the pulse skipping is to be expected.
- Low−I_Q operating mode is entered during pulse−skipping event, permitting higher efficiency operation under low output power operation. The duration is dependent on operating conditions. When the controller exits pulse−skip mode, normal PWM regulation is preceded by up to three ~103 kHz pulses (410 kHz/4) as internal logic comes out of low−I_Q mode.
- As the OTA VCOMP is used for feedback control, the VCOMP will not remain constant, increasing to resume PWM activity.

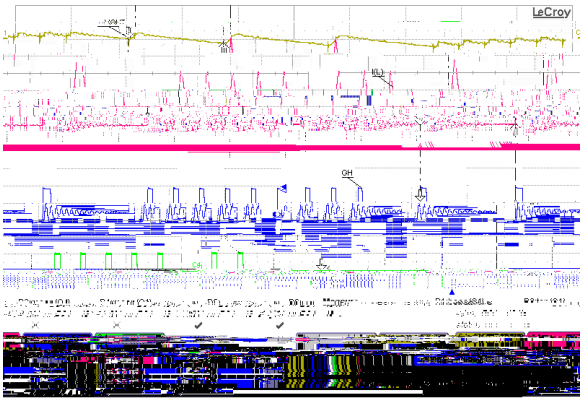


Figure 31. IC Pulse−Skip PWM Behavior, Borderline Pulse−Skip Region

Ch 1: Power supply output voltage (50 mV/div)

Ch 2: Output inductor current (0.5 A/div)

Ch 3: IC gate high (GH) (10 V/div)

Ch 4: IC gate low (GL) (5 V/div)

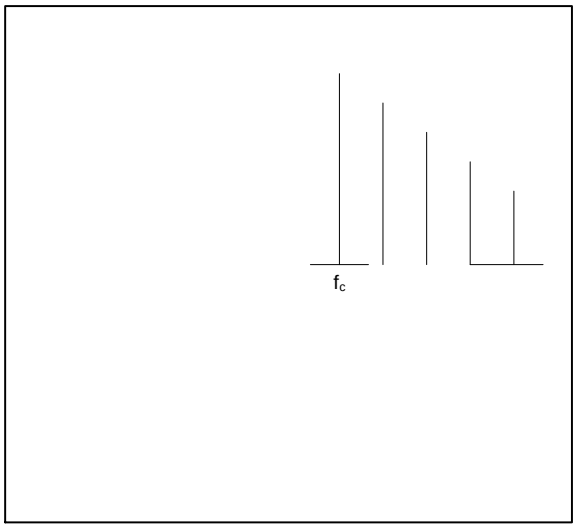
The thermal shutdown protection circuitry is activated at $T_J \approx 85°C$ and remains active during pulse−skipping, consuming additional quiescent current.

Feedback Loop Measurement

The compensation network and voltage feedback OTA are internal to the IC. Monitoring points permitting

Spread Spectrum

In SMPS devices, switching translates to higher efficiency. As a consequence, the switching also leads to a higher EMI profile. We can greatly reduce some of the peak radiated emissions with some spread spectrum techniques. Spread spectrum is a method used to reduce the peak electromagnetic emissions of a switching regulator.



APPLICATIONS INFORMATION

Design Methodology

Choosing external components encompasses the following design process:

1. Operational parameter definition
2. Switching frequency selection (ROSC)
3. Output inductor selection
4. Current sense resistor selection
5. Output capacitor selection
6. Input capacitor selection
7. Thermal considerations

(1) Operational Parameter Definition

Before proceeding with the rest of the design, certain operational parameters must be defined. These are application dependent and include the following:

V_{IN}: input voltage, range from minimum to maximum with a typical value [V]

V_{OUT}: output voltage [V]

I_{OUT}: output current, range from minimum to maximum with initial start−up value [A]

I_{CL}: desired typical current limit [A]

A ripple current δI_L equaling 20−40% of the output rated current is a typical objective when selecting an inductor value for a duty ratio D normally selected at the nominal input operating voltage. The inductor value may be calculated using the following expression:

$$L = \frac{V_{OUT} \cdot (1 - D)}{\delta I_L \cdot f_S} \quad \text{(eq. 13)}$$

Inductor saturation current is specified by inductor manufacturers as the current at which the inductance value has dropped a certain percentage from the nominal value, typically 10−30%. It is recommended to choose an inductor with saturation current sufficiently higher than the peak output current, such that the inductance is very close to the nominal value at the peak output current. This introduces a safety factor and allows for more optimized compensation.

Inductor efficiency is another consideration when selecting an output inductor. Inductor losses include DC and AC winding losses as well as core losses. Core losses are proportional to the amplitude of the ripple current and operating frequency.

AC winding losses are based on the AC resistance of the

Capacitors should also be chosen to provide acceptable output voltage ripple with a DC load, in addition to limiting voltage overshoot during a dynamic response. Key specifications are equivalent series resistance (ESR) and equivalent series inductance (ESL). The output capacitors must have very low ESL for best transient response. The PCB traces will add to the ESL, but by positioning the output capacitors close to the load, this effect can be minimized and ESL neglected when determining output voltage ripple.

The total peak−to−peak ripple δV_{OUT} is defined as:

$$\delta V_{OUT} = \delta I_L \cdot \left(\frac{1}{8 \cdot C \cdot f_{SW}} + r_{ESR} \right) \quad \text{(eq. 20)}$$

Where: δV_{OUT}: total output voltage ripple due to output capacitance and its ESR [V_{pp}]
r_{ESR}: output capacitor ESR [Ω]

Capacitor ESR corresponding to the operating frequency f_s must be used. The steady−state power lost from the capacitor ESR may be calculated as follows:

$$P_{C(ESR)} = \frac{1}{3} \cdot \delta I_L{}^2 \cdot r_{ESR} \quad \text{(eq. 21)}$$

(6) Input Capacitor Selection

The input EMI capacitors must sustain the ripple current produced during the on time of the high−side MOSFET and must have a low ESR to minimize the losses. The RMS value of this ripple is:

$$I_{IN(RMS)} = I_{OUT} \cdot \sqrt{D \cdot (1 - D)} \quad \text{(eq. 22)}$$

where: $I_{IN(RMS)}$ = input RMS current [A]

The peak harmonic current will be at the switching frequency. The above equation reaches its maximum value with D = 0.5, $I_{IN(RMS)} = I_{OUT}/2$. The input capacitors must be rated to handle the RMS ripple current.

Input capacitor RMS current losses may be calculated with the following equation:

$$P_{CIN} = I_{IN(RMS)}{}^2 \cdot R_{ESR(CIN)} \quad \text{(eq. 23)}$$

where: P_{CIN} = power loss from the input capacitors
$R_{ESR(CIN)}$ = effective series resistance of the input capacitance

Due to large current transients through the input capacitors, electrolytic, polymer or ceramics should be used. ripple curren,s i(iscommion toplache)]TJT* 1 Tf1-.0697 Tw[cerami)67.3(ca

Table 10. ORDERING INFORMATION

Device	Output Voltage	Marking	Package	Shipping†
NCV881930MW00AR2G	3.3 V/5.0 V	8819A 3000	QFN24 (Pb−Free)	4000 / Tape & Reel

DISCONTINUED (Note 9)

NCV881930MW00R2G	3.3 V/5.0 V	V8819 3000	QFN24 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NOTE: The NCV881930 will not offer the alternate construction leadframe version illustrated in Detail A and Detail B in the Package Dimensions.

9. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.