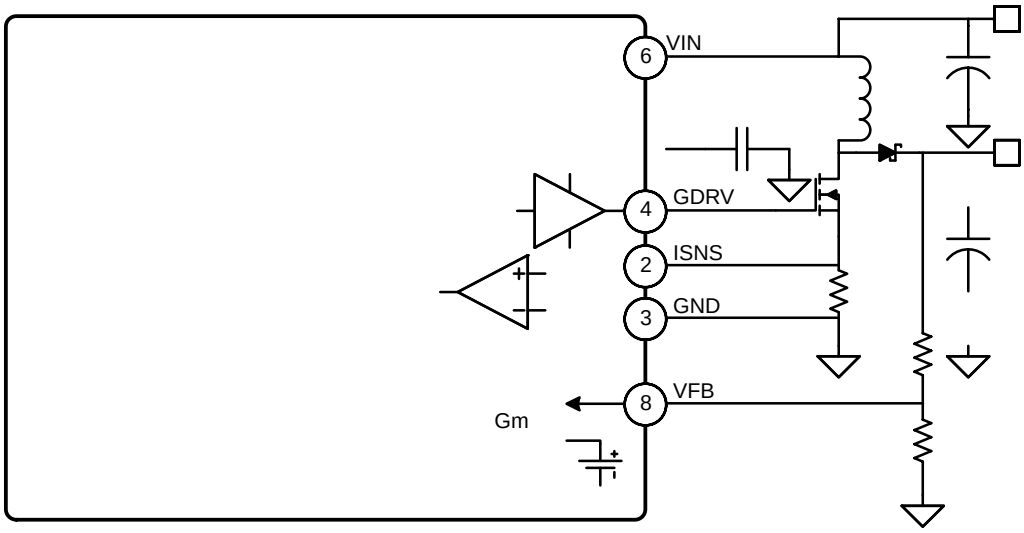

6
VIN
4
GDRV
2
ISNS
3
GND
8
VFB
Gm

ABSOLUTE MAXIMUM RATINGS (Voltages are with respect to GND, unless otherwise indicated)

Rating	Value	Unit
Dc Supply Voltage (VIN)	−0.3 to 40	V
Peak Transient Voltage (Load Dump on VIN)	45	V
Dc Supply Voltage (VDRV, GDRV)	12	V
Peak Transient Voltage (VFB)	−0.3 to 6	V
Dc Voltage (VC, VFB, ISNS)	−0.3 to 3.6	V
Dc Voltage (EN/SYNC)	−0.3 to 6	V
Dc Voltage Stress (VIN − VDRV)*	−0.7 to 45	V
Operating Junction Temperature	−40 to 150	°C
Storage Temperature Range	−65 to 150	°C
Peak Reflow Soldering Temperature: Pb−Free, 60 to 150 seconds at 217°C	265 peak	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*An external diode from the input to the VIN pin is required if bootstrapping VDRV and VIN off of the output voltage.

PACKAGE CAPABILITIES

Characteristic		Value	Unit
ESD Capability (All Pins)	Human Body Model Machine Model	≥ 2.0 ≥ 200	kV V
Moisture Sensitivity Level		1	−
Package Thermal Resistance	Junction−to−Ambient, $R_{\theta JA}$ (Note 1)	100	°C/W

1. 1 in^2, 1 oz copper area used for heatsinking.

Device Variations

The NCV8871 features several variants to better fit a multitude of applications. The table below shows the typical values of parameters for the parts that are currently available.

TYPICAL VALUES

Part No.	D_{max}	f_s	t_{ss}	S_a	V_{cl}	I_{src}	I_{sink}	V_{DRV}	SCE
NCV887100	88%	170 kHz	7.4 ms	53 mV/ s	400 mV	800 mA	600 mA	10.5 V	Y
NCV887103	93%	340 kHz	3.7 ms	53 mV/ s	200 mV	575 mA	350 mA	8.4 V	Y
NCV887104	93%	340 kHz	3.7 ms	53 mV/ s	200 mV	800 mA	600 mA	8.4 V	N
NCV887105	88%	170 kHz	7.4 ms	53 mV/ s	400 mV	800 mA	600 mA	10.5 V	N

DEFINITIONS

Symbol	Characteristic	Symbol	Characteristic	Symbol	Characteristic
D_{max}					

ELECTRICAL CHARACTERISTICS ($-40°C < T_J < 150°C$, $3.2\ V < V_{IN}$

ELECTRICAL CHARACTERISTICS (−40°C < T_J < 150°C, 3.2 V < V_{IN}

ELECTRICAL CHARACTERISTICS (−40°C < T_J < 150°C, 3.2 V < V_{IN} < 40 V, unless otherwise specified) Min/Max values are guaranteed by test, design or statistical correlation.

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Symbol						

TYPICAL PERFORMANCE CHARACTERISTICS

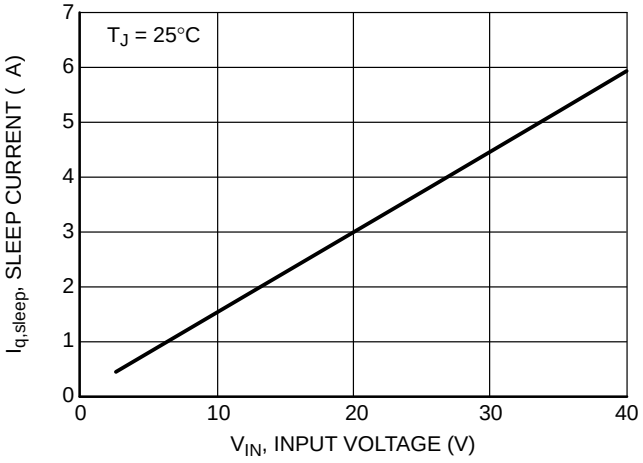


Figure 2. Sleep Current vs. Input Voltage

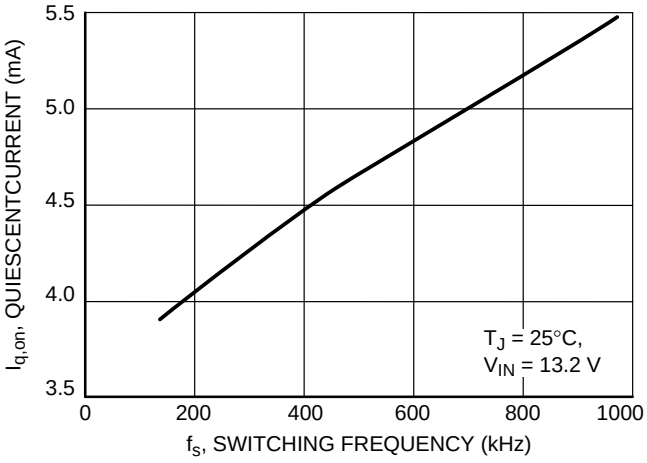


Figure 3. Quiescent Current vs. Switching Frequency

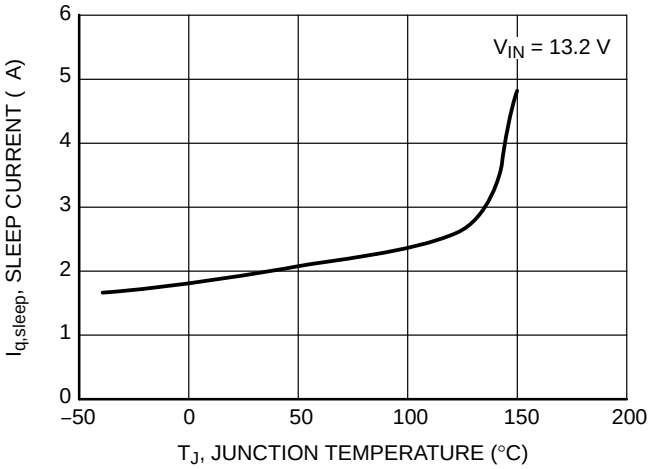


Figure 4. Sleep Current vs. Temperature

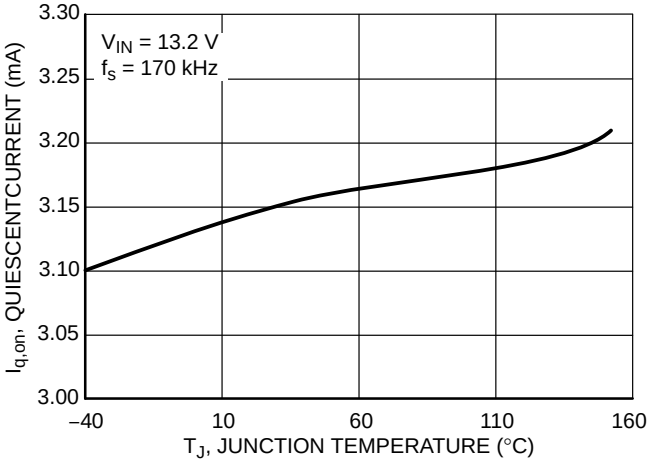


Figure 5. Quiescent Current vs. Temperature

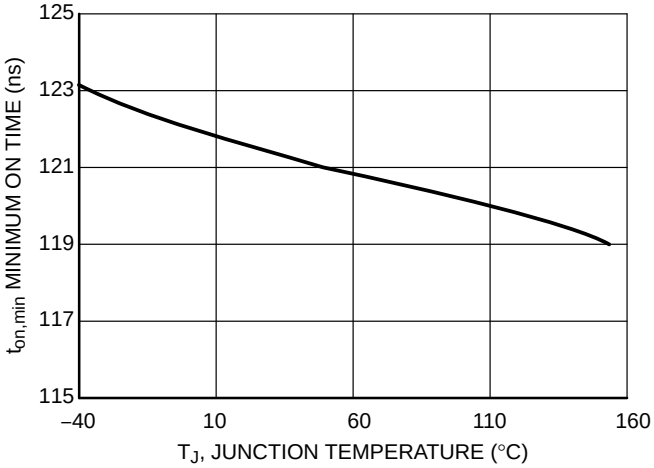


Figure 6. Minimum On Time vs. Temperature

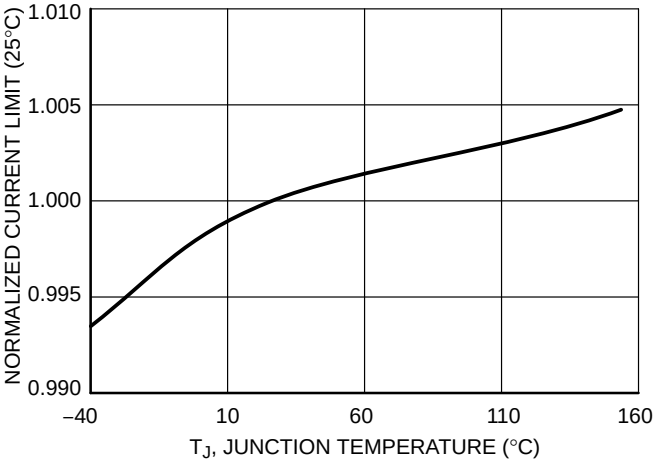


Figure 7. Normalized Current Limit vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

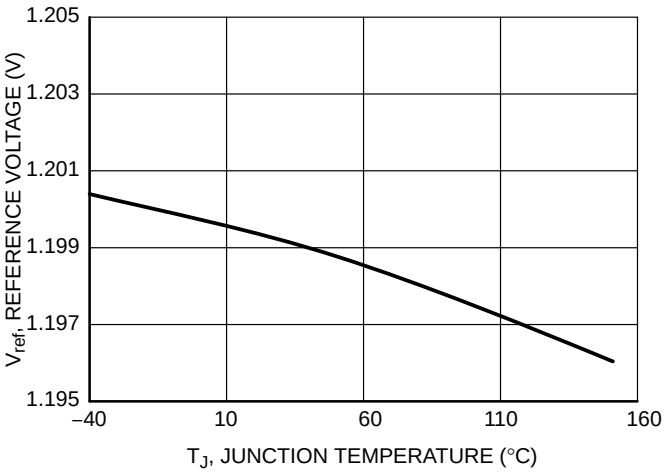


Figure 8. Reference Voltage vs. Temperature

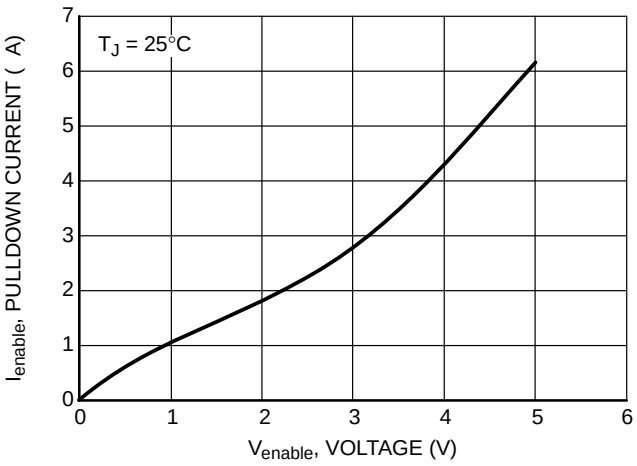


Figure 9. Enable Pulldown Current vs. Voltage

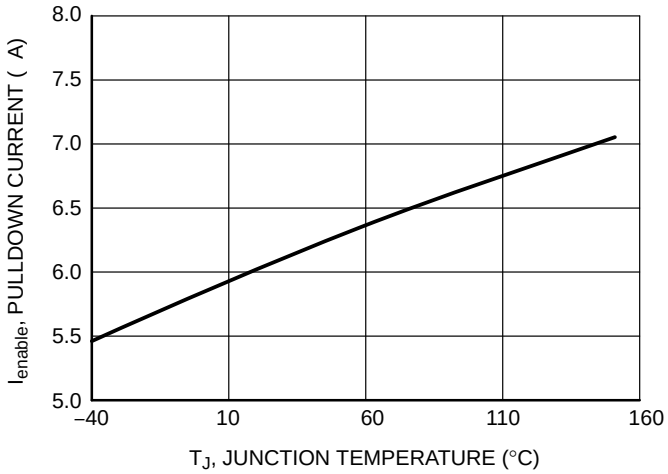


Figure 10. Enable Pulldown Current vs. Temperature

THEORY OF OPERATION

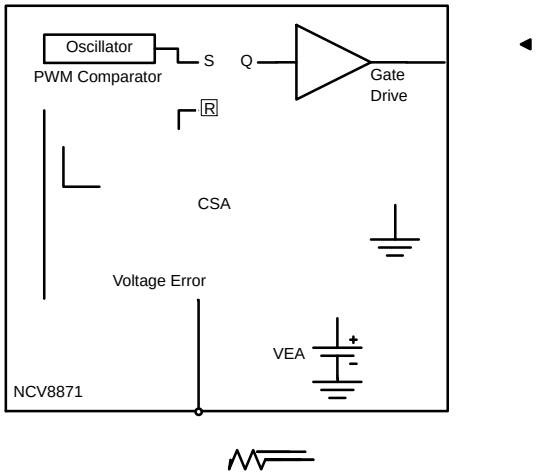


Figure 11. Current Mode Control Schematic

held low during VIN ramp, the internal voltage rails and the POR circuit will decay down to 0 V. If EN/SYNC asserts high before decay of the POR circuit, the logic could become stuck in an invalid state (no switching). To avoid the possibility for such a power up issue, the EN/SYNC signal should be applied a minimum of 500 s after application of voltage on VIN.

If the VIN pin voltage falls below V_{UVLO} when EN/SYNC pin is at logic−high, the IC may not power up when VIN returns back above the UVLO. To resume a normal operating state, the EN/SYNC pin must be cycled with a single logic−low to logic−high transition.

UVLO

Input Undervoltage Lockout (UVLO) is provided to ensure that unexpected behavior does not occur when VIN is too low to support the internal rails and power the controller. The IC will start up when enabled and VIN surpasses the UVLO threshold plus the UVLO hysteresis and will shut down when VIN drops below the UVLO threshold or the part is disabled.

To avoid any lock state under UVLO conditions, the EN/SYNC pin should be in logic−low state. For further details, please refer to EN/SYNC paragraph.

Internal Soft−Start

To insure moderate inrush current and reduce output overshoot, the NCV8871 features a soft start whic gs t

Where: R_S: sense resistor [Ω]
V_{CL}: current limit threshold voltage [V]
I_{CL}: desire current limit [A]

3. Select Output Inductor

The output inductor controls the current ripple that occurs over a switching period. A high current ripple will result in excessive power loss and ripple current requirements. A low current ripple will result in a poor control signal and a slow current slew rate in case of load steps. A good starting point for peak to peak ripple is around 20−40% of the inductor current at the maximum load at the worst case V_{IN}, but operation should be verified empirically. The worst case V_{IN} is half of V_{OUT}, or whatever V_{IN} is closest to half of V_{OUT}. After choosing a peak current ripple value, calculate the inductor value as follows:

$$L = \frac{V_{IN(WC)}\, D_{WC}}{\Delta I_{L,max}\, f_s}$$

Where: $V_{IN(WC)}$: V_{IN} value as close as possible to half of V_{OUT} [V]
D_{WC}: duty cycle at $V_{IN(WC)}$
$\Delta I_{L,max}$: maximum peak to peak ripple [A]

The maximum average inductor current can be calculated as follows:

$$I_{L,AVG} = \frac{V_{OUT} I_{OUT(max)}}{V_{IN(min)} \eta}$$

The Peak Inductor current can be calculated as follows:

$$I_{L,peak} = I_{L,avg} + \frac{\Delta I_{L,max}}{2}$$

Where: $I_{L,peak}$: Peak inductor current value [A]

4. Select Output Capacitors

The output capacitors smooth the output voltage and reduce the overshoot and undershoot associated with line transients. The steady state output ripple associated with the output capacitors can be calculated as follows:

$$V_{OUT(ripple)} = \frac{D I_{OUT(max)}}{f C_{OUT}} + \left(\frac{I_{OUT(max)}}{1 - D} + \frac{V_{IN(min)} D}{2 f L} \right) R_{ESR}$$

The capacitors need to survive an RMS ripple current as follows:

$$I_{Cout(RMS)} = I_{OUT} \sqrt{\frac{D_{WC}}{D'_{WC}} + \frac{D_{WC}}{12} \left(\frac{D'_{WC}}{\frac{L}{R_{OUT} \times T_{SW}}} \right)^2}$$

The use of parallel ceramic bypass capacitors is strongly encouraged to help with the transient response.

5. Select Input Capacitors

The input capacitor reduces voltage ripple on the input to the module associated with the ac component of the input current.

$$I_{Cin(RMS)} = \frac{V_{IN(min)}^2}$$

10. Determine Feedback Loop Compensation Network

The purpose of a compensation network is to stabilize the dynamic response of the converter. By optimizing the compensation network, stable regulation response is achieved for input line and load transients.

Compensator design involves the placement of poles and zeros in the closed loop transfer function. Losses from the boost inductor, MOSFET, current sensing and boost diode losses also influence the gain and compensation expressions. The OTA has an ESD protection structure ($R_{ESD} \approx 502\ \Omega$, data not provided in the datasheet) located on the die between the OTA output and the IC package compensation pin (VC). The information from the OTA PWM feedback control signal (V_{CTRL}) may differ from the IC-VC signal if R_2 is of similar order of magnitude as R_{ESD}. The compensation and gain expressions which follow take influence from the OTA output impedance elements into account.

Type-I compensation is not possible due to the presence of R_{ESD}. The Figures 12 and 13 compensation networks correspond to a Type-II network in series with R_{ESD}. The resulting control-output transfer function is an accurate mathematical model of the IC in a boost converter topology. The model does have limitations and a more accurate SPICE model should be considered for a more detailed analysis:

- The attenuating effect of large value ceramic capacitors

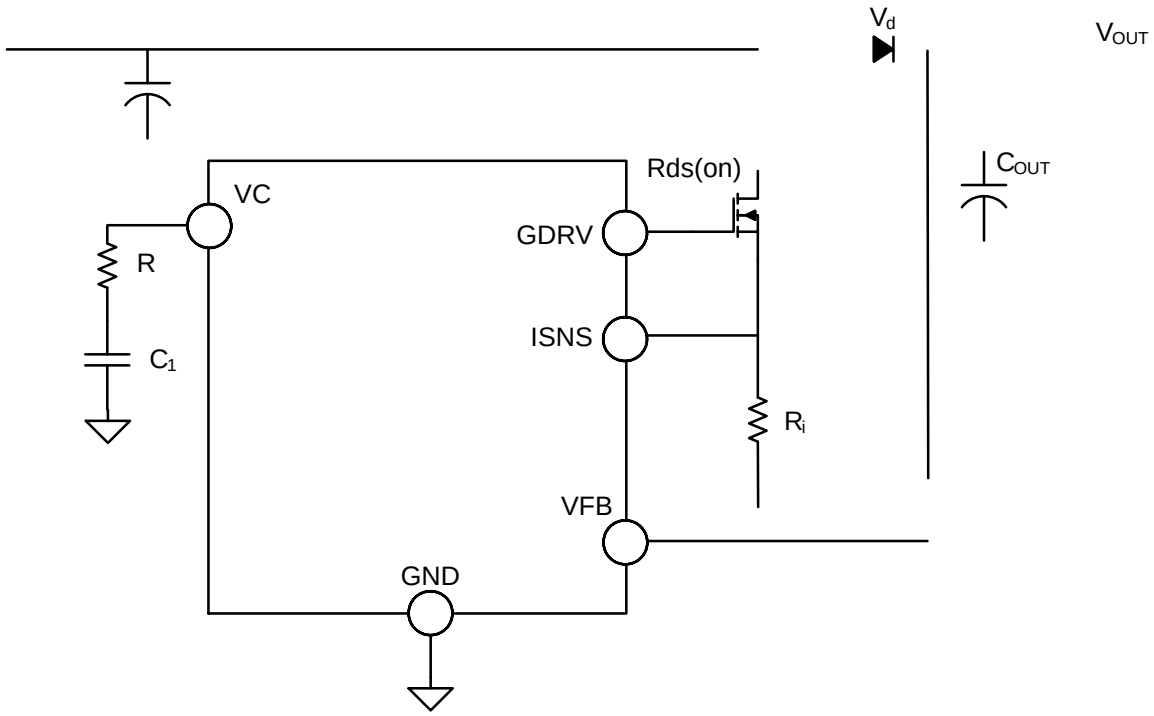

Vd
VOUT
COUT
Rds(on)
VC
GDRV
R
ISNS
C1
Ri
VFB
GND

Table 2. FLYBACK CCM AND DCM TRANSFER FUNCTION EXPRESSIONS

	CCM	DCM
Duty ratio (**D**)		Where:
V_{OUT}/V_{IN} DC Conversion Ratio (**M**)		
Inductor On-slope (***S_n***), V/s		
Compensation Ramp (***m_c***)		
C_{out} ESR Zero (***ω_{z1}***)		
Right-Half-Plane Zero (***ω_{z2}***)		
Modulator Pole (***ω_{p1}***)		
ω_{p2}		
F_m		
H_d		
Control-output Transfer Function (***H_{ctrl_output}(f)***)		

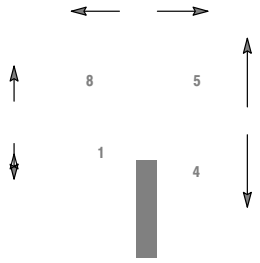
Table 3. OTA COMPENSATION TRANSFER FUNCTION AND COMPENSATION VALUES

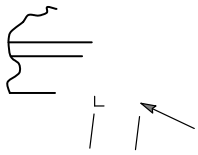
Desired OTA Gain at Cross-over Frequency f_c (***G***)	$10^{\frac{\quad}{0}}$
Desired Phase Boost at Cross-over Frequency f_c (***boost***)	$\left(- \left(\right) \right)^{\frac{1\ 0}{}} - 0 \Big)^{\frac{}{1\ 0}}$
Select OTA Compensation Zero to Coincide with Modulator Pole at f_{p1} (***f_z***)	$\frac{1}{}$
Resulting OTA High Frequency Pole Placement (***f_p***)	$\frac{+ \quad (\quad)}{- \quad (\quad)}$
Compensation Resistor ***R_2***	$\frac{}{1.} \frac{\sqrt{1 + \left(\frac{}{}\right)}}{\sqrt{1 + \left(\frac{}{}\right)}}$
Compensation Capacitor ***C_1***	$\frac{1}{}$
Compensation Capacitor ***C_2***	$\frac{1}{} \cdot \frac{}{+ 1}$
OTA DC Gain (***G_0_OTA***)	$\frac{}{+ 1} \cdot 0$
Low Frequency Zero (ω_{z1e})	$\frac{1}{} \frac{\left(+ \right)}{} \left[1 - \quad 1 - \quad^2 \right.$

2. Select Current Sense Resistor

SOIC 8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011





SEATING
PLANE