

NCV890100

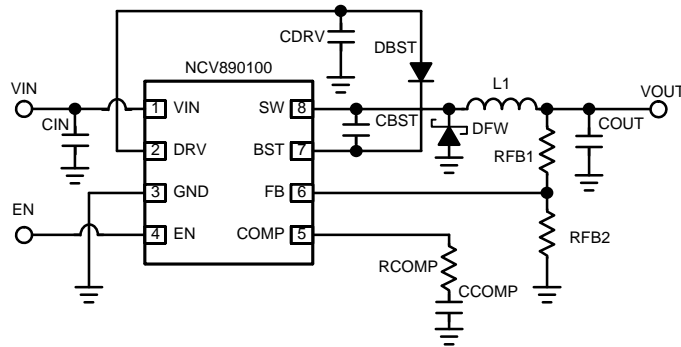


Figure 1. Typical Application

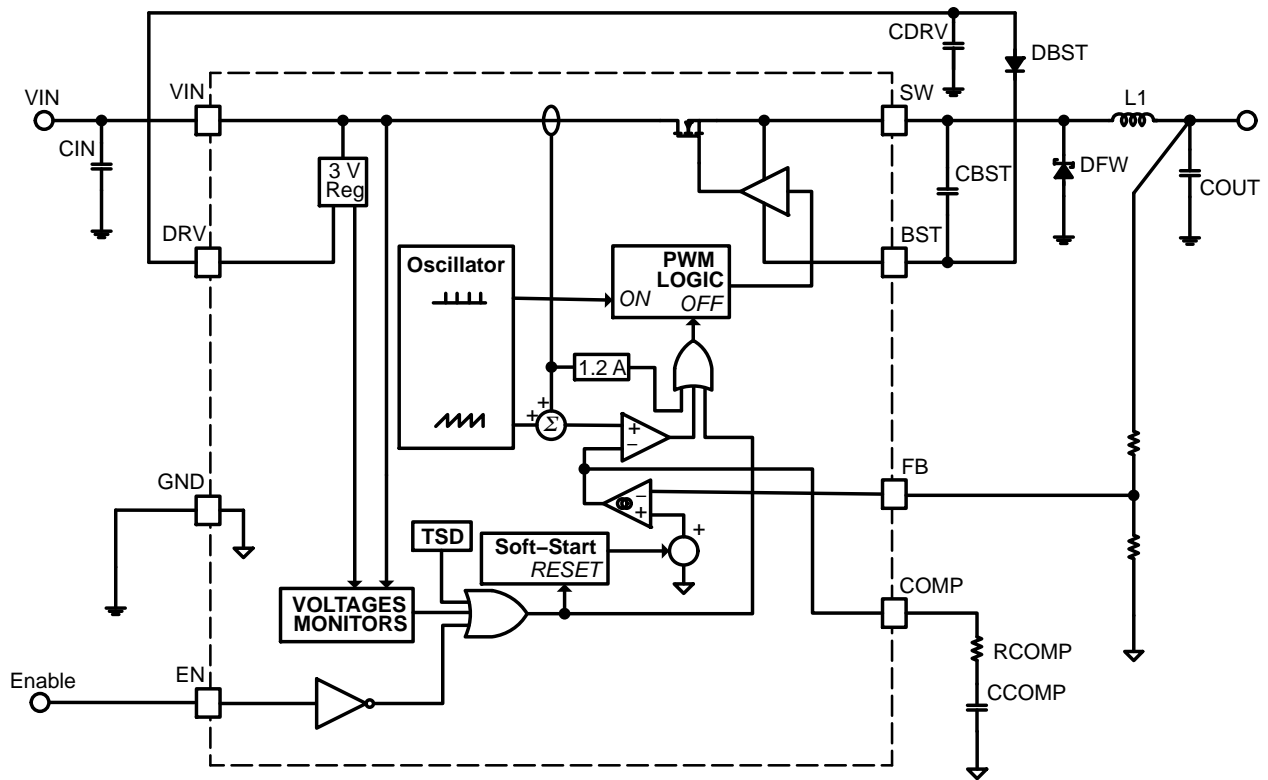


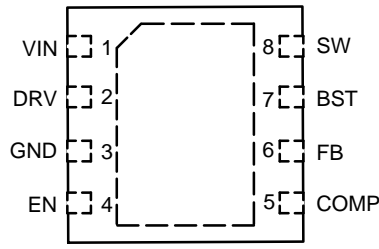
Figure 2. NCV890100 Block Diagram

MAXIMUM RATINGS

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Rating

NCV890100



(Top View)

Figure 3. Pin Connections

PIN FUNCTION DESCRIPTIONS

Pin No.	Symbol	Description
1	VIN	Input voltage from battery. Place an input filter capacitor in close proximity to this pin.
2	DRV	Output voltage to provide a regulated voltage to the Power Switch gate driver.
3	GND	Battery return, and output voltage ground reference.
4	EN	This TTL compatible Enable input allows the direct connection of Battery as the enable signal. Grounding this input stops switching and reduces quiescent current draw to a minimum.
5	COMP	Error Amplifier output, for tailoring transient response with external compensation components.
6	FB	Feedback input pin to program output voltage, and detect pre-charged or shorted output conditions.
7	BST	Bootstrap input provides drive voltage higher than VIN to the N-channel Power Switch for optimum switch $R_{DS(on)}$ and highest efficiency.
8	SW	Switching node of the Regulator. Connect the output inductor and cathode of the freewheeling diode to this pin.
Exposed Pad		Connect to Pin 3 (electrical ground) and to a low thermal resistance path to the ambient temperature environment.

NCV890100

ELECTRICAL CHARACTERISTICS ($V_{IN} = 4.5\text{ V to }28\text{ V}$, $V_{EN} = 5\text{ V}$, V

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ELECTRICAL CHARACTERISTICS ($V_{IN} = 4.5\text{ V to }28\text{ V}$, $V_{EN} = 5\text{ V}$, $V_{BST} = V_{SW} + 3.0\text{ V}$, $C_{DRV} = 0.1\text{ }\mu\text{F}$, Min/Max values are valid for the temperature range $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ unless noted otherwise, and are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
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POWER SWITCH

ON Resistance	R_{DSON}	$V_{BST} = V_{SW} + 3.0\text{ V}$			650	m Ω
Leakage current VIN to SW	I_{LKSW}	$V_{EN} = 0\text{ V}$, $V_{SW} = 0$, $V_{IN} = 18\text{ V}$			10	μA
Minimum ON Time	t_{ONMIN}	Measured at SW pin	45		70	ns
Minimum OFF Time	t_{OFFMIN}	Measured at SW pin At $F_{SW} = 2\text{ MHz}$ (normal) At $F_{SW} = 500\text{ kHz}$ (max duty cycle)	30	30 50	70	ns

PEAK CURRENT LIMIT

Current Limit Threshold	I_{LIM}		1.4	1.55	1.7	A
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SHORT CIRCUIT FREQUENCY FOLDBACK

Lowest Foldback Frequency	F_{SWAF}	$V_{FB} = 0\text{ V}$, $4.5\text{ V} < V_{IN} < 18\text{ V}$	400	500	600	kHz
Lowest Foldback Frequency – High V_{in}	F_{SWAFHV}	$V_{FB} = 0\text{ V}$, $20\text{ V} < V_{IN} < 28\text{ V}$	200	250	300	
Hiccup Mode	F_{SWHIC}	$V_{FB} = 0\text{ V}$	24	32	40	

GATE VOLTAGE SUPPLY (DRV pin)

Output Voltage	V_{DRV}		3.1	3.3	3.5	V
DRV POR Start Threshold	V					

TYPICAL CHARACTERISTICS CURVES

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20 TD0.4cm 0

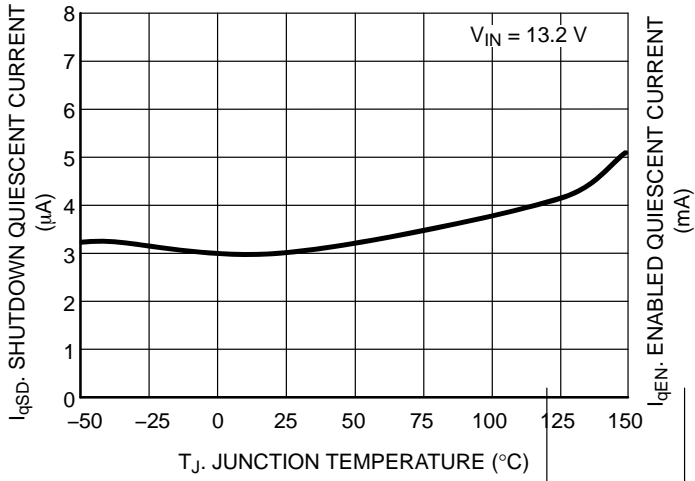


Figure 4. Shutdown Quiescent Current vs. Junction Temperature

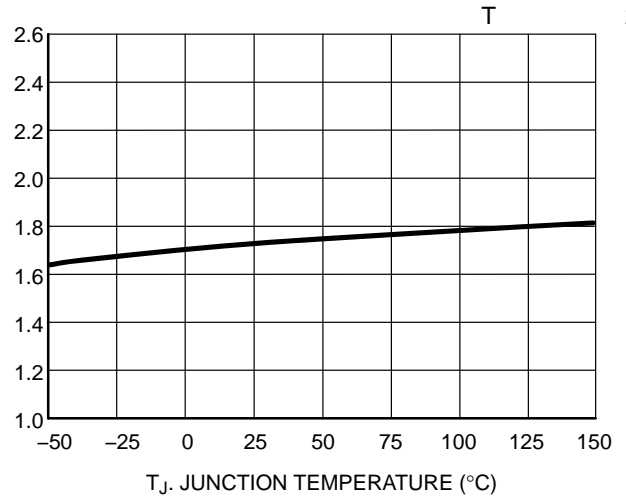


Figure 5. Enabled Quiescent Current vs. Junction Temperature

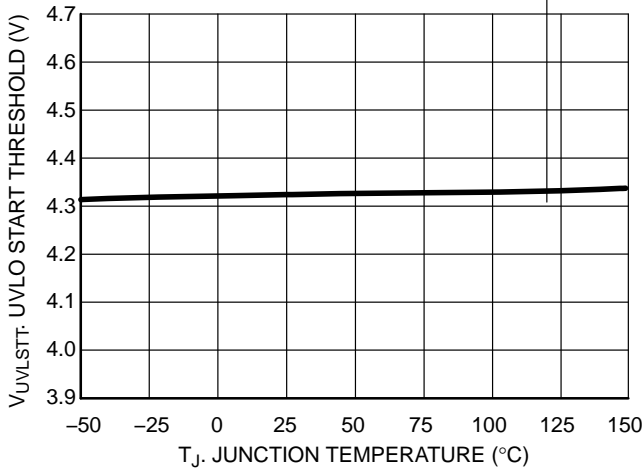
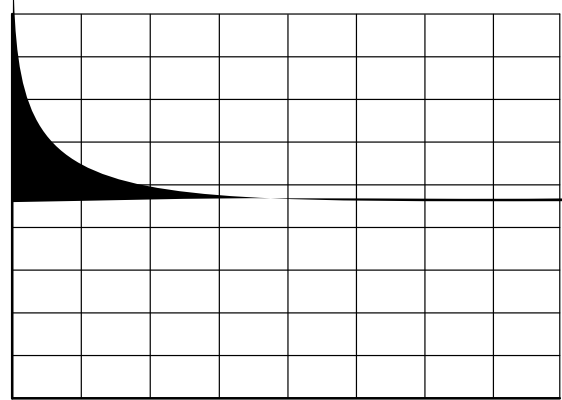


Figure 6. UVLO Start Threshold vs. Junction Temperature



TYPICAL CHARACTERISTICS CURVES

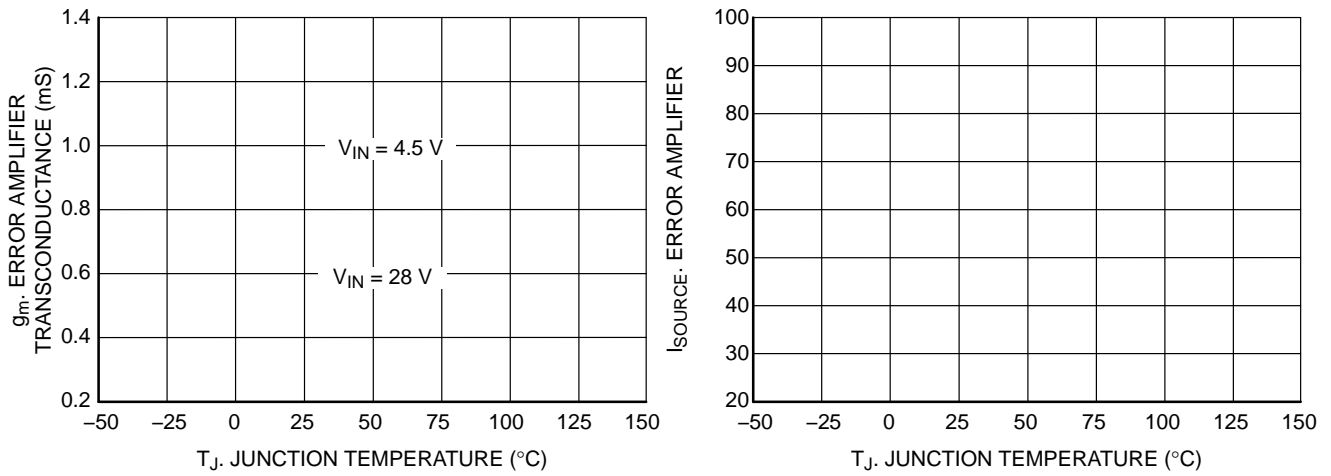


Figure 10. Error Amplifier Transconductance vs. Junction Temperature

TYPICAL CHARACTERISTICS CURVES

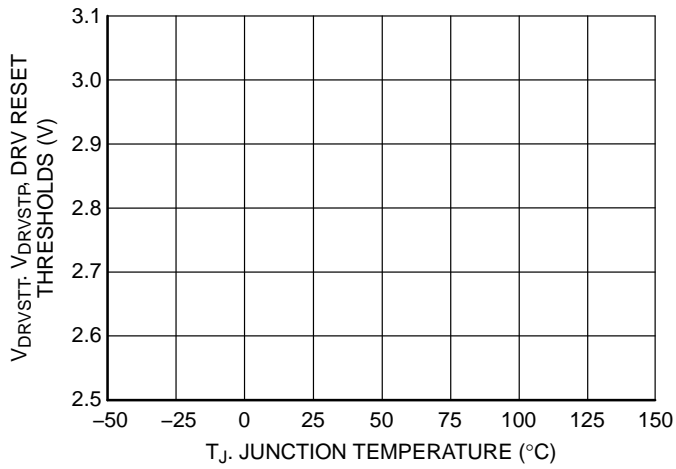


Figure 22. DRV Reset Threshold vs. Junction Temperature

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GENERAL INFORMATION

INPUT VOLTAGE

BOOTSTRAP

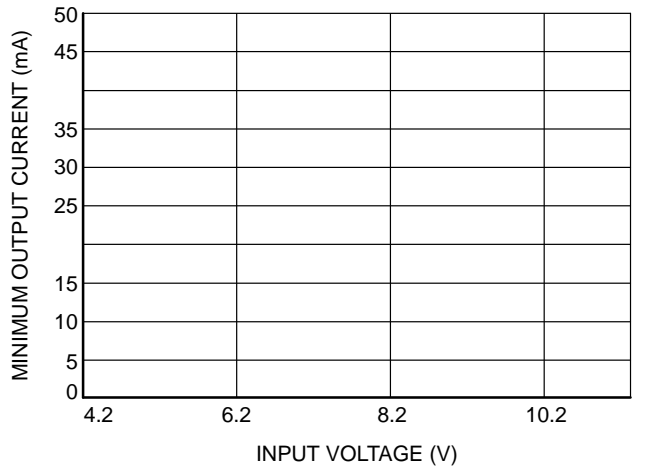
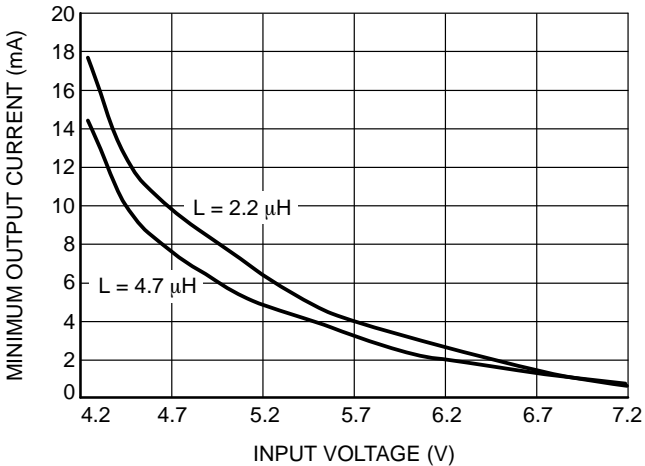
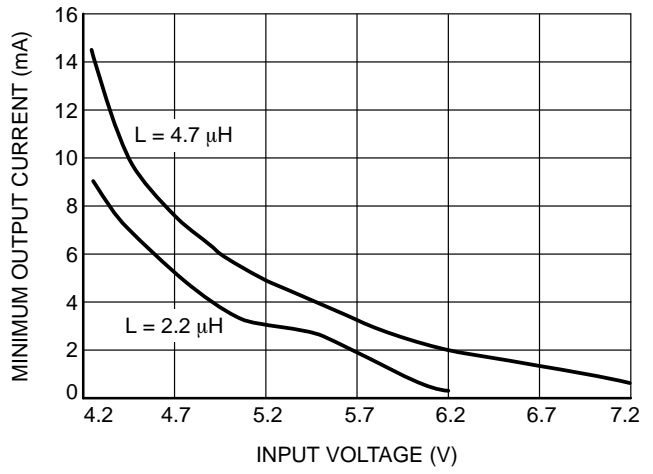
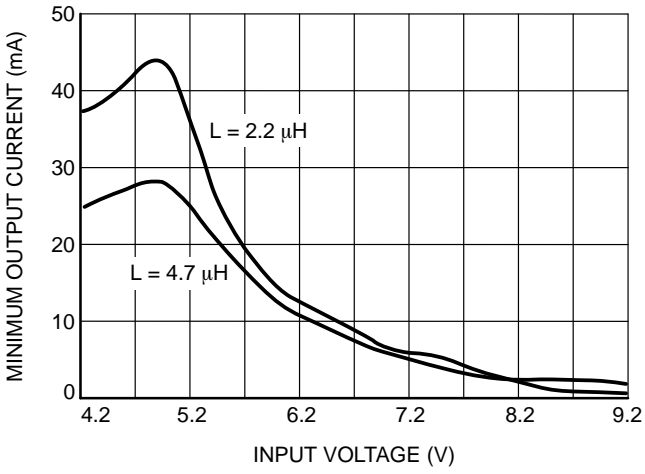


Figure 27. Minimum Load Current with Different Input and Output Voltages

OUTPUT PRECHARGE DETECTION

$$M_c = 1 + \frac{S_e}{S_n} \quad (\text{eq. 16})$$

$$S_n = \frac{V_{in} - V_{out}}{L} \cdot R_i \quad (\text{eq. 17})$$

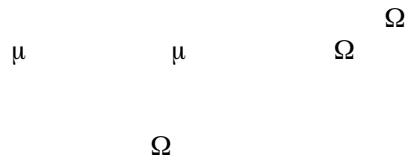
Design of the Compensation Network

Ω

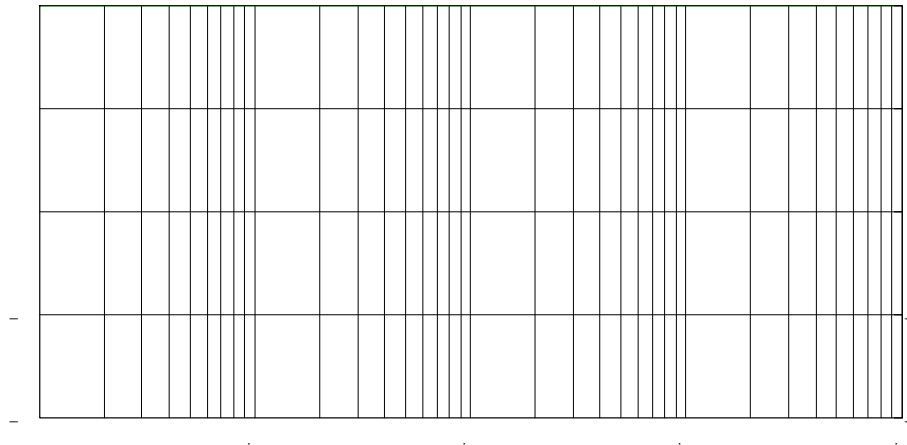
$$F_h(s) = \frac{1}{1 + \frac{s}{\omega_n \cdot Q_p} + \frac{s^2}{\omega_n^2}} \quad (\text{eq. 18})$$

$$\omega_n = \pi \cdot F_{sw}$$

$$Q_p = \frac{1}{\pi \cdot [M_c \cdot (1 - D) - 0.5]} \quad (\text{eq. 19})$$



$$G_{loop}(s) = G_{divider}(s) \cdot G_{err_amp}(s) \cdot G_{ps}(s) \quad (\text{eq. 20})$$



Ω

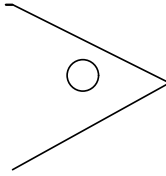
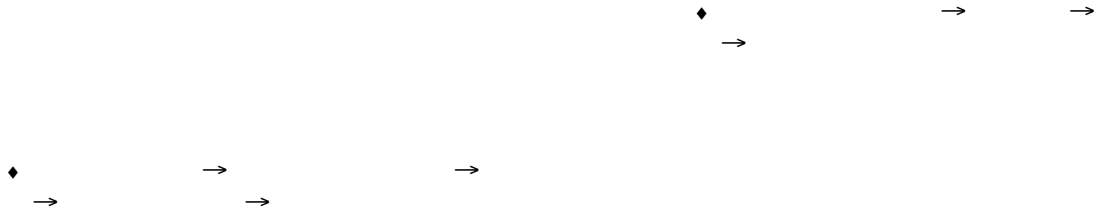


Figure 31. Example of the Feedback Compensation Network

PCB LAYOUT RECOMMENDATION



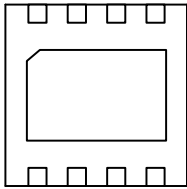
DFN8, 3x3, 0.65P
CASE 506BY
ISSUE A

SCALE 2:1

DATE 23 MAY 2012

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION *b* APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. FOR DEVICE OPN CONTAINING W OPTION,



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