© Semiconductor Components Industries, LLC, 2015

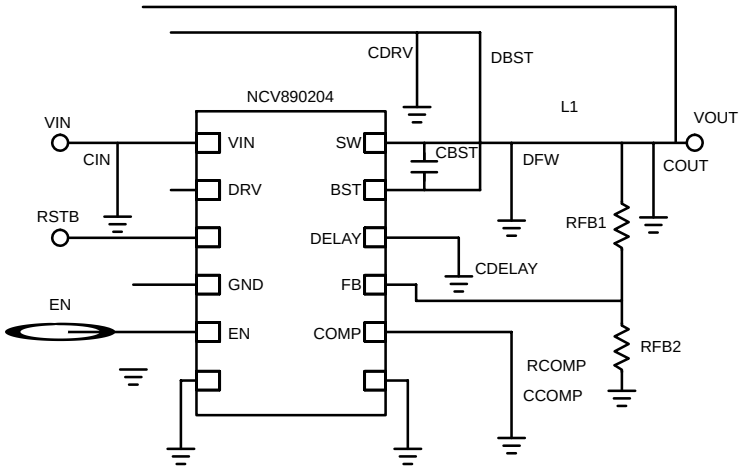


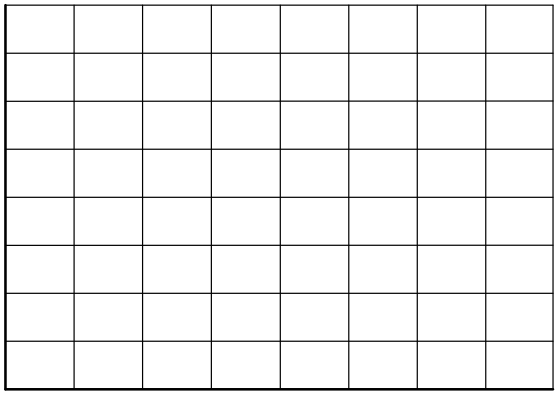
Figure 1. Typical Application

ELECTRICAL CHARACTERISTICS
(V_{IN} = 4.5 V to 28 V, V_{EN} = 5 V, V_{BST} = V_{SW} + 3.0 V, C_{DRV} = 0.1 μ

ELECTRICAL CHARACTERISTICS (continued)
(V_{IN} = 4.5 V to 28 V, V_{EN} = 5 V, V_{BST} = V_{SW} + 3.0 V, C_{DRV} = 0.1 μF, Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DELAY						
Upper charging level	V_{DELU}	V_{FB} > K_{RESU} x V_{FBR}	1.6	1.9	2.15	V
Lower detection threshold	V_{DELTH}	V_{DELAY} decreasing	0.7	0.9		

TYPICAL CHARACTERISTICS CURVES



TYPICAL CHARACTERISTICS CURVES

Figure 16. Minimum On Time vs. Junction Temperature

Figure 17. Minimum Off Time vs. Junction Temperature

GENERAL INFORMATION

INPUT VOLTAGE

An Undervoltage Lockout (UVLO) circuit monitors the input, and inhibits switching and resets the Soft start circuit if there is insufficient voltage for proper regulation. The NCV890204 can regulate a 3.3 V output with input voltages above 4.5 V and a 5.0 V output with an input above 6.5 V.

The NCV890204 withstands input voltages up to 40 V.

To limit the power lost in generating the drive voltage for the Power Switch, the switching frequency is reduced by a factor of 2 when the input voltage exceeds the V_{IN} Frequency Foldback threshold V_{FLDUP} (see Figure 25). Frequency reduction is automatically terminated when the input voltage drops back below the V_{IN} Frequency Foldback threshold V_{FLDDN}.

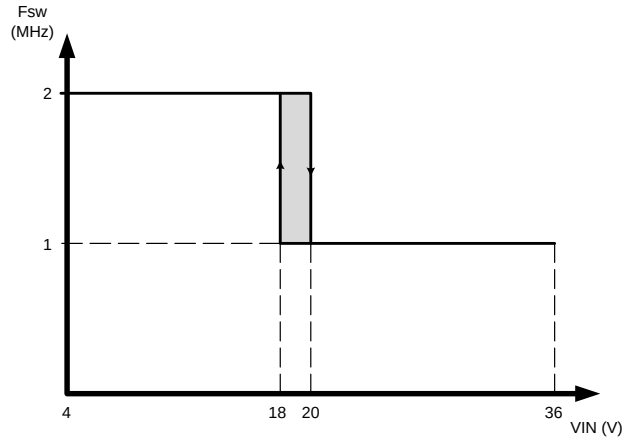


Figure 25. NCV890204 Switching Frequency Reduction at High Input Voltage

ENABLE

The NCV890204 is designed to accept either a logic level signal or battery voltage as an Enable signal. EN low induces a 'sleep mode' which shuts off the regulator and minimizes its supply current to a couple of μA typically (I_{qSD}) by disabling all functions. Upon enabling, voltage is established at the DRV pin, followed by a soft start of the switching regulator output.

SOFT−START

Upon being enabled or released from a fault condition, and after the DRV voltage is established, a soft start circuit ramps the switching regulator error amplifier reference voltage to the final value. During soft start, the average switching frequency is lower than its normal mode value (typically 2 MHz) until the output voltage approaches regulation.

SLOPE COMPENSATION

A fixed slope compensation signal is generated internally and added to the sensed current to avoid increased output voltage ripple due to bifurcation of inductor ripple current at duty cycles above 50%. The fixed amplitude of the slope compensation signal requires the inductor to be greater than a minimum value, depending on output voltage, in order to avoid sub harmonic oscillations. For 3.3 V and 5 V output voltages, the recommended inductor value is 4.7 μH.

SHORT CIRCUIT FREQUENCY FOLDBACK

During severe output overloads or short circuits, the NCV890204 automatically reduces its switching frequency. This creates duty cycles small enough to limit the peak current in the power components, while maintaining the ability to automatically reestablish the output voltage if the overload is removed. If the current is still too high after the switching frequency folds back to 500 kHz, the regulator enters an auto recovery burst mode that further reduces the dissipated power.

CURRENT LIMITING

Due to the ripple on the inductor current, the average output current of a buck converter is lower than the peak current setpoint of the regulator. Figure 26 shows for a 4.7 μH inductor how the variation of inductor peak current with input voltage affects the maximum DC current the NCV890204 can deliver to a load.

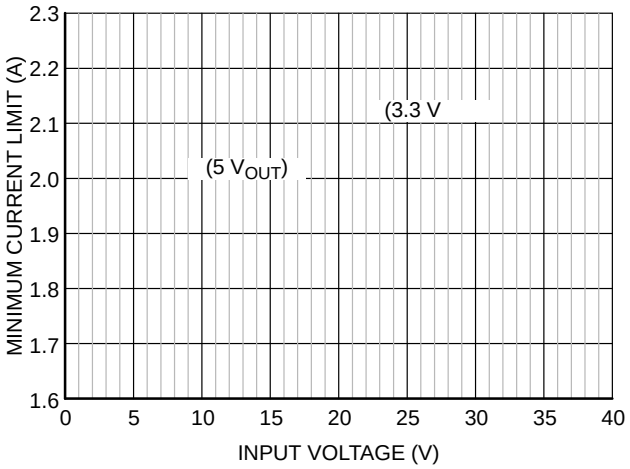


Figure 26. NCV890204 Load Current Capability with 4.7 μH Inductor

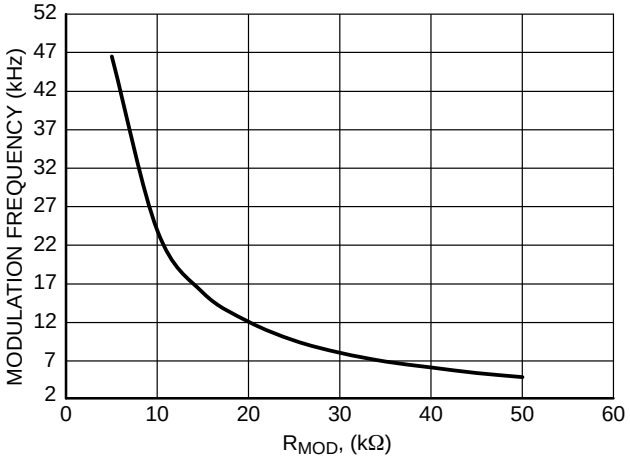


Figure 28. Modulation Frequency vs. RMOD

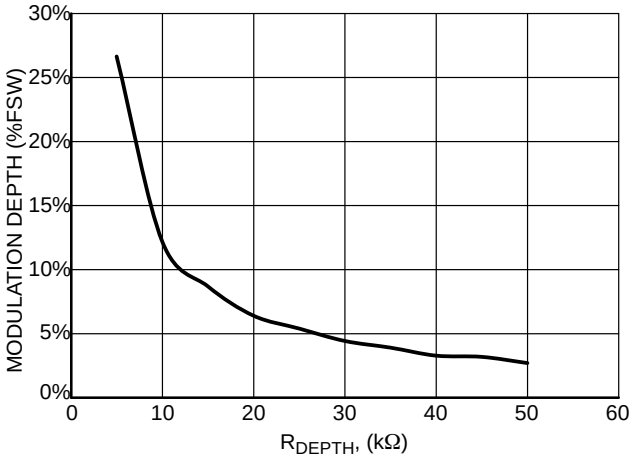
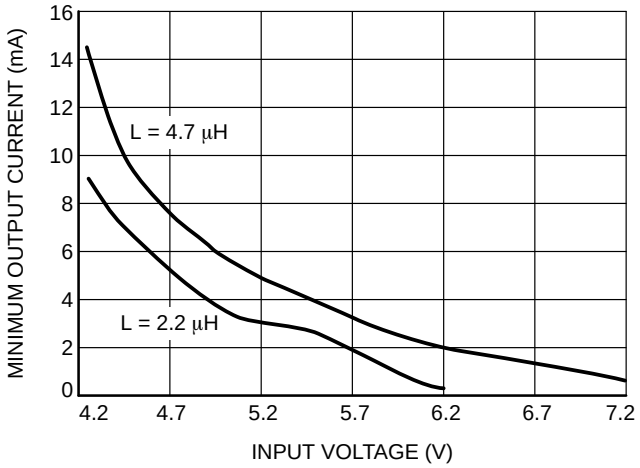


Figure 29. Modulation Depth vs. RDEPTH

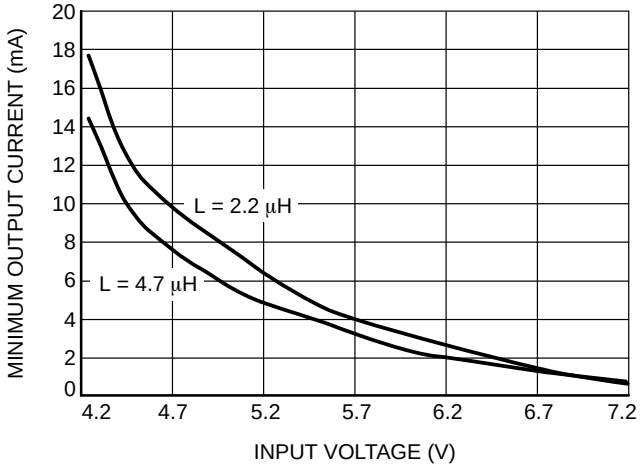
Spread spectrum is automatically turned off when there is a short to GND or an open circuit on either the RMOD pin or the RDEPTH pin.

BOOTSTRAP

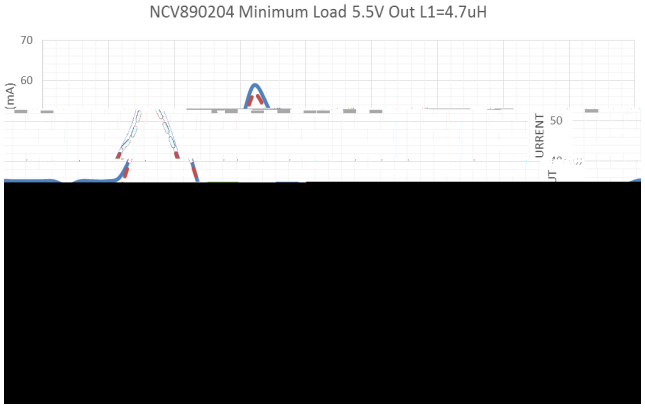
At the DRV pin an internal regulator provides a ground referenced voltage to an external capacitor (C_{DRV}), to allow fast recharge of the external bootstrap capacitor (C_{BST}



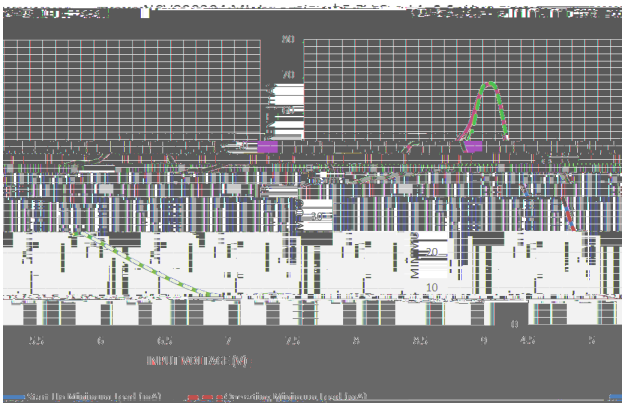
Typical Minimum Load 3.3 V Out



Typical Minimum Load 3.7 V Out



Typical Minimum Load 5.5 V Out, L1 = 4.7 μH



Typical Minimum Load 5.5 V Out, L1 = 2.2 μH

Figure 30. Minimum Load Current with Different Input and Output Voltages

Figure 31. Output Voltage Detection

When operating in continuous conduction mode (CCM), the output voltage is equal to the input voltage multiplied by the duty ratio. Because the NCV890204 needs a sufficient bootstrap voltage to operate, its duty cycle cannot be 100%: it needs a minimum off time (t_{OFFmin}) to periodically re fuel the bootstrap capacitor C_{BST}. This imposes a maximum duty ratio

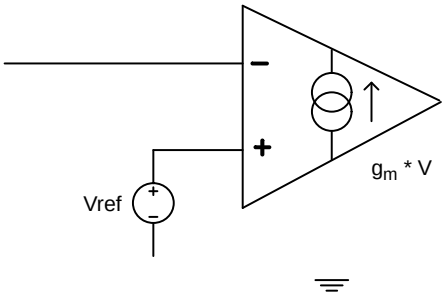
$$D_{MAX} = 1 - t_{OFFmin} \cdot F_{SW(min)},$$

with the switching frequency being folded back down to $F_{SW(min)}$ = 500 kHz to keep regulating at the lowest input voltage possible.

The drop due to the on state resistance is simply the voltage drop across the Switch resistance R_{DSON} at the given output current:

$$V_{SWdrop} = I_{OUT} \cdot R_{DSon}$$

Which773(TD-.0006 Tc9).8 of


−
+
Vref
+
−
g_m * V

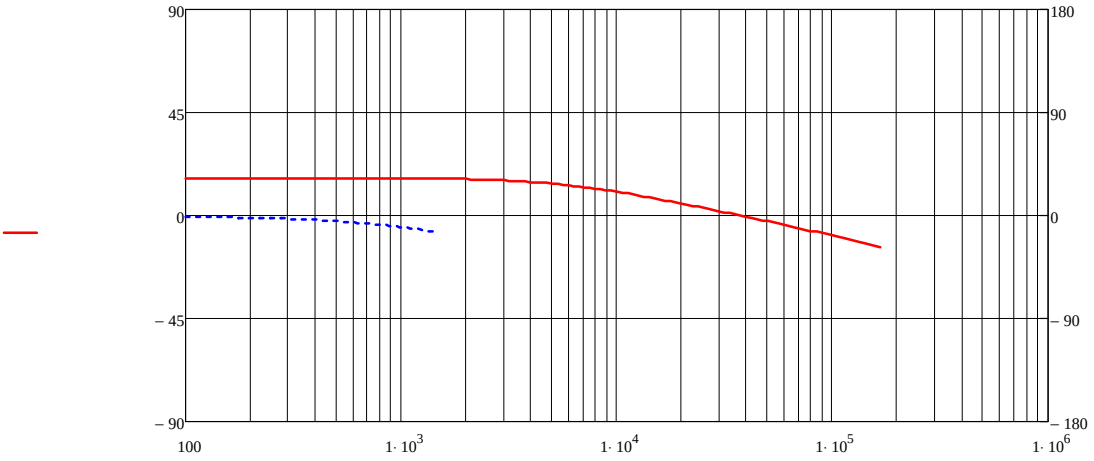


Figure 33. Power Stage Bode Plots

Figure 35 shows the bode plot of the OTA compensator

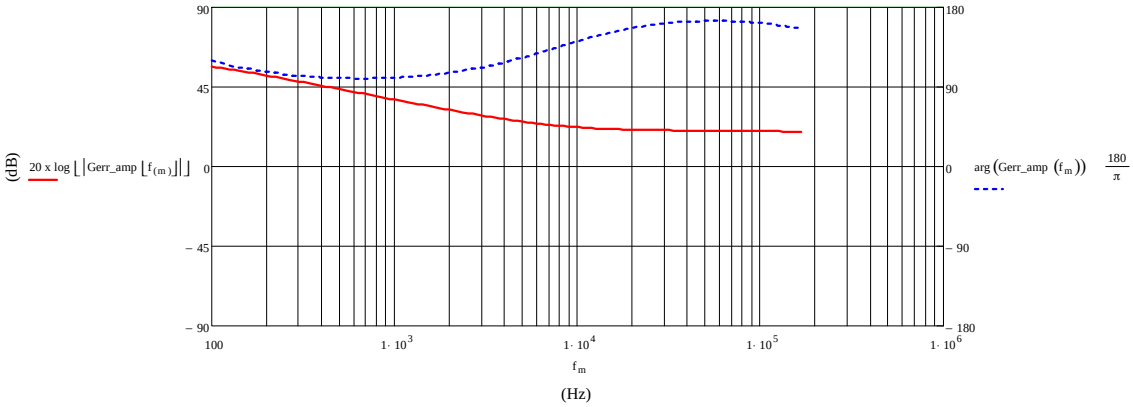
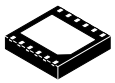
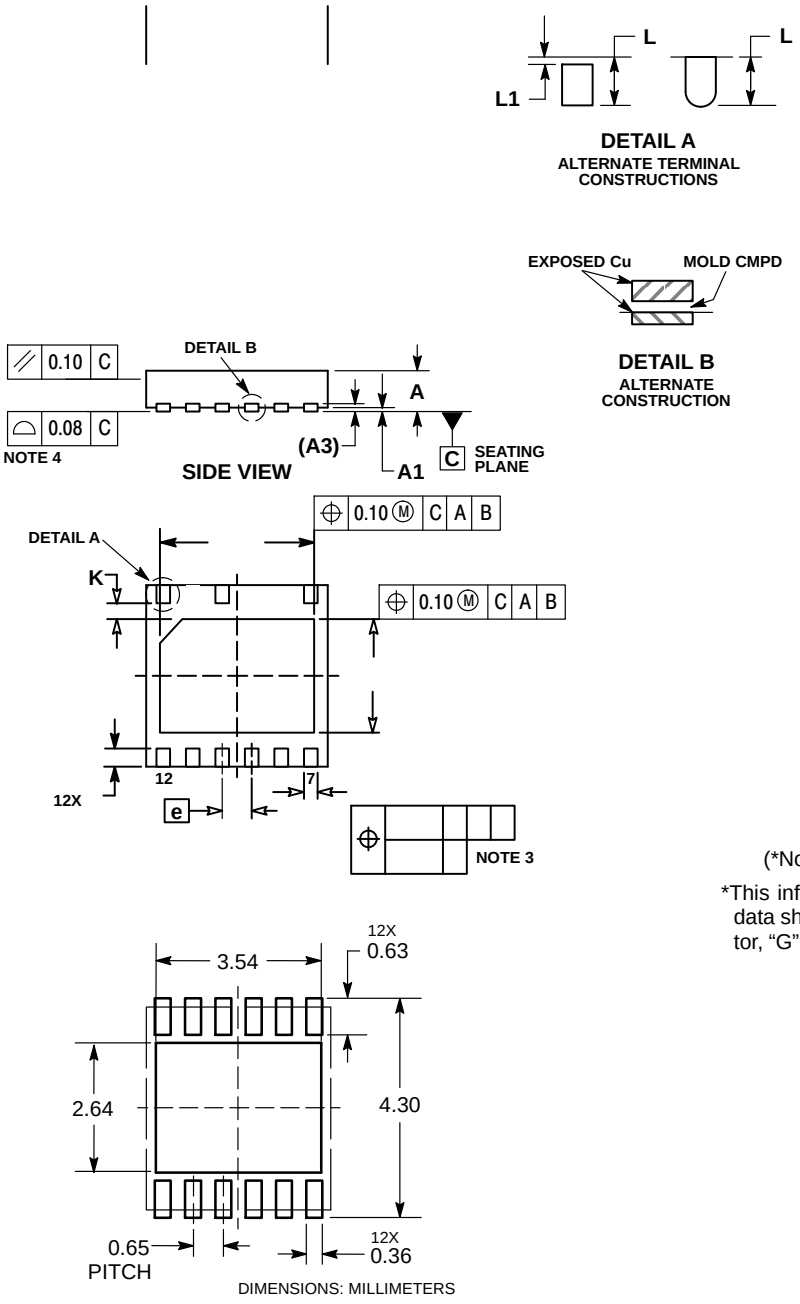


Figure 35. Bode Plot of the OTA Compensator

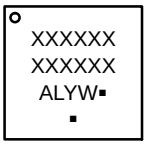




DIMENSIONS: MILLIMETERS

DIM	MILLIMETERS MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	4.00 BSC	
D2	3.30	3.50
E	4.00 BSC	
E2	2.40	2.60
e	0.65 BSC	
K	0.20	−−−
L	0.30	0.50
L1	−−−	0.15

GENERIC MARKING DIAGRAM*



XXXXXX= Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(*Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

onsemi, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba “**onsemi**” or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**’s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided “as−is” and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi**