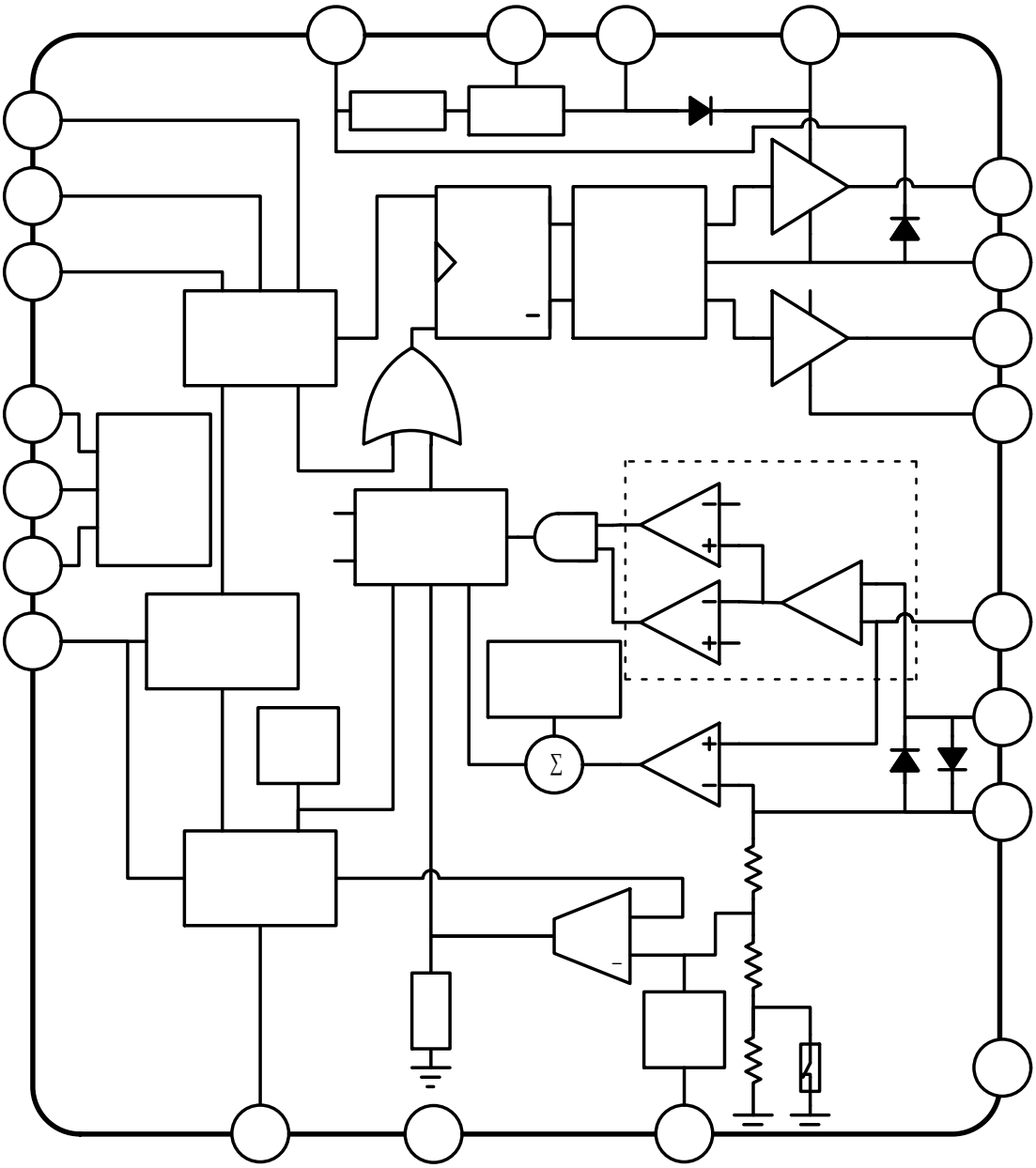

Figure 3. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. QFN24	Pin Name	Description
		µ
		–

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
		–	
≤		– –	
		– –	
		–	
		–	
		–	
		–	
		–	
		–	°
		–	°

ELECTRICAL CHARACTERISTICS μ μ

ELECTRICAL CHARACTERISTICS μ μ

− < < °

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
VSEL						
				−		
			−			μ
RESET						

ELECTRICAL CHARACTERISTICS µ µ

– < < °

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
SYNCHRONIZATION						

Figure 10. VREF vs Temperature

Figure 11. Oscillator Frequency vs Temperature

Table 2. MW891930MW01R2G VALUE RECOMMENDATIONS

Output Current (A)	MOSFET	3.65 V Option			4 V Option		
		Inductor Value (μH)	Current Sense Resistor (Ω)	Output Capacitance (ceramic) (μF)	Inductor Value (μH)	Current Sense Resistor (Ω)	Output Capacitance (Ceramic) (μF)

Input Voltage

An undervoltage lockout (UVLO) circuit monitors the input and can inhibit switching and reset the soft−start circuit if there is insufficient voltage for proper regulation. Depending on the output conditions (voltage option and loading), the NCV891930 may lose regulation and run in drop−out mode before reaching the UVLO threshold. When the input voltage is sufficiently low so that the part cannot regulate due to maximum duty cycle limitation, the high−side MOSFET can be kept on continuously for up to 32 clock cycles (16 μs), to help lower the minimum voltage at which the controller loses regulation.

An overvoltage monitoring circuit automatically terminates switching and disables the output if the input exceeds 37 V (minimum). However, the NCV891930 can withstand input voltages up to 45 V.

GL has a ~140 ns minimum pulse width requirement when VIN < VIN_LOW. Depending on the duty ratio requirement resulting from VIN, output voltage and operating losses, one or more GH turn−off may be skipped to maintain output regulation. Despite the default 2 MHz operating frequency, this skipped pulse will result in the power stage exhibiting a switching frequency of 1 MHz or less.

To avoid skipping switching pulses and entering an uncontrolled mode of operation, the switching frequency is reduced by a factor of 2 when input voltage exceeds the V_{IN} frequency foldback threshold (see Figure 18 below). Frequency reduction is automatically terminated when the input voltage drops back to below the VIN frequency voltage foldback threshold. This also helps limit the MOSFET switching power losses and reduce losses for generating the drive voltage for the Power Switches at high input voltage. Above the frequency foldback threshold, improved efficiency may be expected due to the lower switching frequency.

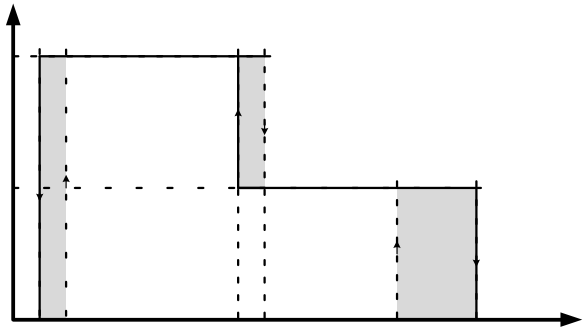

Figure 18. NCV891930 Worst Case Switching Frequency Profile vs Input Voltage

Output Voltage

The output may be programmed to VSEL_LO when VSEL is ground referenced.

When VSEL is connected to DBIAS via an optional 10 kΩ resistor, the output voltage is programmed to VSEL_HI.

The output voltage setting option must be selected prior to enabling the IC via the EN pin. The voltage setting option will be latched prior to initiation of soft−start. The voltage option latch will be reset whenever the EN pin is toggled or during a UVLO event.

IC VIN

A 1 μF decoupling capacitor is recommended between IC−VIN and ground. PCAg capaj33..45acitor is reco011 Tc.1077 Tw(A 1)Tj/F3 6.6.01para8 TwthisTj2.7.52m..9766 0 TD9 Tc.0011 T

Soft Start

STATE DIAGRAM

Figures 21 and 22 and illustrate the state diagram for the NCV891930.

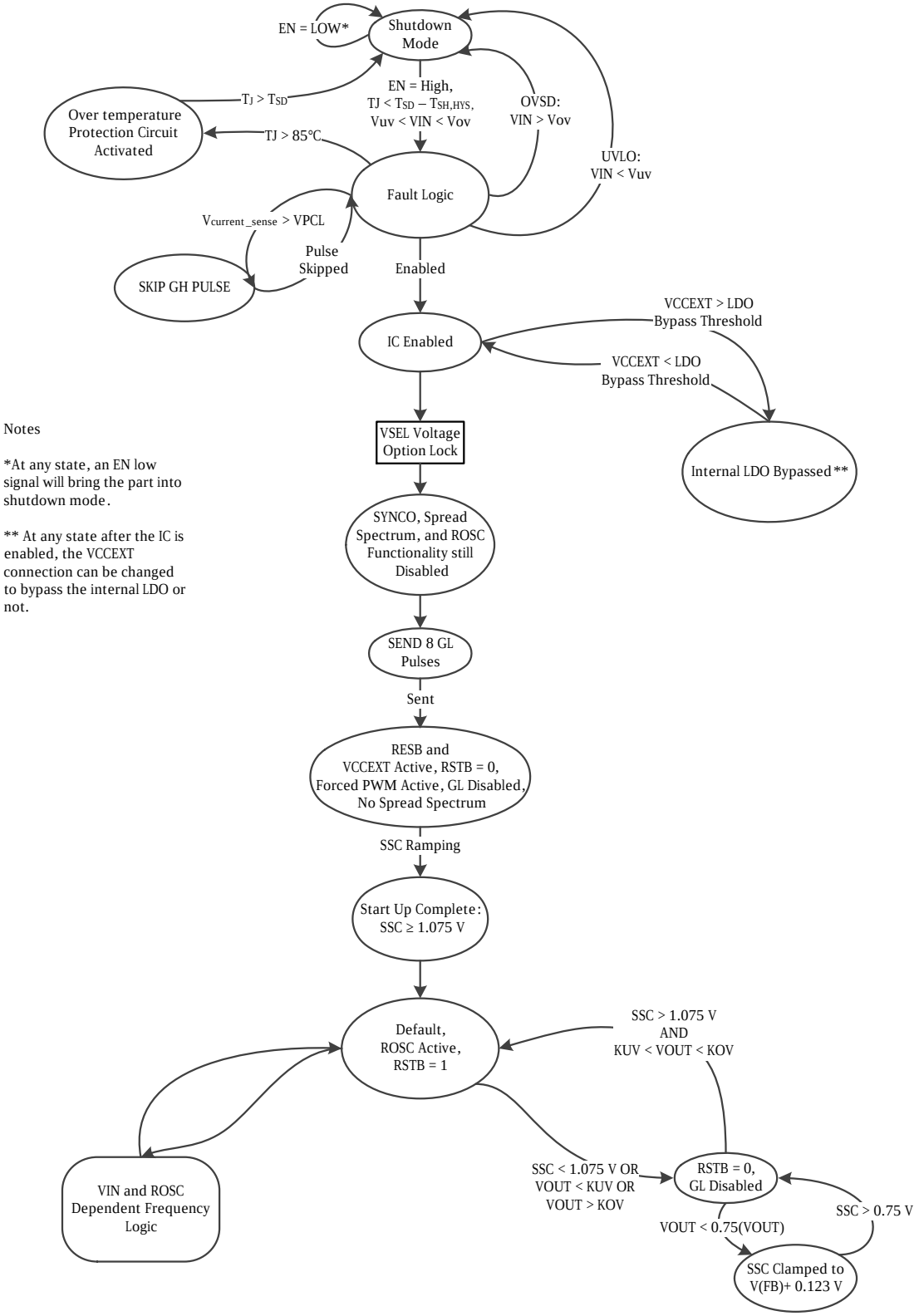

Figure 21. NCV891930 State Diagram

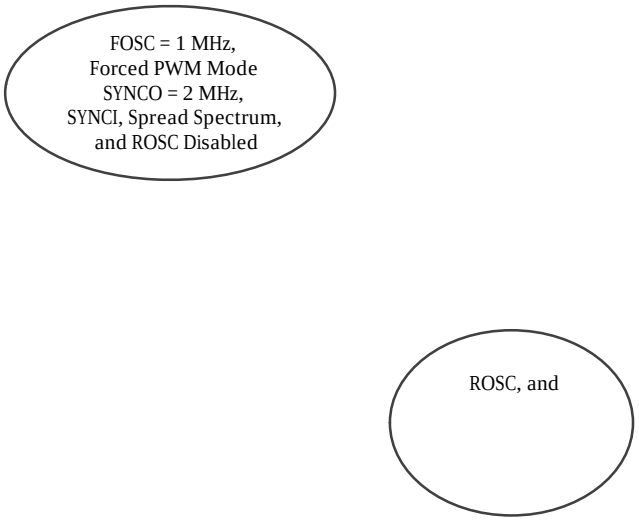

Figure 22. NCV891930 State Diagram – Dependent Switching Logic

Peak Current Mode Control

The NCV891930 incorporates a current mode control scheme, in which the PWM ramp signal is derived from the power switch current. This ramp signal is compared to the output of the error amplifier to control the on − time of the power switch. The oscillator is used as the frequency clock to ensure a PWM switching operation. The resulting control scheme features several advantages over conventional voltage mode control. First, derived directly from the inductor, the ramp signal responds immediately to line voltage transients. This eliminates the delay caused by the output filter and the error amplifier, which is commonly found in voltage mode controllers. The second benefit comes from inherent pulse − by − pulse current limiting by merely clamping the peak switching current. Finally, since current mode commands an output current rather than voltage, the filter offers only a single pole to the feedback loop. This permits simpler internal compensation.

A fixed slope compensation signal is generated internally and added to the sensed current to avoid increased output voltage ripple due to bifurcation of inductor ripple current at duty cycles above 50%. The fixed amplitude of the slope compensation signal requires the inductor to be less than a maximum value, depending on output voltage, in order to avoid sub−harmonic oscillations. Recommended inductor values are described in Table 2. Other values may be possible.

Current Sensing (CSP CSN):

V_CS is derived from VIN. It is a supply input for the internal current sense amplifier and should never be used to power external circuitry. The V_CS ceramic decoupling capacitor a minimum of 50 V voltage rating.

Kelvin connections to current sense resistor (RSNS) are required. CSP−CSN feedback nodes must not be in−line with the power path. An example of a good design practice is to connect the sense lines at the center of the inside edge of the sense resistors (Figure 23).

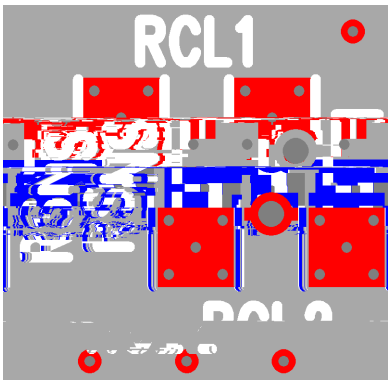

Figure 23. Kelvin Sense Location for Parallel Current Sense Resistors

As a result of the IC's CSP−CSN high input impedance, noise reduction measures should be used for effective noise immunity from the current sense feedback traces.

- Current sense resistors have a small inherent parasitic inductance that will result in a small voltage excursion equaling $L_{RSNS} \cdot \delta I_L / \delta t$ distortion superimposed on the triangular current sense waveform. The differential noise resulting from such a distortion can be minimized with the use of parallel sense resistors. The amplitude of such a distortion is difficult to predict (data not

CSN pin sources a bias current of amplitude $I_{BIAS,CSN}$. RSF2 will create a voltage offset on the CSP−CSN differential current sense current. This offset may be taken into account using the following current CSP−CSN current sense expression.

$$= \frac{\qquad}{\qquad} = \frac{+ \quad \cdot}{\qquad\qquad\qquad\qquad}$$

In the event of an overvoltage (VOUT > K_{UVRIS}), an internal comparator enables a 1 mA current source discharge path on VOUT within typically 2.7 μs. The overvoltage comparator is set 7.5% above the 1 V feedback voltage reference (i.e. 1.075 V) and has a 68 mV hysteresis.

Enable

An EN pin ground referenced resistor is not required. The IC has a pull−down current ($E_{I,EN}$). For low system I_Q operating requirements, such a resistor would result in a larger input quiescent current consumption when the IC is in an enabled state.

The NCV891930 is designed to accept either a logic−level signal or battery voltage as an Enable signal. However, if voltages above 45 V are expected, EN should be tied to VIN through a 10 kΩ resistor to limit the current flowing into the pin's internal ESD clamp.

A low signal on Enable induces a shutdown mode which shuts off the regulator and minimizes its supply current to less than 6 μA by disabling all functions. Pull−down R_{ENLO_VOUT} between IC−VOUT and IC−GND is present if VIN > 4.5 V to permit discharging the power supply output voltage.

Once the IC is enabled, a soft−start is always initiated.

The IC has internal filtering to prevent spurious operation from noise on EN. There is a t_{SSDLY} delay between the EN command entering a logic−high state and initiation of soft−start activity on pin SSC. There is an approximately 15 μs delay between the EN command entering a logic−low state and cessation of PWM activity.

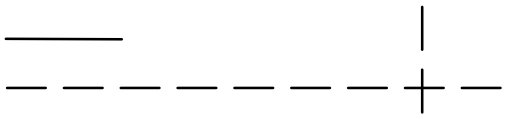

Figure 26. EN Low Response Behaviour

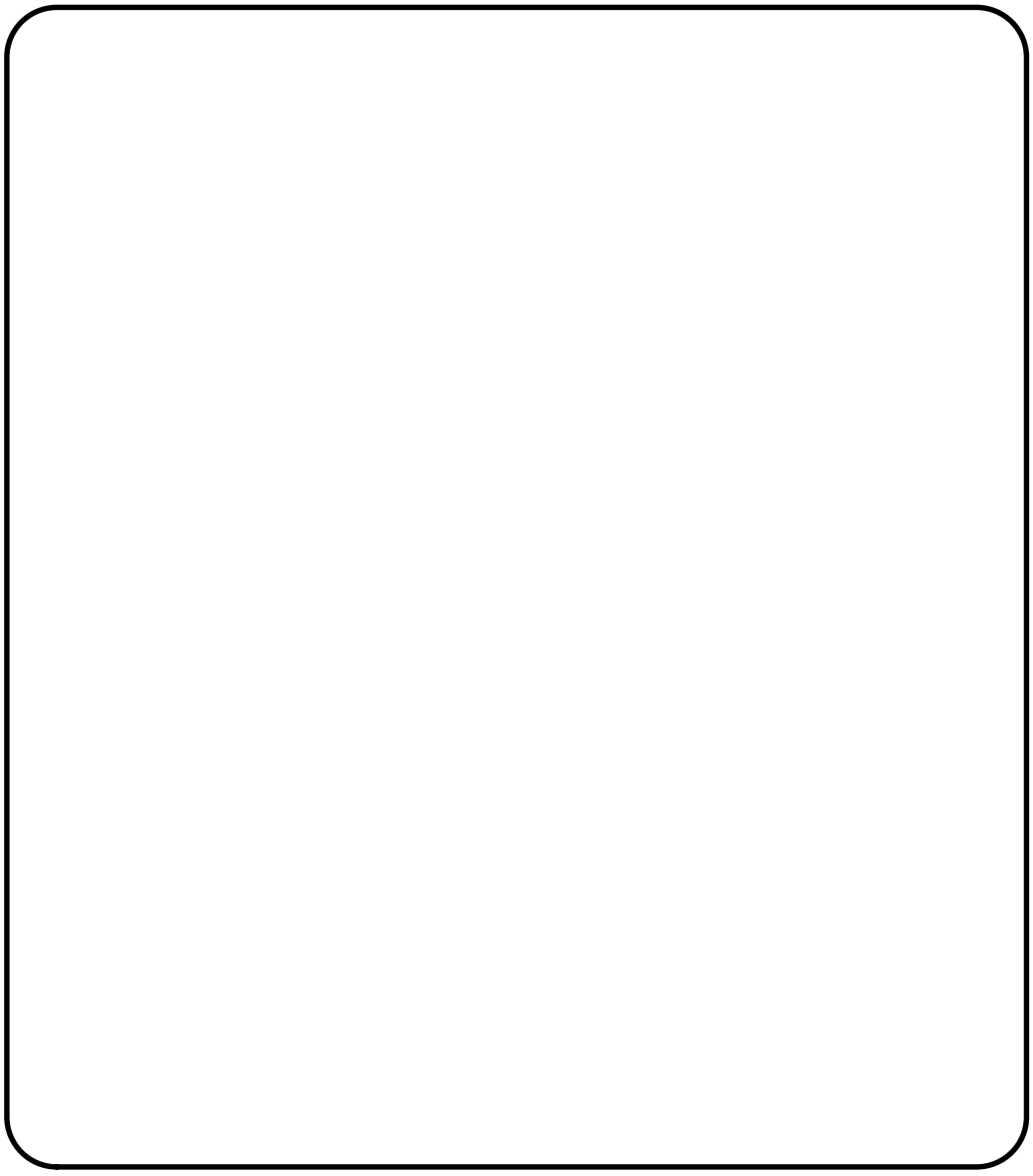

Figure 30. Simplified Block Diagram

SYNC Feature

V_SO is a supply voltage strictly intended for the SYNCO output driver and should never be used to power external circuitry. The V_SO ceramic decoupling capacitor a minimum of 5 V voltage rating. Ground this pin if not used.

An external pulldown resistor is recommended at the SYNCI pin if the function is unused. The SYNCO pulse may be used to synchronize other NCV891930 ICs. If a part does not have its switching frequency controlled by the SYNCI input, the part will operate at the oscillator frequency. A rising edge of the SYNCI pulse causes an NCV891930 to send a GH pulse. If another rising edge does not arrive at the SYNCI pin, the NCV891930 oscillator will take control after the master reassertion time delay which may last up to 3 clock cycles if SYNCI is stopped at logic−low level, up to 4 cycles if SYNCI is stopped at logic−high level. During the master reassertion time, GH will be off and GL will be active−high (i.e. switch node tied to ground). As a result, SYNCI operating mode change is not advised.

After soft−start event, SYNCO becomes active when SSC voltage > 1.075 V. V_{HSYNCI} requires about 2 V headroom from VIN to for its rated amplitude. Amplitude will be reduced when VIN is below approximately 5 V.

During pulse−skip mode, the oscillator enters sleep mode for low I_Q operation power management and SYNCO is inactive. SYNCO functionality resumes when the IC exits pulse−skip mode.

When active, SYNC0 is in phase with SYNCI (Figure 31). Rise/fall edge waveforms have a typical 10 ns delay relative to corresponding SYNCI waveform edges.

SYNCO will be a fixed frequency 2 MHz signal under normal voltage when part is in current limit and VOUT drops by 7.5% (K_{UVFAL}). The VOUT pin sinks 0 mA under typical conditions when the SYNCI pin is logic−low. The VOUT pin sinks 1 mA when any of the following conditions are present:

- SYNCI = logic−high
- SYNCI is driven by an external clock
- VIN < VIN_low threshold
- VIN > frequency foldback threshold voltage

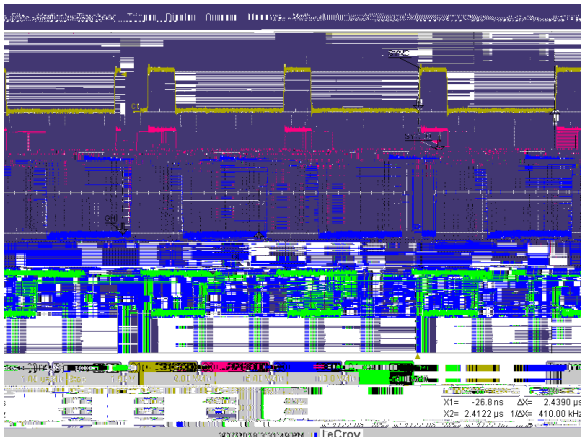

Figure 31. SYNCO Behaviour

Diode Emulation Mode

Diode−emulation mode is active when SYNCI is either open or grounded. A comparator in the current sense block detects the CSP−CSN voltage transition from a positive voltage (positive inductor current) to 0 V (0 A inductor current). When 0 A is detected, the bottom GL signal turns off the low side MOSFET to prevent negative inductor current.

Pulse Skip Mode

7	8	9	1	3

Spread Spectrum

In SMPS devices, switching translates to higher efficiency. As a consequence, the switching also leads to a higher EMI profile. We can greatly reduce some of the peak radiated emissions with some spread spectrum techniques. Spread spectrum is a method used to reduce the peak electromagnetic emissions of a switching regulator.

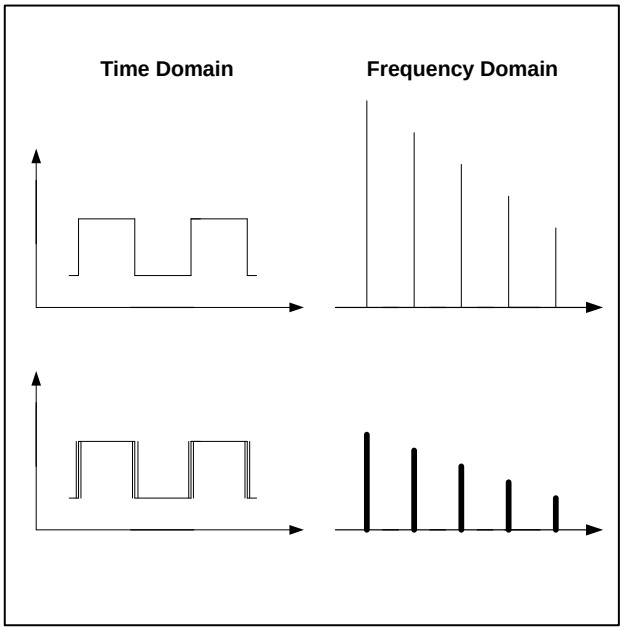

Figure 34. Spread Spectrum Comparison

The NCV891930 has spread spectrum functionality for reduced peak radiated emissions. This IC uses a pseudo−random generator to set the oscillator frequency to one of 8 discrete frequency bins. Each digital bin represents a shift in frequency by 40 kHz over the range 2.0 MHz to

APPLICATIONS INFORMATION

Design Methodology

Choosing external components encompasses the following design process:

1. Operational parameter definition
2. Switching frequency selection (ROSC)
3. Output inductor selection
4. Current sense resistor selection
5. Output capacitor selection
6. Input capacitor selection
7. Thermal considerations

(1) Operational Parameter Definition

Before proceeding with the rest of the design, certain operational parameters must be defined. These are application dependent and include the following:

V_{IN}: input voltage, range from minimum to maximum with a typical value [V]
V_{OUT}: output voltage [V]
I_{OUT}: output current, range from minimum to maximum with initial start−up value [A]
I_{CL}: desired typical current limit [A]

A number of basic calculations must be performed up−front to use in the design process, as follows:

= ————

= ————

= ————

where: D_{MIN}: minimum duty cycle (ideal) [%]
$V_{IN(MAX)}$: maximum input voltage [V]
D: typical duty cycle (ideal) [%]
$V_{IN(TYP)}$: typical input voltage [V]
D_{MAX}: maximum duty cycle (ideal) [%]
$V_{IN(MAX)}$: minimum input voltage [V]

These are ideal duty cycle expressions; actual duty cycles will be marginally higher than these values. Actual duty cycles are dependent on load due to voltage drops in the MOSFETs, inductor and current sense resistor.

(2) Switching Frequency Selection (ROSC)

Selecting the switching frequency is a trade−off between component size and power losses. Operation at higher switching frequencies allows the use of smaller inductor and capacitor values to achieve the same inductor current ripple and output voltage ripple. However, increasing the frequency increases the switching losses of the MOSFETs, leading to decreased efficiency, especially noticeable at light loads.

Typically, the switching frequency is selected to avoid interfering with signals of known frequencies. Often, in this case, the frequency can be programmed to a lower value with ROSC and then a higher−frequency signal can be applied to the SYNC pin to increase the frequency dynamically to avoid given frequencies. A spread spectrum signal could also be used for the SYNC input, as long as the lowest frequency in the range is above the programmed frequency set by ROSC. Additionally, the highest SYNC frequency volo

s42102CJ6.1839ed e⁑e d inclu56 frequencie7e

R

load transients, impacting incremental dynamic response. While the inductor is slewing current during this time, output capacitors must supply the load current. Therefore, decreasing the inductance allows for less output capacitance to hold the output voltage up during a load transient.

A ripple current δI_L equaling 20−40% of the output rated current is a typical objective when selecting an inductor value for a duty ratio D normally selected at the nominal input operating voltage. The inductor value may be calculated using the following expression:

$$= \frac{\cdot \quad -}{\delta \quad \cdot}$$

Inductor saturation current is specified by inductor manufacturers as the current at which the inductance value has dropped a certain percentage from the nominal value, typically 10−30%. It is recommended to choose an inductor with saturation current sufficiently higher than the peak output current, such that the inductance is very close to the nominal value at the peak output current. This introduces a safety factor and allows for more optimized compensation.

Inductor efficiency is another consideration when selecting an output inductor. Inductor losses include DC and AC winding losses as well as core losses. Core losses are proportional to the amplitude of the ripple current and operating frequency.

AC winding losses are based on the AC resistance of the winding and the RMS ripple current through the inductor, which is much lower than the DC current. AC winding losses are due to skin and proximity effects and are typically much less than the DC losses, but increase with frequency. The DC winding losses in the inductor can be calculated with the following equation:

$$= \quad \cdot$$

where: $P_{L(DC)}$: DC winding losses in the output inductor
R_{DC}: DC resistance of the output inductor (DCR)

(4) Current Sense Resistor Selection

Current sensing for peak current mode control relies on the amplitude of the inductor current. The current is translated into a voltage via a current sense resistor placed in series with the output inductor located between the output inductor and capacitors. The resulting voltage is then measured differentially by a current sense amplifier, generating a single−ended output to use as a control signal. If a current sense π−filter is implemented as in Figure 24, the following expression may be used to determine the current sense resistor value.

$$+ \quad \cdot$$
$$=$$

During soft−start, the inductor current must provide current to the load as well as current to charge the output capacitor. The current limit defines the maximum current which the inductor is allowed to conduct. Setting the inrush current to the current limit places a limit on the maximum capacitor value (inductor ripple current not considered) as follows:

$$= \frac{\left(\quad - \quad \right) \cdot}{\quad}$$

where: C_{MAX}: maximum output capacitance [F]

Capacitors should also be chosen to provide acceptable

Table 6. ORDERING INFORMATION

Device	Output Voltage	Marking	Package	Shipping
			–	

DISCONTINUED

			–	
			–	

DISCONTINUED: **onsemi**