B ck C n e e - L
V l age, D al,
2.1 MH

NCV896530

The NCV896530 dual step−down dc−dc converter is a monolithic integrated circuit dedicated to automotive driver information systems from a downstream voltage rail.

Both channels are externally adjustable from 0.9 V to 3.3 V and can source totally up to 1600 mA. Converters are running at 2.1 MHz switching frequency above the sensitive AM band and operate 180 out of phase to reduce large amounts of current demand on the rail. Synchronous rectification offers improved system efficiency.

The NCV896530 provides additional features expected in automotive power systems such as integrated soft−start, hiccup mode current limit and thermal shutdown protection. The device can also be synchronized to an external clock signal in the range of 2.1 MHz.

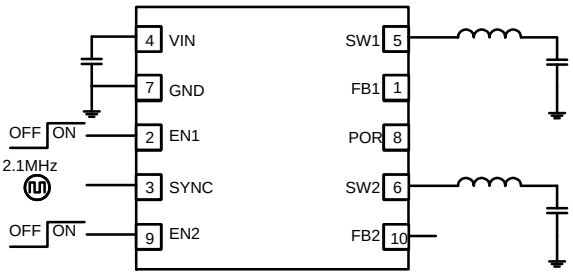
The NCV896530 is available in a space saving, 3 x 3 mm 10−pin DFN package.

Features

- Synchronous Rectification for Higher Efficiency
- 2.1 MHz Switching Frequency, 180 Out−of−Phase
- Sources up to 1600 mA Total and 1 A Per Channel
- Adjustable Output Voltage from 0.9 V to 3.3 V
- 2.7 V to 5.5 V Input Voltage Range
- Thermal Limit and Short Circuit Protection
- Auto Synchronizes with an External Clock
- Wettable Flanks – DFN
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This is a Pb−Free Device

Typical Applications

- Audio
- Infotainment
- Vision System
- Instrumentation

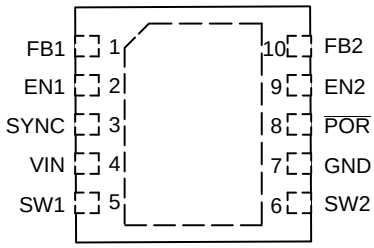


MARKING DIAGRAM

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Device

(Note: Microdot may be in either location)

PIN CONNECTIONS

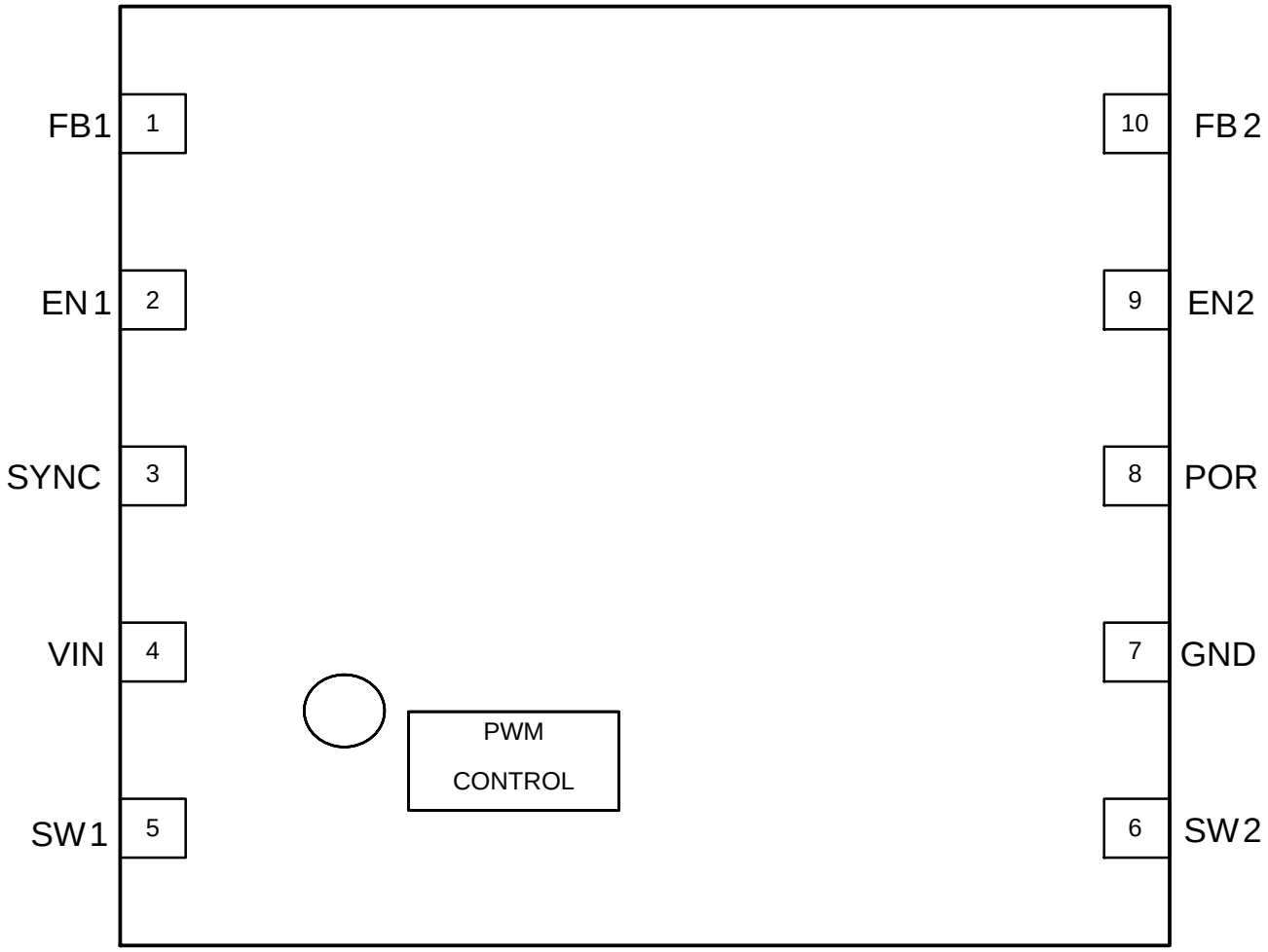


(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 8 of this data sheet.

BLOCK DIAGRAM



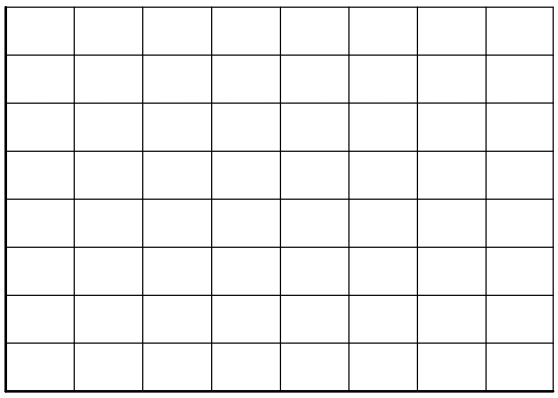
PIN FUNCTION DESCRIPTION

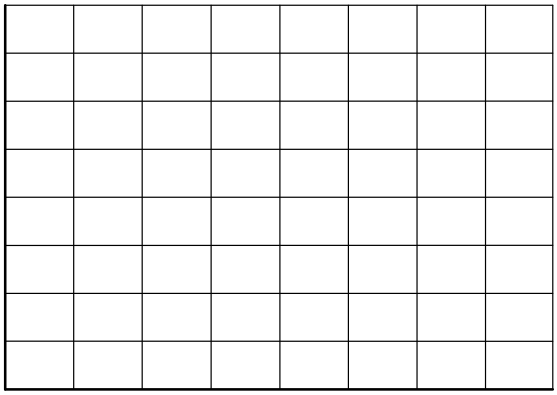
Pin	Pin Name	Type	Description
1	FB1	Analog Input	Feedback voltage from the output 1. This is the input to the error amplifier.
2			

ELECTRICAL CHARACTERISTICS (2.7 V < V_{IN} < 5.5 V, Min and Max values are valid for the temperature range −40 C T_J +150 C unless noted otherwise, and are guaranteed by test design or statistical correlation, Typical values are referenced to T_A = +25 C)

Rating	Conditions	Symbol	Min	Typ	Max	Unit
INPUT VOLTAGE						
Quiescent Current	SYNC = GND, V_{FB} = 0 V					

TYPICAL CHARACTERISTICS CURVES





TYPICAL CHARACTERISTICS CURVES

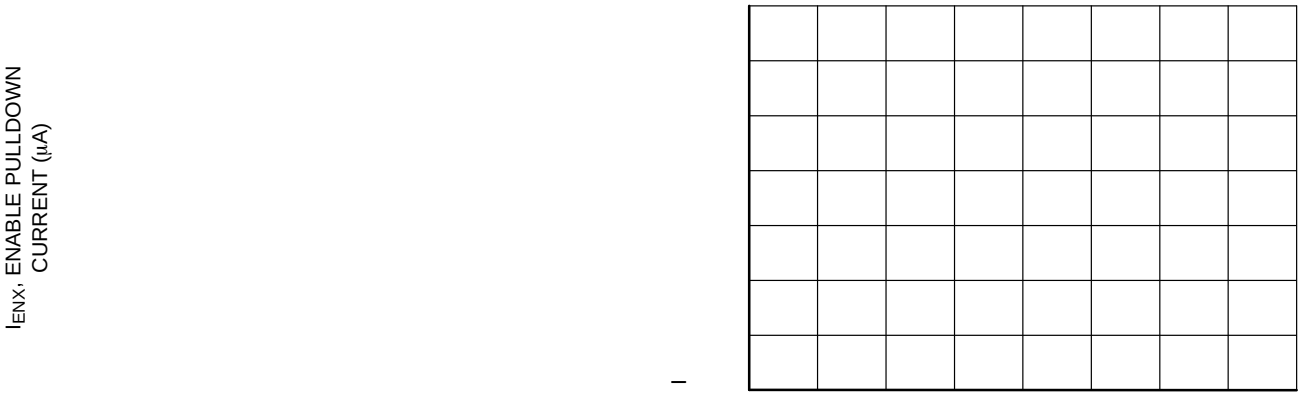


Figure 9. Enable Pulldown Current vs. Temperature

DC/DC OPERATION DESCRIPTION

PWM Operating Mode

The output voltage of the device is regulated by modulating the on−time pulse width of the main switch Q1 at a fixed 2.1 MHz frequency (Figure 13).

The switching of the PMOS Q1 is controlled by a flip−flop driven by the internal oscillator and a comparator that compares the error signal from an error amplifier with the sum of the sensed current signal and compensation ramp.

The driver switches ON and OFF the upper side transistor (Q1) and switches the lower side transistor in either ON state or in current source mode.

At the beginning of each cycle, the main switch Q1 is turned ON by the rising edge of the internal oscillator clock. The inductor current ramps up until the sum of the current sense signal and compensation ramp becomes higher than the error amplifier's voltage. Once this has occurred, the PWM comparator resets the flip−flop, Q1 is turned OFF while the synchronous switch Q2 is turned in its current source mode. Q2 replaces the external Schottky diode to reduce the conduction loss and improve the efficiency. To avoid overall power loss, a certain amount of dead time is introduced to ensure Q1 is completely turned OFF before Q2 is being turned ON.

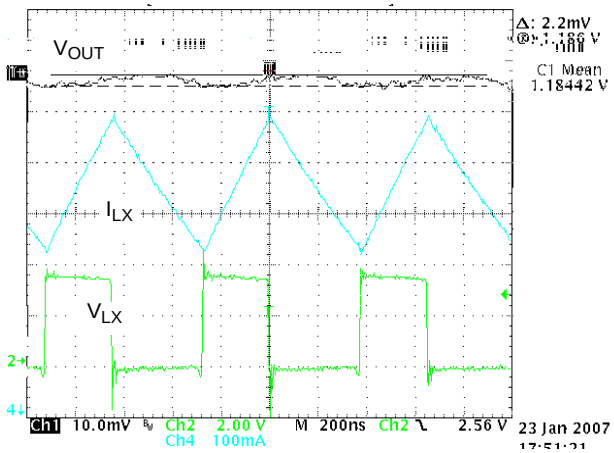


Figure 13. PWM Switching Waveforms

(V_{IN} = 3.6 V, V_{OUT} = 1.2 V, I_{OUT} = 600 mA, Temp = 25 C)

Soft−Start

The NCV896530 uses soft start to limit the inrush current when the device is initially powered up or enabled. Soft start is implemented by gradually increasing the reference voltage until it reaches the full reference voltage. During startup, a pulsed current source charges the internal soft start capacitor to provide gradually increasing reference voltage. When the voltage across the capacitor ramps up to the nominal reference voltage, the pulsed current source will be switched off and the reference voltage will switch to the regular reference voltage.

Over Current Hiccup Protection

When the current through the inductor exceeds the current limit the NCV896530 enters over current hiccup mode. When an over current event is detected the NCV896530 disables the outputs and attempts to re−enable the outputs after the hiccup time. The part remains off for the hiccup time and then goes through the power on reset procedure. If the excessive load has been removed then the output stage re−enables and operates normally; however, if the excessive load is still present the cycle begins again. Internal heat dissipation is kept to a minimum as current will only flow during the reset time of the protection circuitry. The hiccup mode is continuous until the excessive load is removed.

Low Dropout Operation

The NCV896530 offers a low input−to−output voltage difference. The NCV896530 can operate at 100% duty cycle on both channels.

In this mode the PMOS (Q1) remains completely ON. The minimum input voltage to maintain regulation can be calculated as:

$$V_{IN(min)} = V_{OUT(max)} + \left(I_{OUT} \times \left(R_{DS(on)} + R_{INDUCTOR}\right)\right) \quad \text{(eq. 1)}$$

V_{OUT}: Output Voltage
I_{OUT}: Max Output Current
$R_{DS}(ON)$: P−Channel Switch $R_{DS(on)}$
$R_{INDUCTOR}$: Inductor Resistance (DCR)

Power On Reset

The Power On Reset (POR) is pulled low when one of the converter is out of 90% of the regulation. When both outputs are in the range of regulation. If only one channel is active, POR stays low. When the inactive regulator becomes enabled, POR is kept low until the output reaches its voltage range. A pull−up resistor is needed to this open drain output. The resistor may be connected to VIN or to an output voltage of one regulator if the device supplied can not accept VIN on the IO. POR is low when NCV896530 is off. Leave the POR pin unconnected when not used.

Frequency Synchronization

The NCV896530 can be synchronized with an external clock signal by using the SYNC pin (1.8 MHz − 2.4 MHz). During synchronization, the outputs are in phase.

Thermal Shutdown

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. If the junction temperature exceeds T_{SD}, the device shuts down. In this mode all power transistors and control circuits are turned off. The device restarts in soft start after the temperature drops below 130 C min. This feature is provided to prevent catastrophic failures from accidental device overheating.